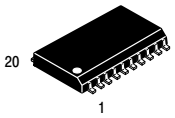
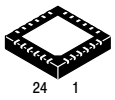
# 2.5 V/3.3 V Any Level Positive Input to -3.3 V/-5.5 V NECL Output Translator

# MC100EP91




SOIC−20 WB
DW SUFFIX
CASE 751D




QFN−24
MN SUFFIX
CASE 485L

## Description

The MC100EP91 is a triple any level positive input to NECL output translator. The device accepts LVPECL, LVTTL, LVCMOS, HSTL, CML or LVDS signals, and translates them to differential NECL output signals (−3.0 V/−5.5 V).

To accomplish the level translation the EP91 requires three power rails. The $V_{CC}$ pins should be connected to the positive power supply, and the $V_{EE}$ pin should be connected to the negative power supply. The GND pins are connected to the system ground plane. Both $V_{EE}$ and $V_{CC}$ should be bypassed to ground via 0.01 μF capacitors.

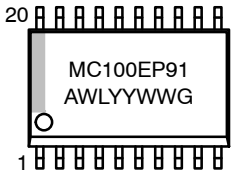
Under open input conditions, the $\overline{D}$ input will be biased at $V_{CC}/2$ and the D input will be pulled to GND. These conditions will force the Q outputs to a low state, and Q outputs to a high state, which will ensure stability.

The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

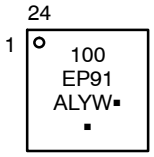
## Features

- Maximum Input Clock Frequency = > 2.0 GHz Typical
- Maximum Input Data Rate = > 2.0 Gb/s Typical
- 500 ps Typical Propagation Delay
- Operating Range:
  $V_{CC}$ = 2.375 V to 3.8 V; $V_{EE}$ = −3.0 V to −5.5 V; GND = 0 V
- Q Output will Default LOW with Inputs Open or at GND
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

## MARKING DIAGRAMS*




SOIC−20 WB




QFN−24

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC100EP91MNG | QFN−24 (Pb−Free) | 92 Units / Tube |

**DISCONTINUED** (Note 1)

| | | |
|---|---|---|
| MC100EP91DWG | SOIC−20 WB (Pb-Free) | 38 Units / Tube |
| MC100EP91DWR2G | SOIC−20 WB (Pb-Free) | 1000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

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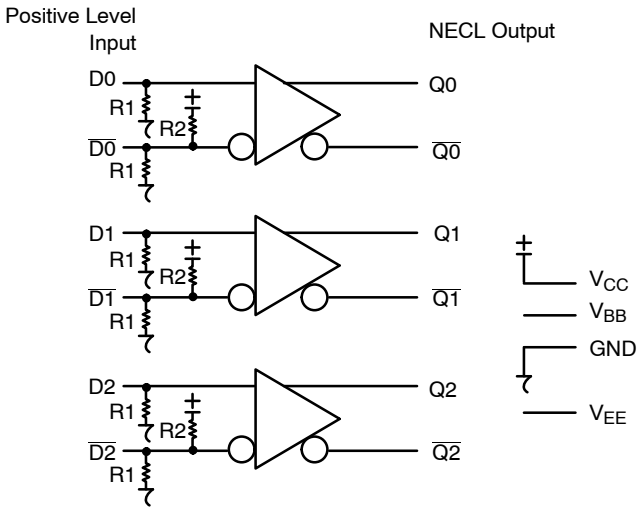



**Figure 1. Logic Diagram**

**Table 1. PIN DESCRIPTION**

| Pin | | Name | I/O | Default State | Description |
|---|---|---|---|---|---|
| SOIC | QFN | | | | |
| 1, 20 | 3, 4, 12 | $V_{CC}$ | – | – | Positive Supply Voltage. All $V_{CC}$ Pins must be Externally Connected to Power Supply to Guarantee Proper Operation |
| 10 | 15, 16 | $V_{EE}$ | – | – | Negative Supply Voltage. All $V_{EE}$ Pins must be Externally Connected to Power Supply to Guarantee Proper Operation |
| 14, 17 | 19, 20, 23, 24 | GND | – | – | Ground |
| 4, 7 | 7, 11 | $V_{BB}$ | – | – | ECL Reference Voltage Output |
| 2, 5, 8 | 5, 8, 13 | D[0:2] | LVPECL, LVDS, LVTTL, LVCMOS, CML, HSTL Input | Low | Noninverted Differential Inputs [0:2]. Internal 75 kΩ to GND. |
| 3, 6, 9 | 6, 9, 14 | $\overline{D[0:2]}$ | LVPECL, LVDS, LVTTL,LVCMOS, CML, HSTL Input | High | Inverted Differential Inputs [0:2]. Internal 75 kΩ to GND and 75 kΩ to $V_{CC}$. When Inputs are Left Open They Default to ($V_{CC}$ – GND) / 2 |
| 19,16,13 | 2, 22, 18 | Q[0:2] | NECL Output | – | Noninverted Differential Outputs [0:2]. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} – 2$ V |
| 18,15,12 | 1, 21, 17 | $\overline{Q[0:2]}$ | NECL Output | – | Inverted Differential Outputs [0:2]. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} – 2$ V |
| 11 | 10 | NC | – | – | No Connect. The NC Pin is NOT Electrically Connected to the Die and may Safely be Connected to Any Voltage from $V_{EE}$ to $V_{CC}$ |
| N/A | – | EP | – | | Exposed Pad (Note 1) |

1. The thermally conductive exposed pad on the package bottom (see case drawing) must be attached to a heat−sinking conduit and may only be electrically connected to $V_{EE}$ (not GND).



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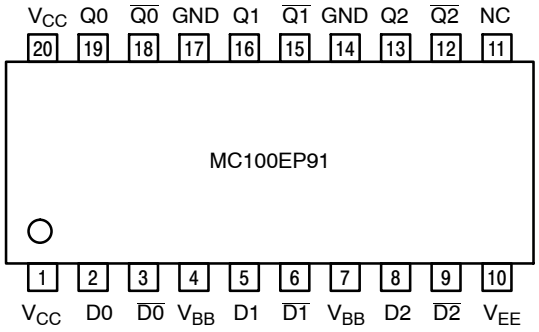



**Figure 2. SOIC−20 Lead Pinout** (Top View)

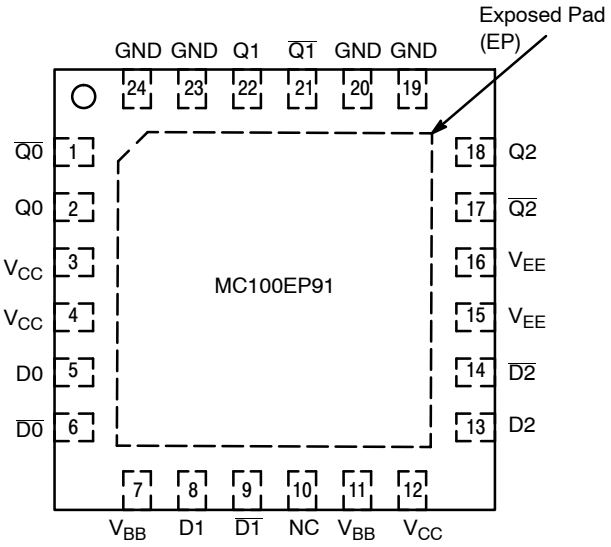



**Figure 3. QFN−24 Lead Pinout** (Top View)*

*All $V_{CC}$, $V_{EE}$ and GND pins must be externally connected to a power supply and the underside exposed pad must be attached to an adequate heat−sinking conduit to guarantee proper operation.

**Table 2. ATTRIBUTES**

| Characteristics | Value |
|---|---|
| Internal Input Pulldown Resistor (R1) | 75 kΩ |
| Internal Input Pullup Resistor (R2) | 75 kΩ |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | <br>> 2 kV<br>> 150 V<br>> 2 kV |
| Moisture Sensitivity (Note 1) | Pb-Free Pkg |
| SOIC−20 WB<br>QFN−24 | Level 3<br>Level 1 |
| Flammability Rating<br>Oxygen Index: 28 to 34 | <br>UL 94 V−0 @ 0.125 in |
| Transistor Count | 446 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.



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**Table 3. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive Power Supply | GND = 0 V | | 3.8 to 0 | V |
| $V_{EE}$ | Negative Power Supply | GND = 0 V | | −6 | V |
| $V_I$ | Positive Input Voltage | GND = 0 V | $V_I \le V_{CC}$ | 3.8 to 0 | V |
| $V_{OP}$ | Operating Voltage | GND = 0 V | $V_{CC} - V_{EE}$ | 9.8 | V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA |
| $I_{BB}$ | PECL $V_{BB}$ Sink/Source | | | ±0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)<br>JESD 51−3 (1S-Single Layer Test Board) | 0 lfpm<br>500 lfpm | SOIC−20 WB<br>SOIC−20 WB | 90<br>60 | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)<br>JESD 51−6 (2S2P Multilayer Test Board) with Filled Thermal Vias | 0 lfpm<br>500 lfpm | QFN−24<br>QFN−24 | 37<br>32 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC−20 WB<br>QFN−24 | 30 to 35<br>11 | °C/W |
| $T_{sol}$ | Wave Solder (Pb-Free) | | | 225 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 4. DC CHARACTERISTICS POSITIVE INPUTS** ($V_{CC}$ = 2.5 V, $V_{EE}$ = −3.0 V to −5.5 V, GND = 0 V (Note 1))

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| $I_{CC}$ | Positive Power Supply Current | 10 | 14 | 20 | 10 | 14 | 20 | 10 | 14 | 20 | mA |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 1335 | | $V_{CC}$ | 1335 | | $V_{CC}$ | 1335 | | $V_{CC}$ | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | GND | | 875 | GND | | 875 | GND | | 875 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 2) | 0 | | 2.5 | 0 | | 2.5 | 0 | | 2.5 | V |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$)<br>D<br>$\overline{D}$ | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input parameters vary 1:1 with $V_{CC}$. $V_{CC}$ can vary +1.3 V / −0.125 V.
2. $V_{IHCMR}$ min varies 1:1 with GND. $V_{IHCMR}$ max varies 1:1 with $V_{CC}$.



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**Table 5. DC CHARACTERISTICS POSITIVE INPUT** ($V_{CC}$ = 3.3 V; $V_{EE}$ = −3.0 V to −5.5 V; GND = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{CC}$ | Positive Power Supply Current | 10 | 16 | 24 | 10 | 16 | 24 | 10 | 16 | 24 | mA |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 2135 | | $V_{CC}$ | 2135 | | $V_{CC}$ | 2135 | | $V_{CC}$ | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | GND | | 1675 | GND | | 1675 | GND | | 1675 | mV |
| $V_{BB}$ | PECL Output Voltage Reference | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 2) | 0 | | 3.3 | 0 | | 3.3 | 0 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current (@ $V_{IH}$) | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current (@ $V_{IL}$)<br>D<br>$\overline{D}$ | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | <br>0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input parameters vary 1:1 with $V_{CC}$. $V_{CC}$ can vary +0.5 / −0.925 V.
2. $V_{IHCMR}$ min varies 1:1 with GND. $V_{IHCMR}$ max varies 1:1 with $V_{CC}$.

**Table 6. DC CHARACTERISTICS NECL OUTPUT** ($V_{CC}$ = 2.375 V to 3.8 V; $V_{EE}$ = −3.0 V to −5.5 V; GND = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Negative Power Supply Current | 40 | 50 | 60 | 38 | 50 | 68 | 38 | 50 | 68 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | −1145 | −1020 | −895 | −1145 | −1020 | −895 | −1145 | −1020 | −895 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | −1945 | −1770 | −1600 | −1945 | −1770 | −1600 | −1945 | −1770 | −1600 | mV |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Output parameters vary 1:1 with GND.
2. All loading with 50 Ω resistor to GND − 2.0 V.



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**Table 7. AC CHARACTERISTICS** ($V_{CC}$ = 2.375 V to 3.8 V; $V_{EE}$ = −3.0 V to −5.5 V; GND = 0 V)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OUTPP}$ | Output Voltage Amplitude ($f_{in}$ ≤ 1.0 GHz)<br>(Figure 4) ($f_{in}$ ≤ 1.5 GHz)<br>(Note 1) ($f_{in}$ ≤ 2.0 GHz) | 575<br>525<br>300 | 800<br>750<br>600 | | 600<br>525<br>250 | 800<br>750<br>550 | | 550<br>400<br>150 | 800<br>750<br>500 | | mV |
| $t_{PLH}$<br>$t_{PHL0}$ | Propagation Delay (Differential)<br>D to Q (Single-Ended) | 375<br>300 | 500<br>450 | 600<br>650 | 375<br>300 | 500<br>450 | 600<br>675 | 400<br>300 | 550<br>500 | 650<br>750 | ps |
| $t_{SKEW}$ | Pulse Skew (Note 2)<br>Output-to-Output (Note 3)<br>Part-to-Part (Diff) (Note 3) | | 15<br>25<br>50 | 75<br>95<br>125 | | 15<br>30<br>50 | 75<br>105<br>125 | | 15<br>30<br>70 | 80<br>105<br>150 | ps |
| $t_{JITTER}$ | RMS Random Clock Jitter (Note 4) ($f_{in}$ = 2.0 GHz)<br>Peak-to-Peak Data Dependant Jitter ($f_{in}$ = 2.0 Gb/s)<br>(Note 5) | | 0.5<br>20 | 2.0 | | 0.5<br>20 | 2.0 | | 0.5<br>20 | 2.0 | ps |
| $V_{INPP}$ | Input Voltage Swing (Differential Configuration)<br>(Note 6) | 200 | 800 | 1200 | 200 | 800 | 1200 | 200 | 800 | 1200 | mV |
| $t_r$, $t_f$ | Output Rise/Fall Times @ 50 MHz (20%−80%)<br>Q, $\overline{Q}$ | 75 | 150 | 250 | 75 | 150 | 250 | 75 | 150 | 275 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to GND − 2.0 V. Input edge rates 150 ps (20% − 80%).
2. Pulse Skew = $|t_{PLH} - t_{PHL}|$
3. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
4. RMS Jitter with 50% Duty Cycle Input Clock Signal.
5. Peak-to-Peak Jitter with input NRZ PRBS $2^{31-1}$ at 2.0 Gb/s.
6. Input voltage swing is a Single-Ended measurement operating in differential mode. The device has a DC gain of ≈50.

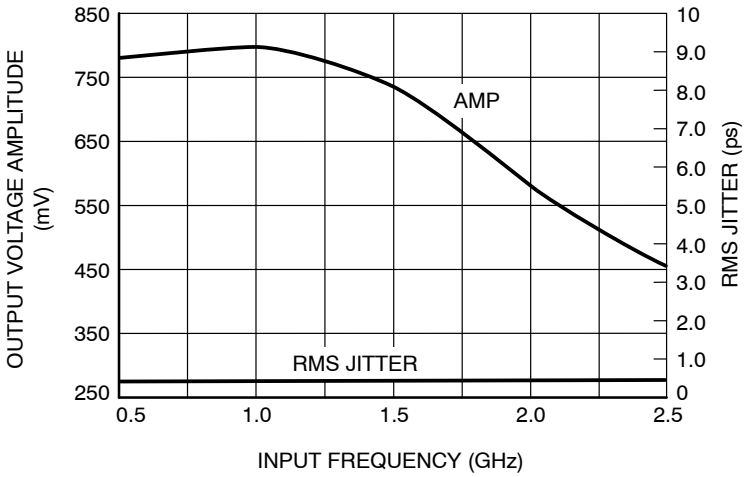



**Figure 4. Output Voltage Amplitude ($V_{OUTPP}$) / RMS Jitter vs. Input Frequency ($f_{in}$) at Ambient Temperature (Typical)**

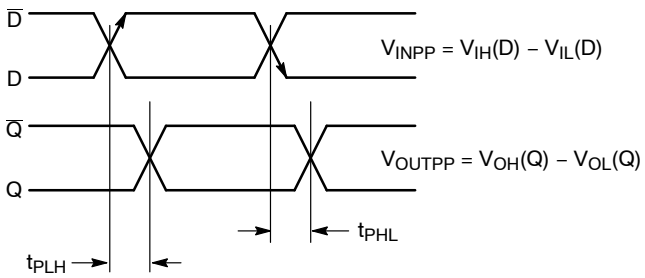



**Figure 5. AC Reference Measurement**



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### Application Information

All MC100EP91 inputs can accept LVPECL, LVTTL, LVCMOS, HSTL, CML, or LVDS signal levels. The limitations for differential input signal (LVDS, HSTL, LVPECL, or CML) are the minimum input swing of 150 mV and the maximum input swing of 3.0 V. Within these conditions, the input voltage can range from $V_{CC}$ to GND. Examples interfaces are illustrated below in a 50 Ω environment (Z = 50 Ω).

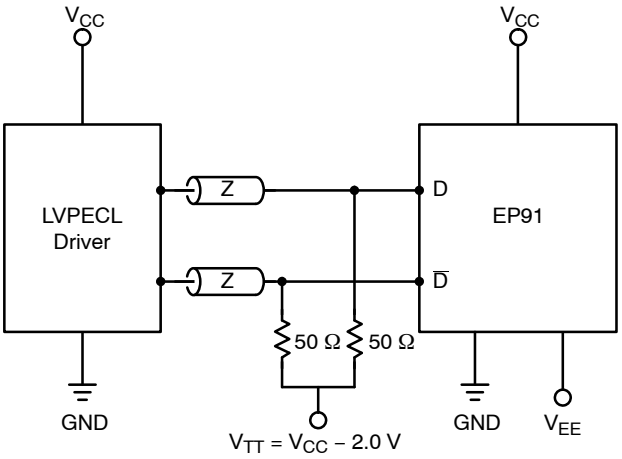



**Figure 6. Standard LVPECL Interface**

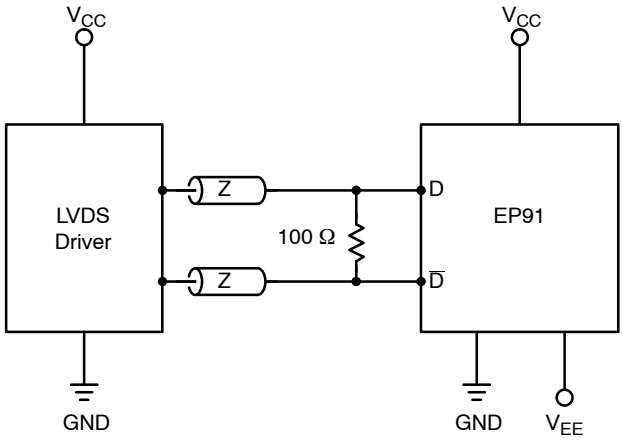



**Figure 7. Standard LVDS Interface**

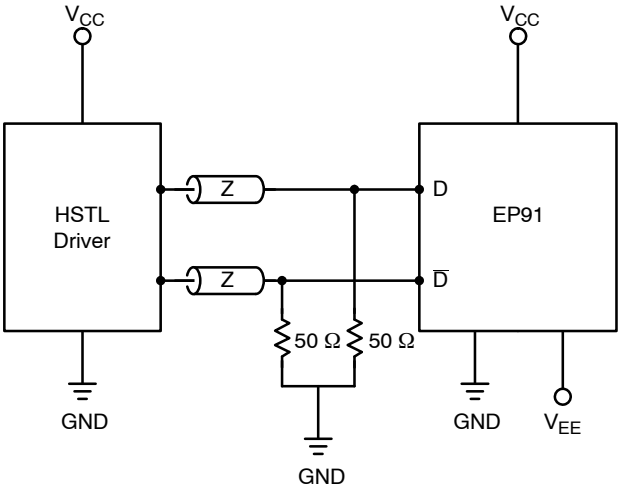



**Figure 8. Standard HSTL Interface**

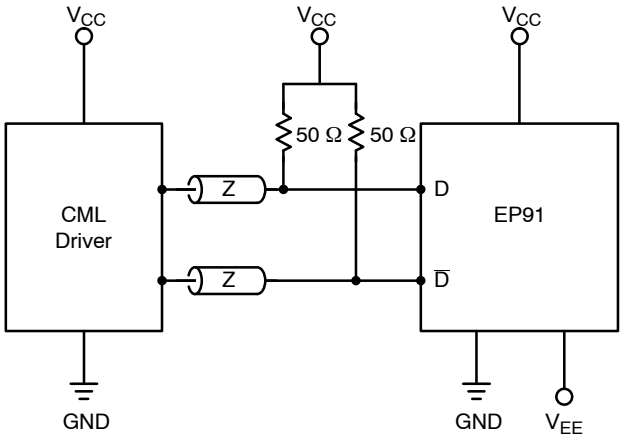



**Figure 9. Standard 50 Ω Load CML Interface**

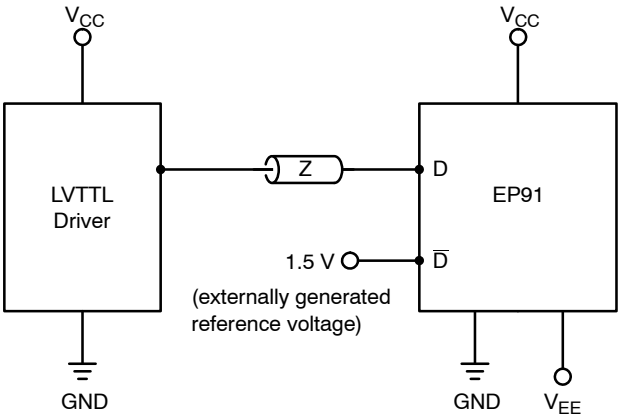



**Figure 10. Standard LVTTL Interface**

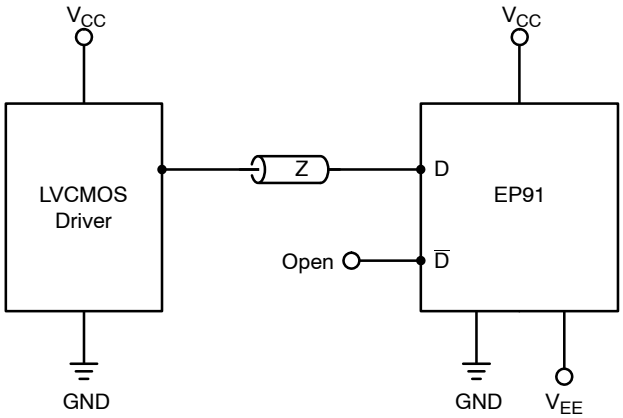



**Figure 11. Standard LVCMOS Interface ($\overline{D}$ will default to $V_{CC}$/2 when left open. A reference voltage of $V_{CC}$/2 should be applied to D input, if $\overline{D}$ is interfaced to CMOS signals)**



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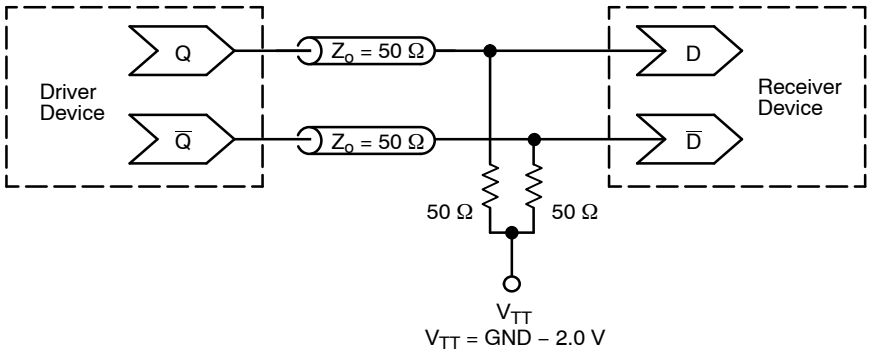



**Figure 12. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices)**

### Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

**AND8020/D** – Termination of ECL Logic Devices

**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices

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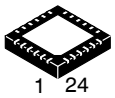


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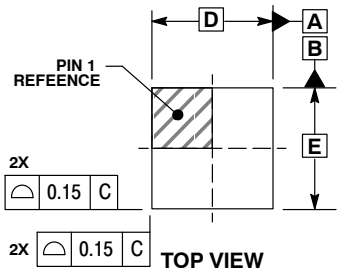
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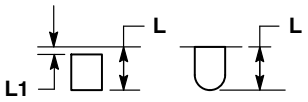
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CASE 485L
ISSUE B

DATE 05 JUN 2012

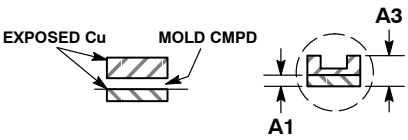



SCALE 2:1

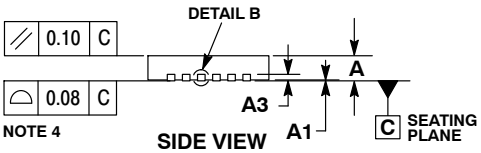



**DETAIL A**
ALTERNATE CONSTRUCTIONS

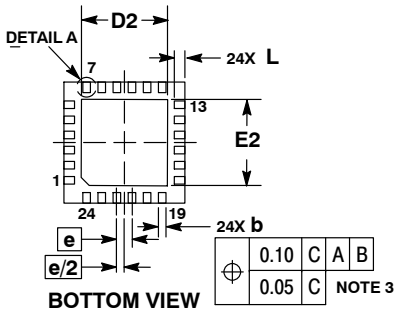



**DETAIL B**
ALTERNATE TERMINAL CONSTRUCTIONS




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 4.00 BSC | |
| D2 | 2.70 | 2.90 |
| E | 4.00 BSC | |
| E2 | 2.70 | 2.90 |
| e | 0.50 BSC | |
| L | 0.30 | 0.50 |
| L1 | 0.05 | 0.15 |




## GENERIC MARKING DIAGRAM*

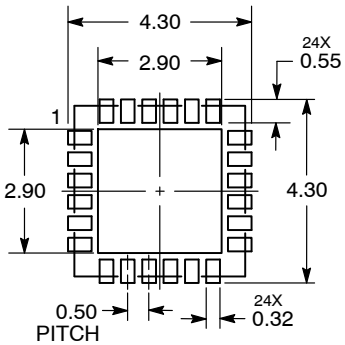



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

## RECOMMENDED SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
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