Wide Input 5 V, 50 mA, Automotive Regulator with Output Short-to-Battery Protection and Power OK

Discontinued Product

These parts are no longer in production The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: September 30, 2024

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to the A4481KLJTR-T.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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A4480

Wide Input 5 V, 50 mA, Automotive Regulator with Output Short-to-Battery Protection and Power OK

FEATURES AND BENEFITS

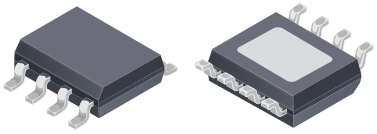
- Automotive AEC-Q100 qualified
- Wide operating range of 3.5 to 28 V, with 40 V load dump rating
- Linear regulator output with foldback short-circuit and short-to-battery protection
- Boost function to maintain output when input is low
- Power OK (POK) flag
- High-voltage logic-level enable input (ENB) for microprocessor or ignition control
- Pin-to-pin and pin-to-ground tolerant at every pin

APPLICATIONS

- Microcontroller power
- Transceivers (CAN, LIN, etc.) power supplies
- Sensors

PACKAGE

8-pin SOIC with exposed thermal pad (suffix LJ)



Not to scale

DESCRIPTION

The A4480 is a wide input regulator with complete control, diagnostics, and protection features that address many requirements of automotive applications. It includes a boost function to allow operation with input voltages from 3.5 to 28 V, while maintaining a 5 V output voltage. The A4480 is able to supply up to 50 mA of load current.

An enable pin (ENB) allows control of the regulator output. This pin is rated to operate at up to 40 V, so it can be connected directly to a car battery.

Diagnostic output from the A4480 includes an open-drain Power OK (POK) output to alert the microprocessor that a fault has occurred.

Protection features include input undervoltage lockout (UVLO), foldback overcurrent protection, output under/overvoltage protections (UV/OVP), and thermal shutdown (TSD). In addition, the output is protected from a short-to-battery event.

The A4480 device is available in an 8-pin eSOIC package with exposed pad for enhanced thermal dissipation. It is lead (PB) free, with 100% matte tin leadframe plating.

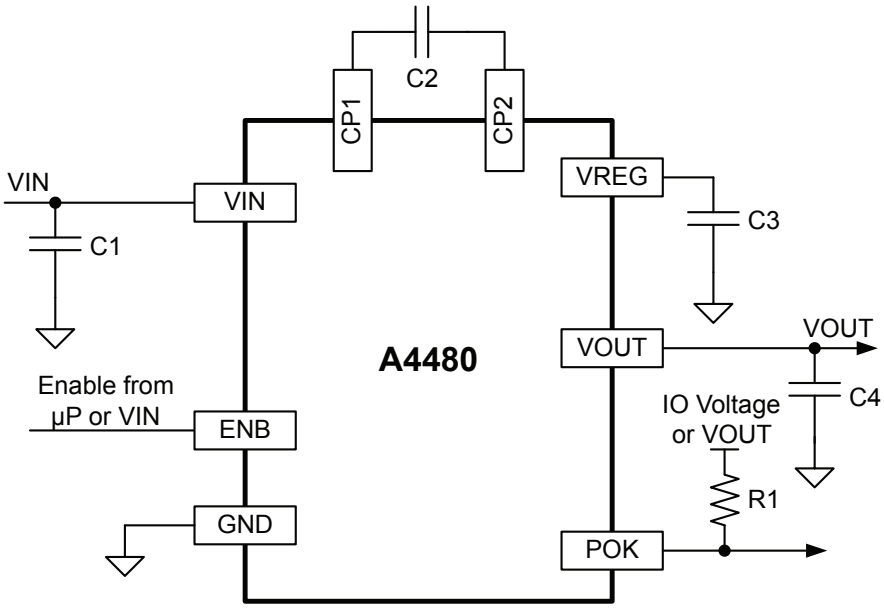


Figure 1: Typical Application Circuit

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SELECTION GUIDE

Part Number	Temperature Range (°C)	Package	Leadframe	Packing*
A4480KLJTR-T	–40 to 150	8-pin eSOIC with exposed thermal pad	Matte Tin	3000 pieces per 7-in. reel

*Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Notes	Rating	Unit
VIN, ENB, CP1	V_{IN}, V_{ENB}, V_{CP1}		−0.3 to 40	V
VCP2, VREG, VPOK	V_{CP2}, V_{REG}, V_{POK}		−0.3 to 20	V
VOUT	V_{OUT}	Independent of V_{IN}	−1 to 40	V
Junction Temperature Range	T_J		−40 to 165	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

*Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS*: May require derating at maximum conditions; see application section for optimization

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	eSOIC-8 with thermal pad (LJ) package on 4-layer PCB based on JEDEC standard	35	°C/W

*Additional thermal information available on the Allegro website.

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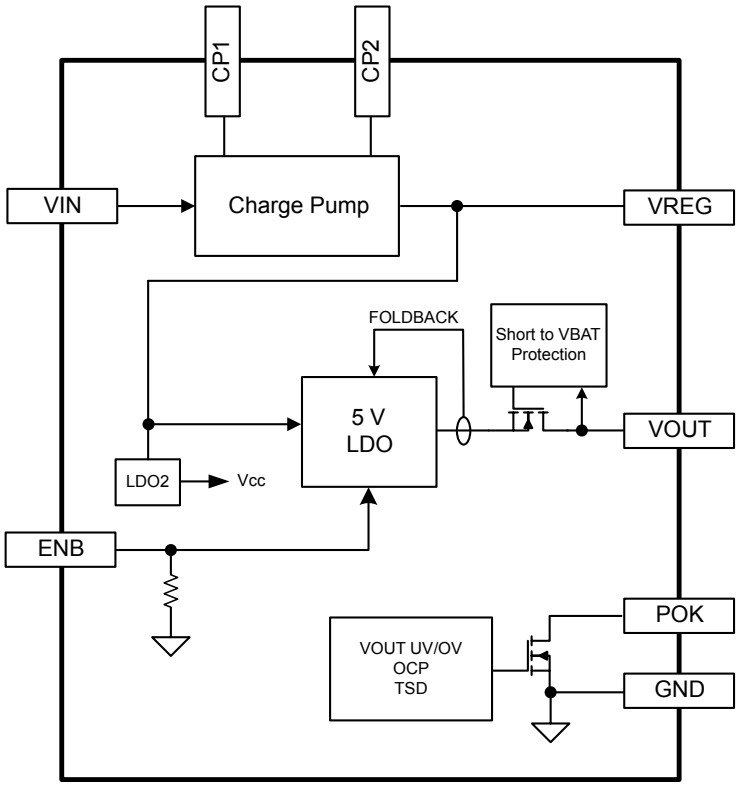
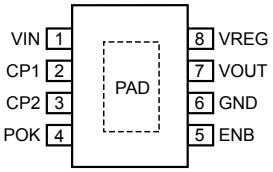


Figure 2: Functional Block Diagram

Pinout Diagram



Terminal List Table

Number	Name	Function
1	VIN	Connection for input voltage. Connect a 2.2 µF capacitor from this pin to GND. Keep capacitor close to A4480.
2	CP1	Internal charge pump flying capacitor connection, connect a 0.47 µF ceramic capacitor from this pin to the CP2 pin. Keep capacitor close to A4480.
3	CP2	Internal charge pump flying capacitor connection, use a 0.47 µF capacitor to CP1.
4	POK	Open-drain active-high Power OK signal. Use a 100 kΩ pull-up resistor to system IO rail or VOUT.
5	ENB	Regulator active high enable input. Can be connected to VIN or logic level signal.
6	GND	Ground pin.
7	VOUT	Regulated output pin. It is recommended to use a 4.7 µF ceramic capacitor from this pin to GND. Keep capacitor close to A4480.
8	VREG	Charge pump output which is input to internal linear regulator. Connect a 2.2 µF ceramic capacitor from this pin to GND. Keep capacitor close to A4480.

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ELECTRICAL CHARACTERISTICS [1]: Valid at 3.5 V ≤ V_{IN} ≤ 28 V, −40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
INPUT VOLTAGE						
Operating Input Voltage	V_{IN}	ENB high and after V_{IN} > 6.0 V	3.5	13.5	28	V
VIN UVLO Start Voltage	$V_{IN(START)}$	V_{IN} rising, ENB high	3.1	–	3.45	V
VIN UVLO Stop Voltage	$V_{IN(STOP)}$	V_{IN} falling, ENB high	2.6	–	2.9	V
VIN UVLO Hysteresis	$V_{IN(HYS)}$	$V_{IN(START)} – V_{IN(STOP)}$	–	0.6	–	V
INPUT CURRENT						
Input Quiescent Current [1]	I_Q	V_{IN} = 13.5 V, ENB high	–	4	–	mA
Input Sleep Supply Current [1]	$I_{Q(SLEEP)}$	V_{IN} = 13.5 V, ENB low	–	1	10	μA
CHARGE PUMP						
Output Voltage	V_{REG}	ENB high, 5 mA ≤ I_{OUT} ≤ 50 mA, V_{IN} = 3.95 V	5.25	–	7	V
		ENB high, 5 mA ≤ I_{OUT} ≤ 33 mA, V_{IN} = 3.5 V	5.25	–	7	V
Switching Frequency	f_{SW}		–	325	–	kHz
Doubler to Pass Through Switchover	$V_{DOUBLER(H)}$	V_{IN} rising	7.8	–	8.65	V
Pass Through to Step Down Switchover	$V_{STEPDOWN(H)}$	V_{IN} rising	11.5	–	12.45	V
Step Down to Pass Through Switchover	$V_{STEPDOWN(L)}$	V_{IN} falling	10.5	–	11.7	V
Pass Through to Doubler Switchover	$V_{DOUBLER(L)}$	V_{IN} falling	6.9	–	7.5	V
5 V LINEAR REGULATOR						
Accuracy and Load Regulation	V_{OUT}	5 mA ≤ I_{OUT} ≤ 50 mA, 3.95 V ≤ V_{IN} ≤ 28 V	4.9	5.0	5.1	V
		5 mA ≤ I_{OUT} ≤ 33 mA, 3.5 V ≤ V_{IN} < 3.95 V	4.9	5.0	5.1	V
Output Capacitance Range [2]	C_{OUT}		3	–	10	μF
Startup Time [2]	t_{START}	C_{OUT} ≤ 4.7 μF, Load = 125 Ω ±5% (50 mA)	1.4	2.2	3.0	ms
LOGIN ENABLE (ENB) INPUT						
ENB Threshold	$V_{ENB(H)}$	V_{ENB} rising	–	–	2.0	V
	$V_{ENB(L)}$	V_{ENB} falling	0.8	–	–	V
ENB Resistance	R_{ENB}		–	100	–	kΩ
ENB Filter/Deglitch Time	$t_{d(EN,FILT)}$		10	15	20	μs

Continued on next page...

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.5 V ≤ V_{IN} ≤ 28 V, −40°C ≤ T_J ≤ 150°C, unless otherwise specified

OVERCURRENT PROTECTION (OCP)						
Current Limit [1]	I_{LIM}	V_{OUT} = 5 V	−60	−100	–140	mA
Foldback Current [1]	I_{FBK}	V_{OUT} = 0 V	−15	−30	−45	mA
THERMAL PROTECTION (TSD)						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	165	–	–	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	15	–	°C
VOUT OV/UV PROTECTIONS						
VOUT OV Thresholds	$V_{OV(H)}$	V_{OUT} rising, V_{IN} = 13.5 V	5.15	5.33	5.50	V
	$V_{OV(L)}$	V_{OUT} falling, V_{IN} = 13.5 V	–	5.30	–	V
VOUT OV Hysteresis	$V_{OV(HYS)}$	$V_{OV(H)} – V_{OV(L)}$, V_{IN} = 13.5 V	15	–	50	mV
VOUT UV Thresholds	$V_{UV(H)}$	V_{OUT} rising, V_{IN} = 13.5 V	–	4.71	–	V
	$V_{UV(L)}$	V_{OUT} falling, V_{IN} = 13.5 V	4.50	4.68	4.85	V
VOUT UV Hysteresis	$V_{UV(HYS)}$	$V_{UV(H)} – V_{UV(L)}$, V_{IN} = 13.5 V	15	–	50	mV
VOUT Output Disconnect Threshold	V_{DISC}	V_{OUT} rising, V_{IN} = 13.5 V	–	7.2	–	V
POK OUTPUTS						
POK Output Low Voltage	$V_{POK(L)}$	ENB high, V_{IN} ≥ 3.5 V, I_{POK} = 1 mA	–	150	400	mV
POK Leakage Current [1]	$I_{POK(LKG)}$	V_{POK} = 3.3 V	–	–	35	µA
OV and UV Filter/Deglitch Times [2]	$t_{d(FILT)}$	Applies to undervoltage of the V_{OUT} voltages	10	15	20	µs

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.

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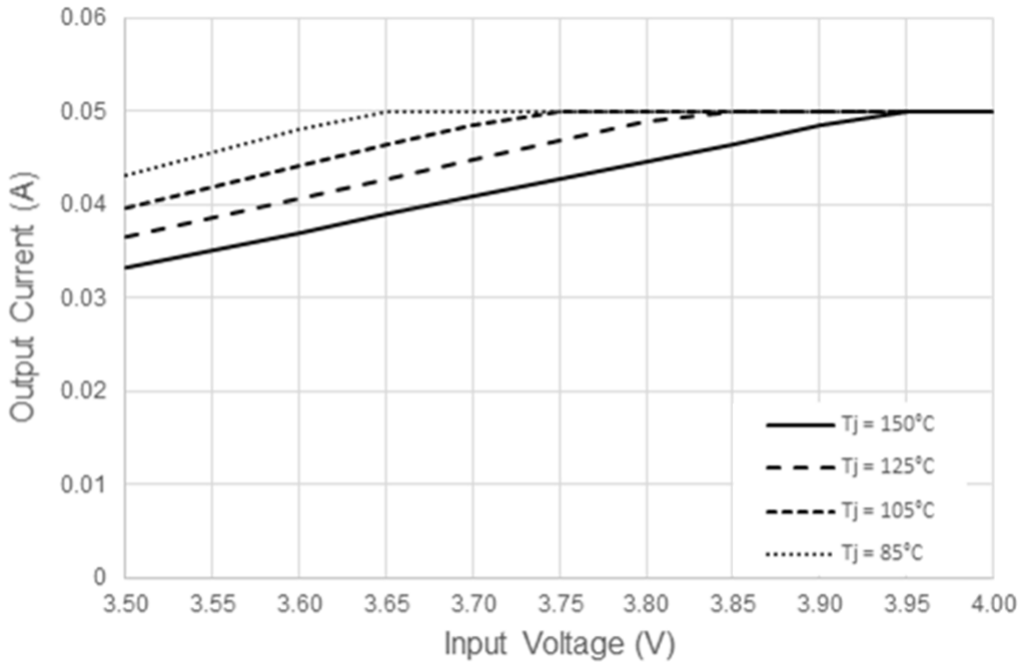

Figure 3: Output Current Derating versus Input Voltage

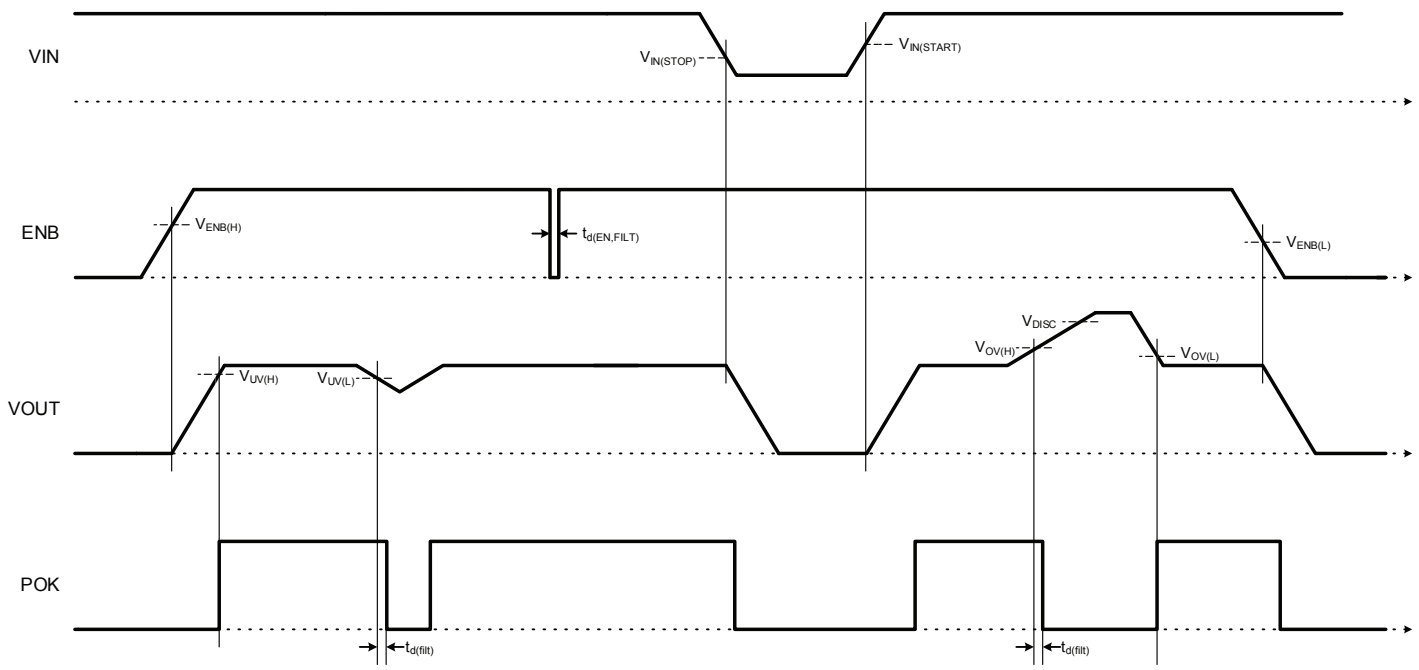

Figure 4: Timing Diagram (not to scale)

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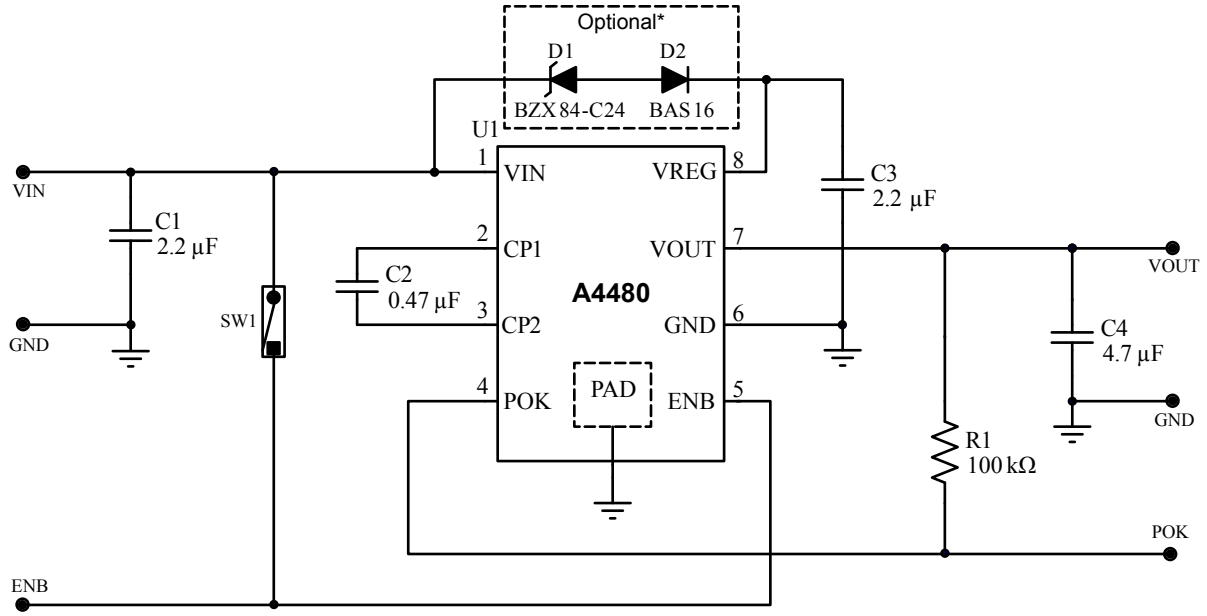

* Diodes D1 and D2 are only required if A4480 must be enabled when V_{IN} is greater than 28 V. If A4480 is already enabled before V_{IN} is greater than 28 V or if A4480 is off then operation to 40 V is possible without D1 and D2 diodes.

Figure 5: Typical Application Schematic

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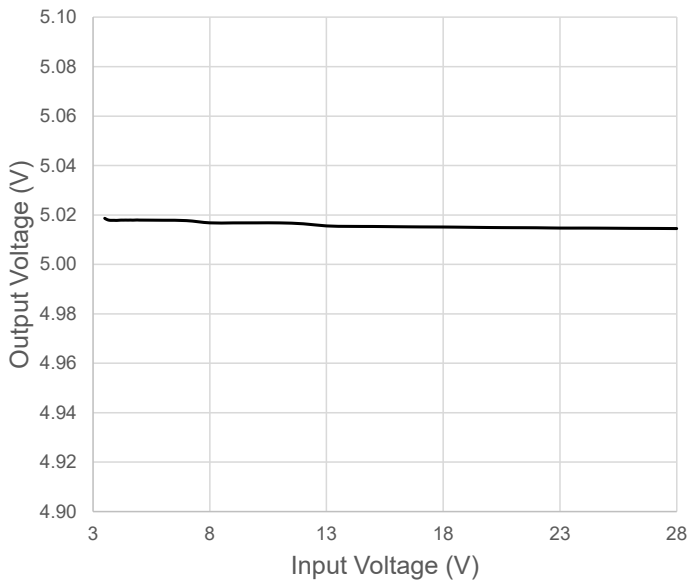
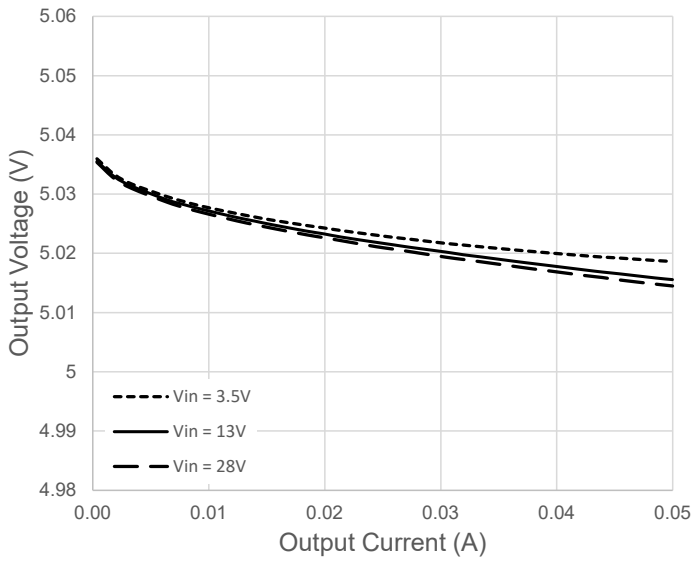
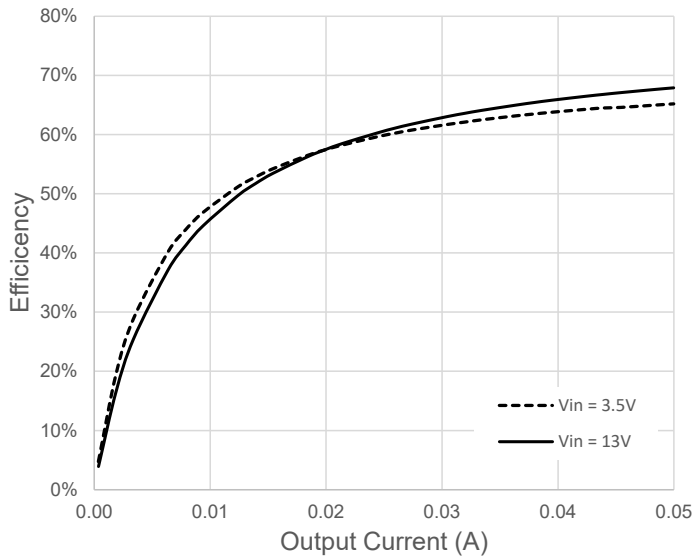
PERFORMANCE DATA



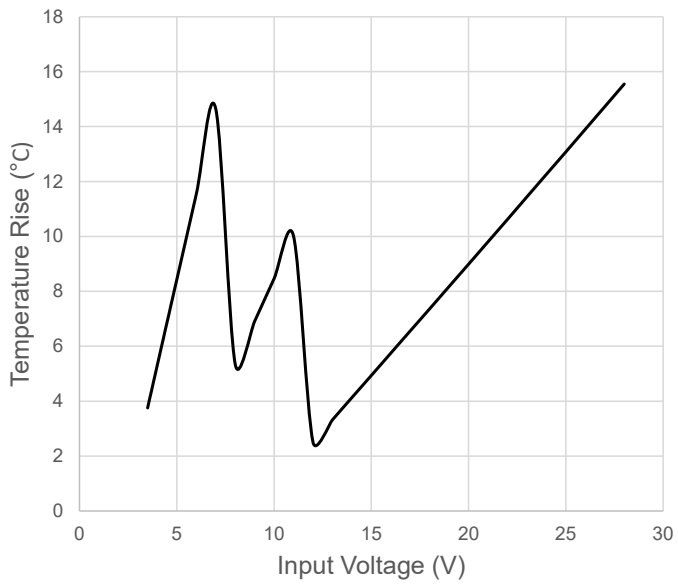
Line Regulation at 50 mA



Load Regulation



Typical Efficiency



Estimated Temperature Rise

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PCB LAYOUT GUIDELINES

The A4480 contains a switching charge pump circuit, so care must be taken when placing this part on the system PCB. The four decoupling capacitors (C1, C2, C3, and C4) must be placed as close to the A4480 as possible. Figure 6 below shows the recommend layout. The input capacitor C1 is placed next to pin 1 of the A4480 (U1). It connects directly to the pin 6 using copper on the top side of the PCB. The charge pump flying capacitor (C2) connects directly to pins 2 and 3 of A4480. The VREG capacitor connects to pins 8 and 6; top-side copper should only be used for this connection. The output capacitor (C4) connects to pins 7 and 8.

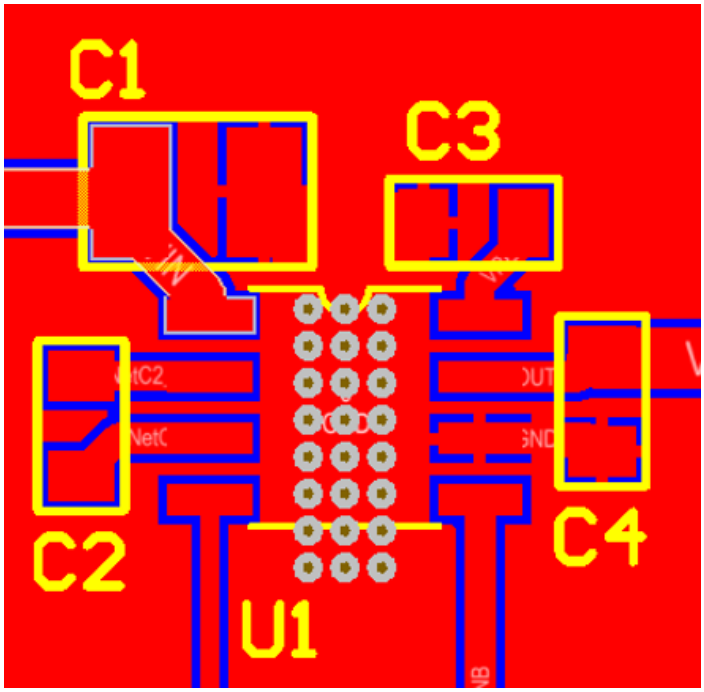

Figure 6: Typical Layout of the A4480

The vias under the A4480 are recommended for improved thermal performance. The ground copper plane should be a large as possible to reduce the junction to ambient thermal impedance of the A4480.

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000380, Rev. 2 and JEDEC MS-012BA)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

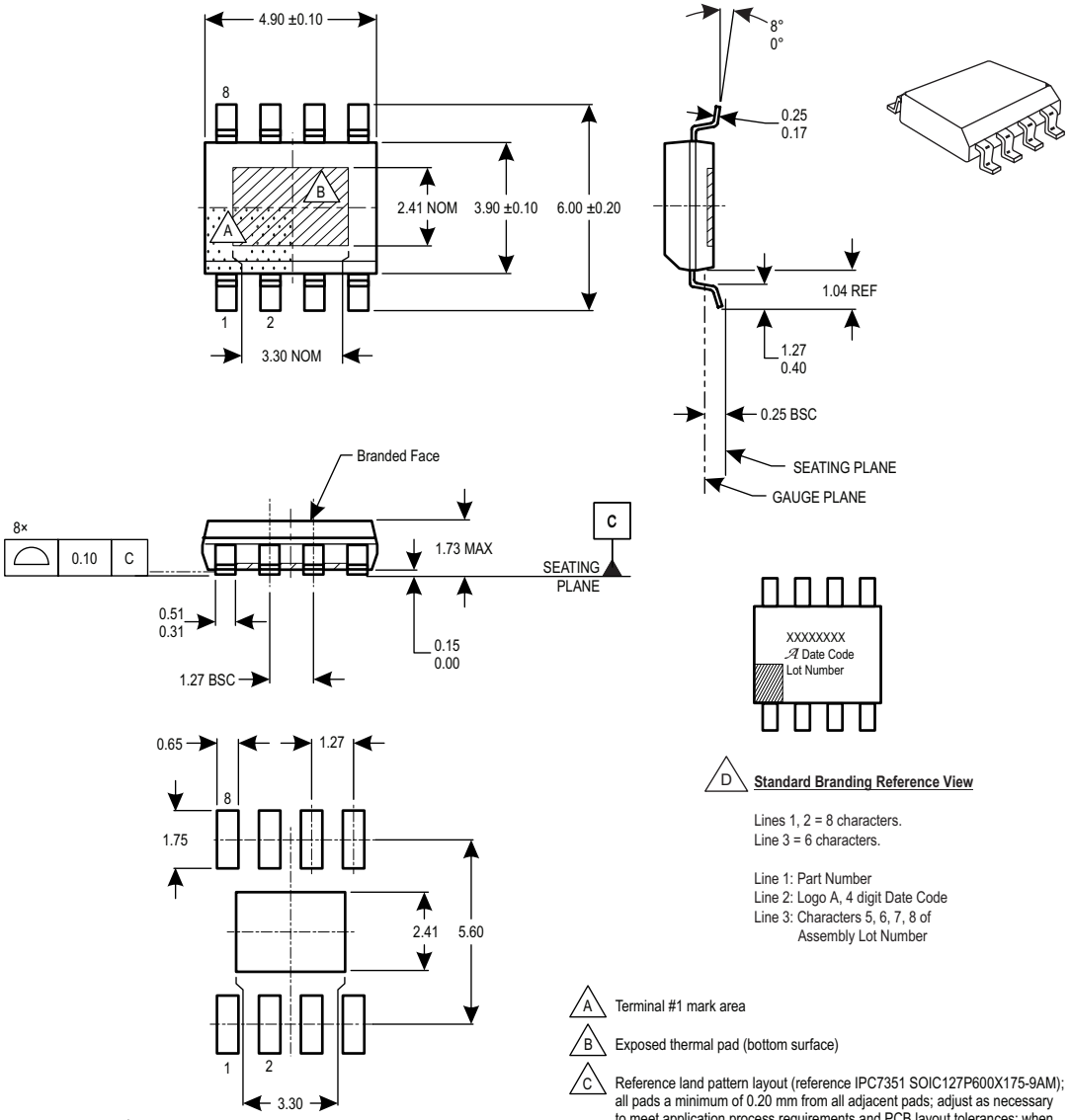

Figure 7: Package LJ, 8-Pin eSOIC

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Revision History

Number	Date	Description
–	June 1, 2017	Initial release
1	July 10, 2017	Updated Charge Pump Output Voltage test conditions (page 4), Accuracy and Load Regulation test conditions (page 4), and Figure 3 (page 6).
2	July 5, 2018	Minor editorial updates
3	July 12, 2019	Minor editorial updates
4	July 21, 2021	Updated Package Outline Drawing (page 10)
5	March 13, 2024	Updated product status to Last-Time Buy
6	September 13, 2024	Updated product status to Discontinued

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