SLC NAND FLASH and LPDDR 130-Ball MCP
MCP (Multi-Chip Package)

MX63UxGxxx

Key Features

NAND Flash Features:

- *Low Power Dissipation*
- *High Reliability*

Contents

1. MCP FEATURES

Operation Temperature

- -40°C to +85°C

Package

- 130-ball FBGA - 8.0mm x 9.0mm, 1.0mm (h), 0.65mm pitch

NAND Flash Features

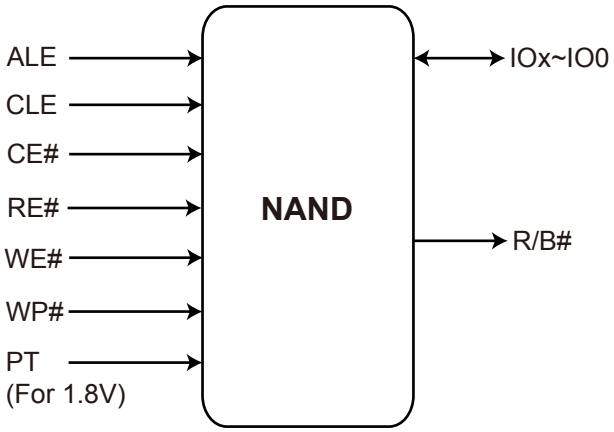
- **2G-bit SLC NAND Flash**
  - Bus: x8 / x16
  - Page size: (2048+64) byte for x8 bus, (1024+32) word for x16 bus
  - Block size: (128K+4K) byte for x8 bus, (64K+2K) word for x16 bus
  - Plane size: 1024-block/plane x 2
- **1G-bit SLC NAND Flash**
  - Bus: x8 / x16
  - Page size: (2048+64) byte for x8 bus, (1024+32) word for x16 bus
  - Block size: (128K+4K) byte for x8 bus, (64K+2K) word for x16 bus
  - Plane size: 1024-block/plane x 1
- **ONFI 1.0 compliant**
- **User Redundancy**
  - 64-byte attached to each page
- **Fast Read Access**
  - Latency of array to register: 25us
  - Sequential read: 25ns
- **Cache Read Support**
- **Page Program Operation**
  - Page program time: 320us (typ.)
- **Cache Program Support**
- **Block Erase Operation**
  - Block erase time: 1.0ms (typ.)
- **Single Voltage Operation:**
  - VCC: 1.7 ~ 1.95V
- **Low Power Dissipation**
  - Max. 30mA (1.8V) Active current (Read/Program/Erase)
- **Sleep Mode**
  - 50uA (Max) standby current
- **Unique ID Read support (ONFI)**
- **Secure OTP support**
- **Electronic Signature (5 Cycles)**
- **High Reliability**
  - Endurance: typical 100K cycles (with 4-bit ECC per (512+16) Byte)
  - Data Retention: 10 years
- **Wide Temperature Operating Range**
  - 40°C to +85°C

LPDDR DRAM Features

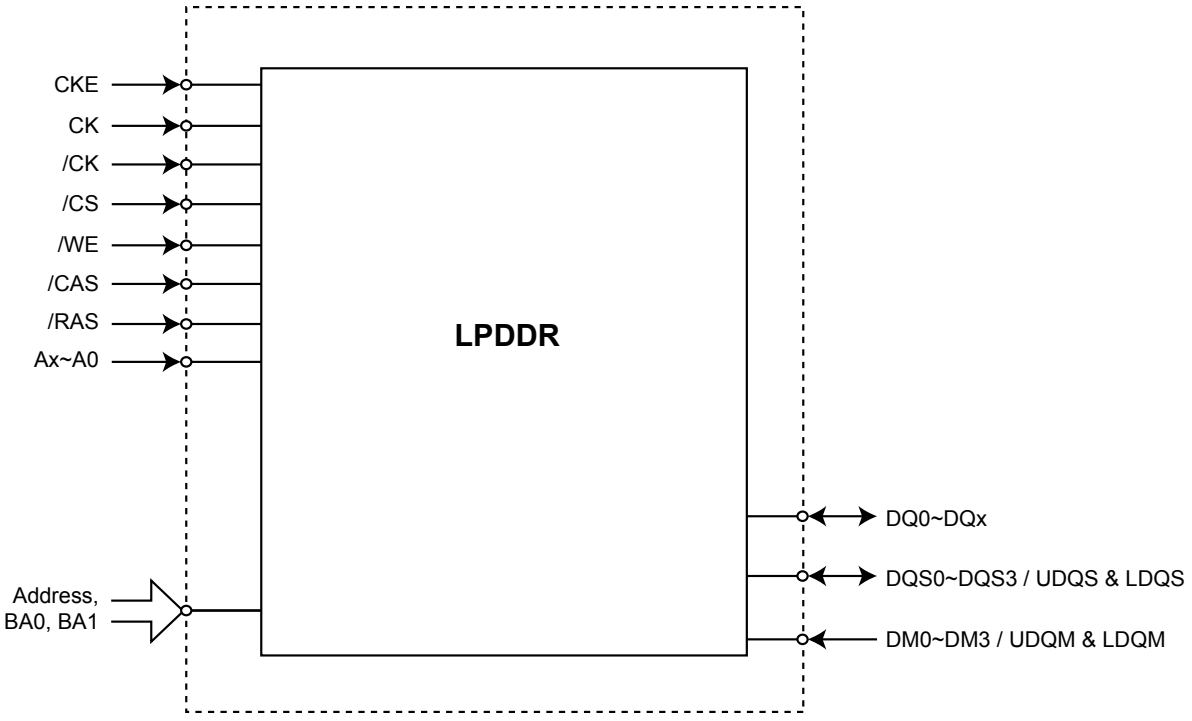
- VDD/VDDQ = 1.7~1.95V
- Data width: x16, x32
- Clock rate: 200MHz, 166MHz, 133MHz
- Partial Array Self-Refresh (PASR)
- Auto Temperature Compensated Self-Refresh (ATCSR)
- Power Down Mode
- Deep Power Down Mode (DPD Mode)
- Programmable output buffer driver strength
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Clock Stop capability during idle periods
- Auto Pre-charge option for each burst access
- Double data rate for data output
- Differential clock inputs (CK and /CK)
- Bidirectional, data strobe (DQS)
- /CAS Latency: 2 and 3
- Burst Length: 2, 4, 8 and 16
- Burst Type: Sequential or Interleave
- 64 ms Refresh period
- Interface: LVCMOS
- Operating Temperature Range
  - Industrial (-40°C to +85 °C)

2. BLOCK DIAGRAM

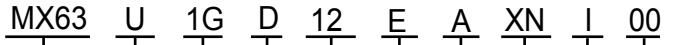
NAND



LPDDR



3. PART NAME DESCRIPTION



Reserved

Product Grade

I: Industrial

Package

XM: 162-Ball FBGA
XN: 130-Ball FBGA

MCP Combinations

Type	CE#	Combination
A	1,1	1 NAND; 1 LPDDR

LPDDR Configuration

Type		Bus	Vcc	Generation	Speed
A	DDR2	x16	1.7-1.95V	3	533MHz
B	DDR2	x32	1.7-1.95V	2	533MHz
C	DDR2	x32	1.7-1.95V	3	533MHz
E	DDR	x16	1.7-1.95V	5	200MHz
F	DDR	x32	1.7-1.95V	5	200MHz
J	DDR	x16	1.7-1.95V	5	200MHz
K	DDR	x32	1.7-1.95V	5	200MHz

LPDDR Density

256M = 56 2G = 2G
512M = 12 4G = 4G
1G = 1G 8G = 8G

NAND Configuration

Type	Bus	Number of ECC-bit	Generation
A	x8	8	1st
B	x16	8	1st
C	x8	4	1st
D	x16	4	1st

NAND Density

512M = 12 8G = 8G
1G = 1G 16G = AG
2G = 2G 32G = BG
4G = 4G 64G = CG

NAND Voltage: 1.8V

Product Family

MX63U : NAND + LPDRAM MCP

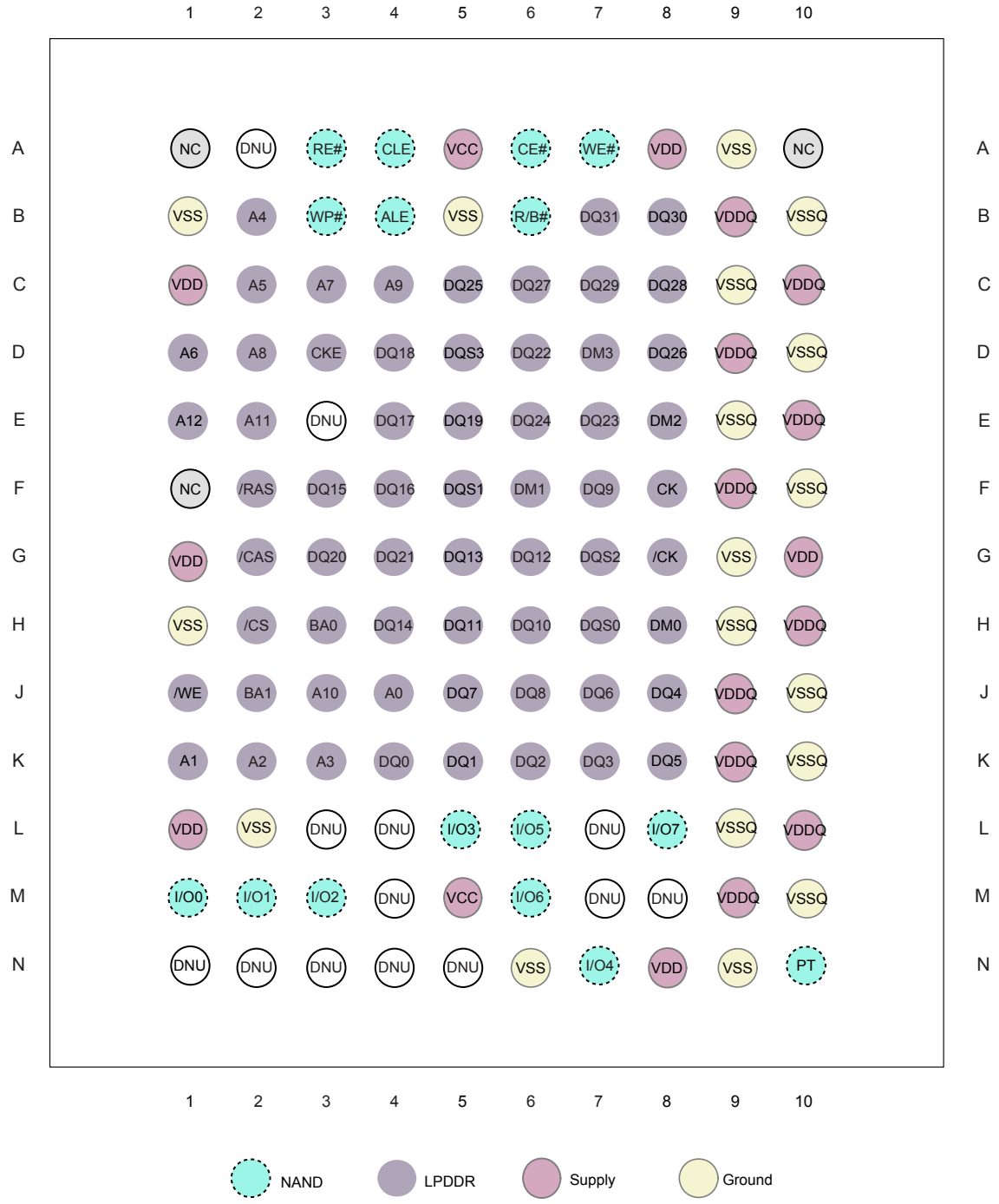
4. Product Selection Guide

Device	NAND Flash	Mobile DRAM	Package Type
MX63U1GD12EAXNI00	1Gb, x16, 1.8V, 4-bit ECC	512Mb, LPDDR, x16, 1.8V	130 Ball BGA
MX63U1GC12FAXNI00	1Gb, x8, 1.8V, 4-bit ECC	512Mb, LPDDR, x32, 1.8V	130 Ball BGA
MX63U2GC1GKAXNI00 *	2Gb, x8, 1.8V, 4-bit ECC	1Gb, LPDDR, x32, 1.8V	130 Ball BGA
MX63U2GD1GJAXNI00 *	2Gb, x16, 1.8V, 4-bit ECC	1Gb, LPDDR, x16, 1.8V	130 Ball BGA

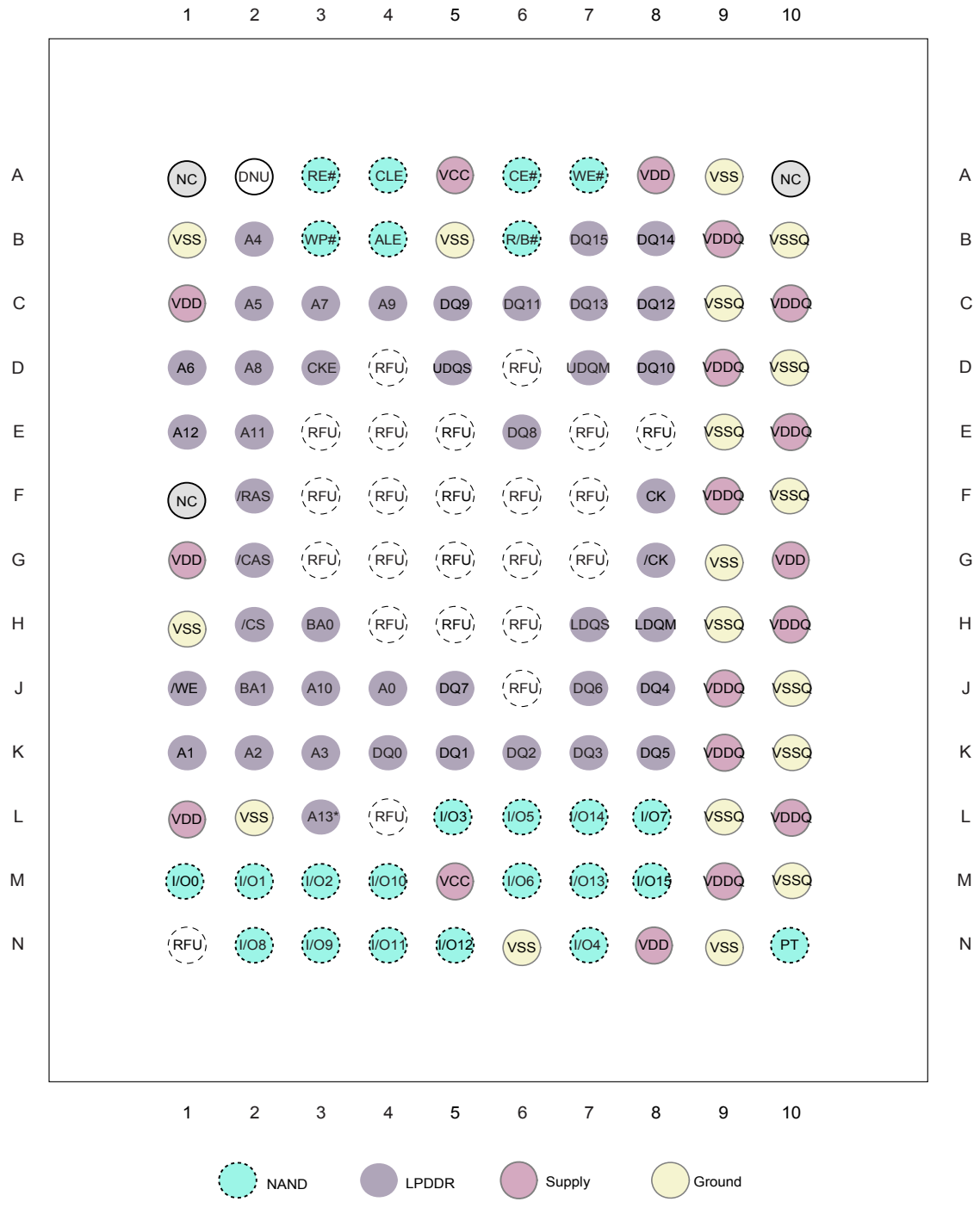
Notes:
1. For other NAND/ LPDDR I/O combination, please cotact Macronix Representative.
2. * Advanced Information

5. PIN CONFIGURATIONS

130-Ball, BGA (NAND x8; LPDDR x32)



130-Ball, BGA (NAND x8/x16; LPDDR x16)



*Note: A13 is only for 1Gb LPDDR1. It is DNU pin in Other density.

6. PIN DESCRIPTION

LPDDR x32

SYMBOL	DESCRIPTION	NAND Flash 2Gb (x8) 1Gb (x8)	LPDDR 1Gb (32Mb x32) 512Mb (16Mbx32)
I/O0 ~ I/O7	Data Input / Output	V	
CLE	Command Latch Enable	V	
ALE	Address Latch Enable	V	
CE#	Chip Enable	V	
WE#	Write Enable	V	
RE#	Read Enable	V	
WP#	Write Protect	V	
R/B#	Ready / Busy Out	V	
VCC	Supply Voltage	V	
VSS	Ground	V	V
PT	Chip Protection Enable	V	
CK, /CK	Differential Clock Input		V
CKE	Clock Enable		V
/CS	Chip Select		V
/RAS, /CAS, /WE	Command Input		V
DM0 ~ DM3	Input Data Mask		V
DQ0 ~ DQ31	Data I/O		V
DQS0 ~ DQS3	Data Strobe Pin		V
BA0, BA1	Bank Address Input		V
Ax ~ A0	Address Input		V
VDDQ	DQ Power Supply		V
VSSQ	DQ Ground		V
VDD	Power Supply		V
NC	No Connection		V
DNU *	Do Not Use	V	V

* : DNU pin must keep floating.

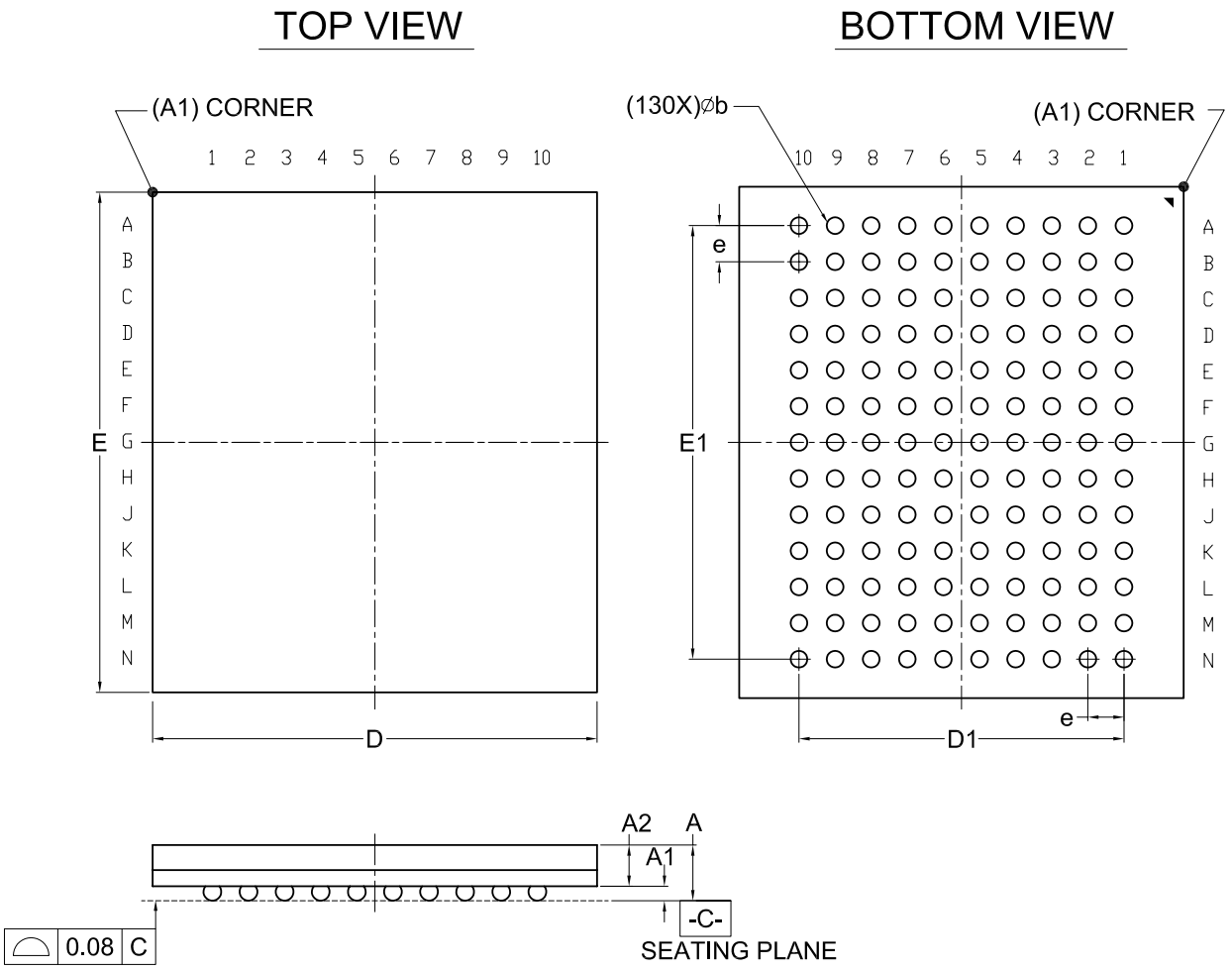
LPDDR x16

SYMBOL	DESCRIPTION	NAND Flash 2Gb (x16) 1Gb (x16)	LPDDR 1Gb (64Mb x16) 512Mb (32Mb x16)
I/O0 ~ I/Ox	Data Input / Output	V	
CLE	Command Latch Enable	V	
ALE	Address Latch Enable	V	
CE#	Chip Enable	V	
WE#	Write Enable	V	
RE#	Read Enable	V	
WP#	Write Protect	V	
R/B#	Ready / Busy Out	V	
VCC	Supply Voltage	V	
VSS	Ground	V	V
PT	Chip Protection Enable	V	
CK, /CK	Differential Clock Input		V
CKE	Clock Enable		V
/CS	Chip Select		V
/RAS, /CAS, /WE	Command Input		V
UDQM & LDQM	Input Data Mask		V
DQ0 ~ DQx	Data I/O		V
UDQS & LDQS	Data Strobe Pin		V
BA0, BA1	Bank Address Input		V
Ax ~ A0	Address Input		V
VDDQ	DQ Power Supply		V
VSSQ	DQ Ground		V
VDD	Power Supply		V
NC	No Connection		V
DNU *	Do Not Use	V	V

* : DNU pin must keep floating.

7. PACKAGE INFORMATION

Title: **Package Outline for CSP 130BALL(8X9X1.0MM,BALL PITCH 0.65MM,BALL DIAMETER 0.3MM)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.16	0.61	0.25	7.90	---	8.90	---	---
	Nom.	---	0.21	0.67	0.30	8.00	5.85	9.00	7.80	0.65
	Max.	1.00	0.27	0.73	0.35	8.10	---	9.10	---	---
Inch	Min.	---	0.006	0.024	0.010	0.311	---	0.350	---	---
	Nom.	---	0.008	0.026	0.012	0.315	0.230	0.354	0.307	0.026
	Max.	0.039	0.011	0.029	0.014	0.319	---	0.358	---	---

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4272	2	MO-207			

8. REVISION HISTORY

Revision No.	Description	Page	Date
0.01	1. Removed MX63U2GA1GEAXNI00 ; Added MX63U1GD12EAXNI00/MX63U1GC12FAXNI00/ MX63U2GC1GKAXNI00/MX63U2GD1GJAXNI00	All	SEP/25/2014
	2. Modified Package Information	P10	
1.0	1. Removed document status "ADVANCED INFORMATION"	All	MAR/13/2015
	2. Content modification	P3,9-10	
	3. Updated the PART NAME DESCRIPTION	P5	
	4. Re-arrange the order of pin description tables	P9-10	
	5. Added note in PIN CONFIGURATIONS - 130-Ball, BGA (NAND x8/x16; LPDDR x16)	P8	

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