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Kind regards,

Team Nexperia



PSMN3R2-25YLC

N-channel 25 V 3.4 mΩ logic level MOSFET in LPAK using NextPower technology

Rev. 01 — 2 May 2011

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD and QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

1.4 Quick reference data

Table 1. Quick reference data

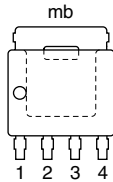
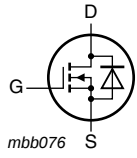
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	-	25	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1 [1]	-	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	79	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; see Figure 12	-	3.7	4.45	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 12	-	2.85	3.4	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 4.5 V; I _D = 25 A; V _{DS} = 12 V; see Figure 14 ; see Figure 15	-	4	-	nC
Q _{G(tot)}	total gate charge		-	14	-	nC



[1] Continuous current is limited by package

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		
			SOT669 (LPAK; Power-SO8)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R2-25YLC	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PSMN3R2-25YLC	3C225L

[1] % = placeholder for manufacturing site code

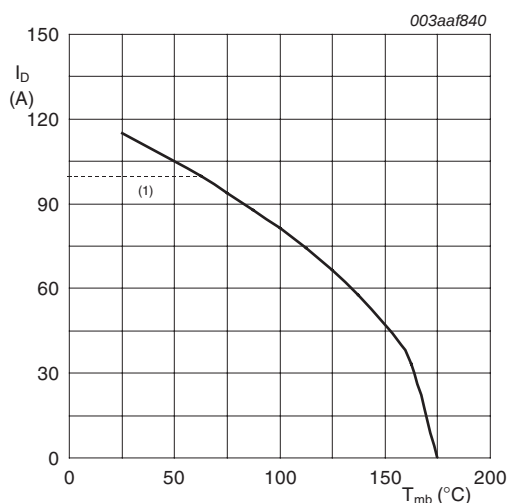
5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

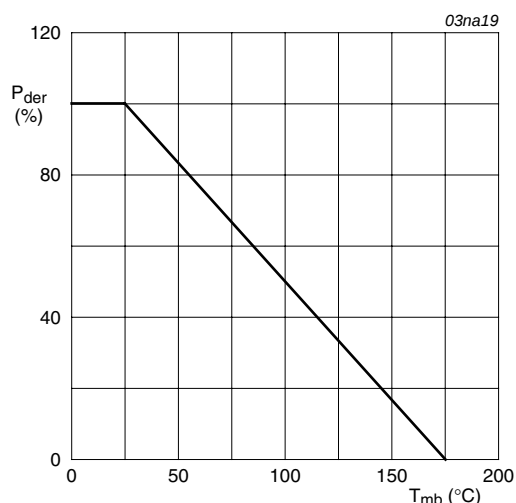
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ^[1]	-	100	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	81	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 4	-	462	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	79	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
V_{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	340	-	V
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	72	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	462	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 25\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$; see Figure 3	-	34	mJ

[1] Continuous current is limited by package



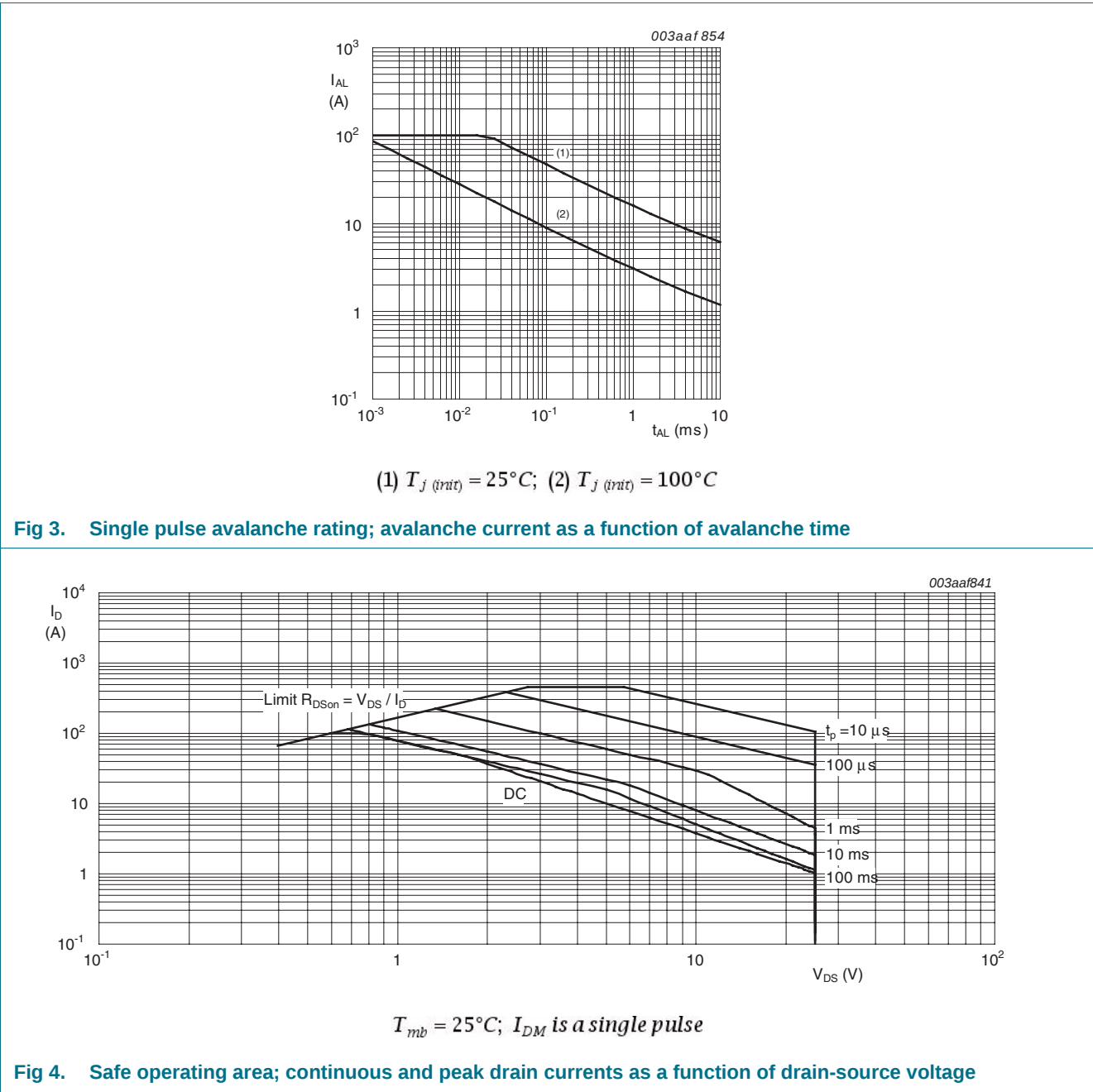
$V_{GS} \geq 10\text{ V}$; (1) Capped at 100A due to package

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

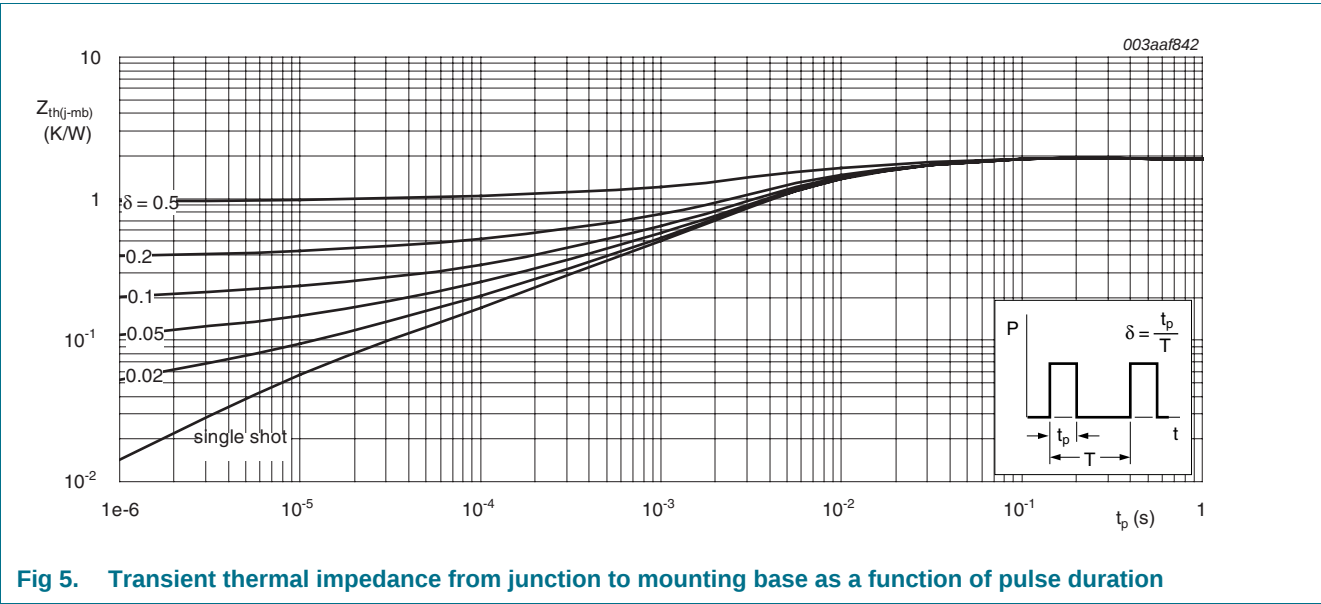
Fig 2. Normalized total power dissipation as a function of mounting base temperature



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	1.72	1.9	K/W



7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	25	-	-	V
		$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = -55\ ^\circ\text{C}$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ\text{C}$; see Figure 10 ; see Figure 11	1.05	1.54	1.95	V
		$I_D = 10\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 150\ ^\circ\text{C}$	0.5	-	-	V
		$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = -55\ ^\circ\text{C}$	-	-	2.25	V
I_{DSS}	drain leakage current	$V_{DS} = 25\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 25\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 150\ ^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -16\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}$; $I_D = 25\ \text{A}$; $T_j = 25\ ^\circ\text{C}$; see Figure 12	-	3.7	4.45	mΩ
		$V_{GS} = 4.5\ \text{V}$; $I_D = 25\ \text{A}$; $T_j = 150\ ^\circ\text{C}$; see Figure 12 ; see Figure 13	-	-	7.2	mΩ
		$V_{GS} = 10\ \text{V}$; $I_D = 25\ \text{A}$; $T_j = 25\ ^\circ\text{C}$; see Figure 12	-	2.85	3.4	mΩ
		$V_{GS} = 10\ \text{V}$; $I_D = 25\ \text{A}$; $T_j = 150\ ^\circ\text{C}$; see Figure 12 ; see Figure 13	-	-	5.5	mΩ
R_G	gate resistance	$f = 1\ \text{MHz}$	-	1.8	3.6	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 10\ \text{V}$; see Figure 14 ; see Figure 15	-	30	-	nC
		$I_D = 25\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 14 ; see Figure 15	-	14	-	nC
		$I_D = 0\ \text{A}$; $V_{DS} = 0\ \text{V}$; $V_{GS} = 10\ \text{V}$	-	26	-	nC
Q_{GS}	gate-source charge	$I_D = 25\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 14 ; see Figure 15	-	4.5	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	3.2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.3	-	nC
Q_{GD}	gate-drain charge		-	4	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\ \text{A}$; $V_{DS} = 12\ \text{V}$; see Figure 14 ; see Figure 15	-	2.48	-	V
C_{iss}	input capacitance	$V_{DS} = 12\ \text{V}$; $V_{GS} = 0\ \text{V}$; $f = 1\ \text{MHz}$; $T_j = 25\ ^\circ\text{C}$; see Figure 16	-	1781	-	pF
C_{oss}	output capacitance		-	462	-	pF
C_{rss}	reverse transfer capacitance		-	152	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\ \text{V}$; $R_L = 0.5\ \Omega$; $V_{GS} = 4.5\ \text{V}$; $R_{G(ext)} = 4.7\ \Omega$	-	19	-	ns
t_r	rise time		-	19	-	ns
$t_{d(off)}$	turn-off delay time		-	30	-	ns
t_f	fall time		-	11	-	ns

Table 7. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 12\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$	-	9.6	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17	-	0.8	1.1	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A/}\mu\text{s}$;	-	29	-	ns
Q_r	recovered charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 12\text{ V}$	-	18	-	nC
t_a	reverse recovery rise time	$V_{GS} = 0\text{ V}$; $I_S = 25\text{ A}$;	-	17	-	ns
t_b	reverse recovery fall time	$dI_S/dt = -100\text{ A/}\mu\text{s}$; $V_{DS} = 12\text{ V}$; see Figure 18	-	12	-	ns

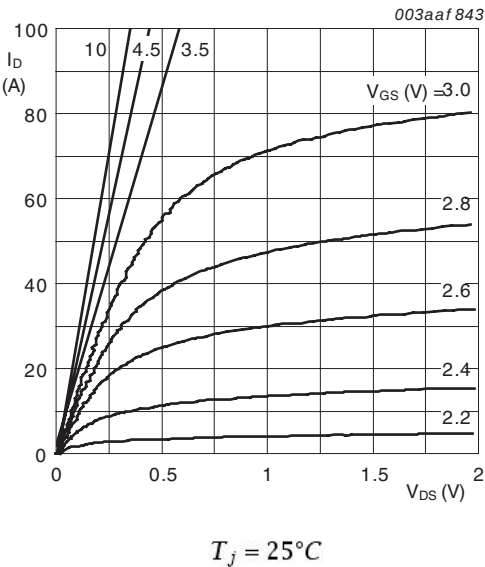


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

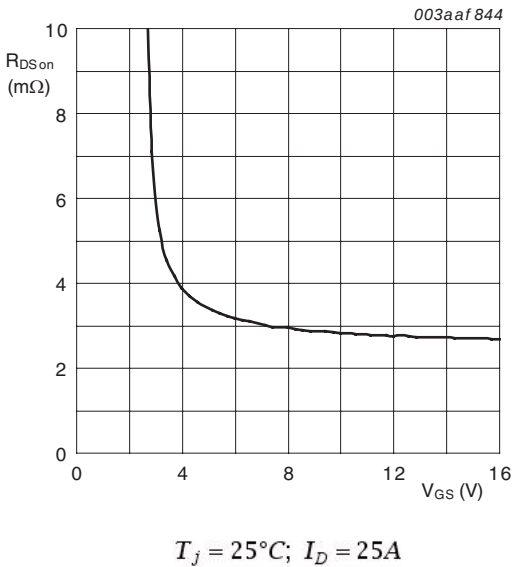


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

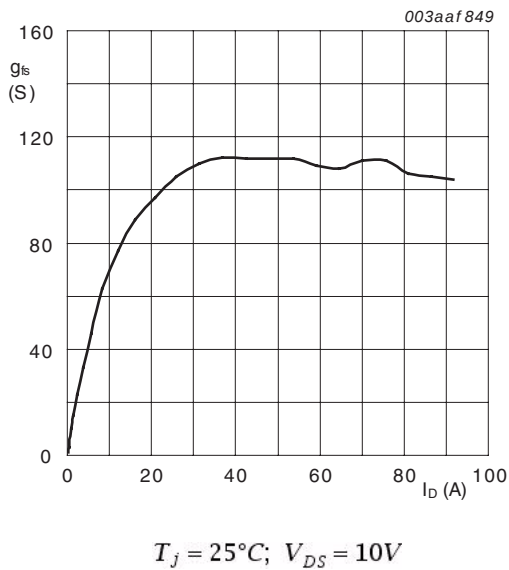


Fig 8. Forward transconductance as a function of drain current; typical values

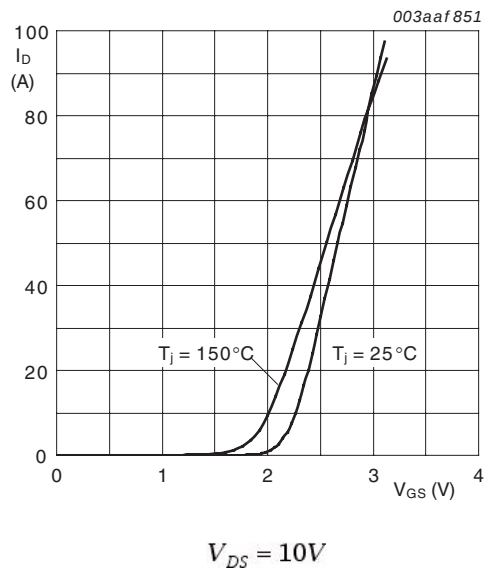


Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

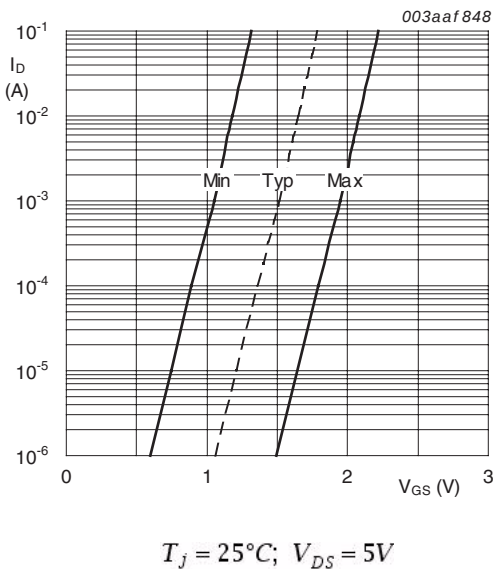


Fig 10. Sub-threshold drain current as a function of gate-source voltage

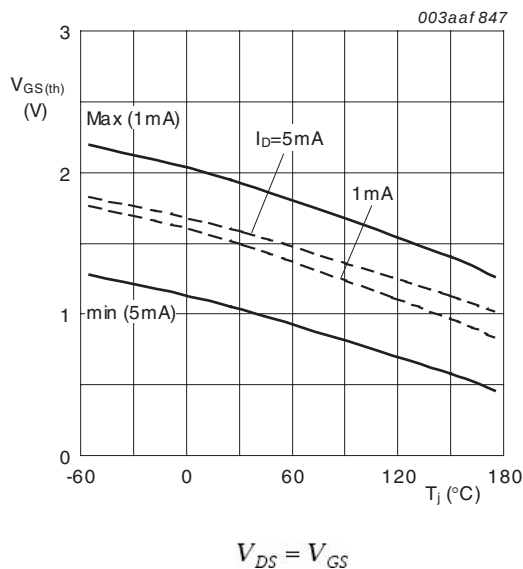


Fig 11. Gate-source threshold voltage as a function of junction temperature

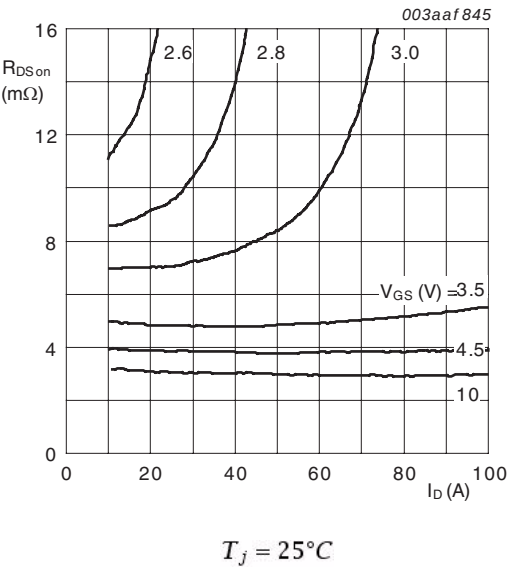


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

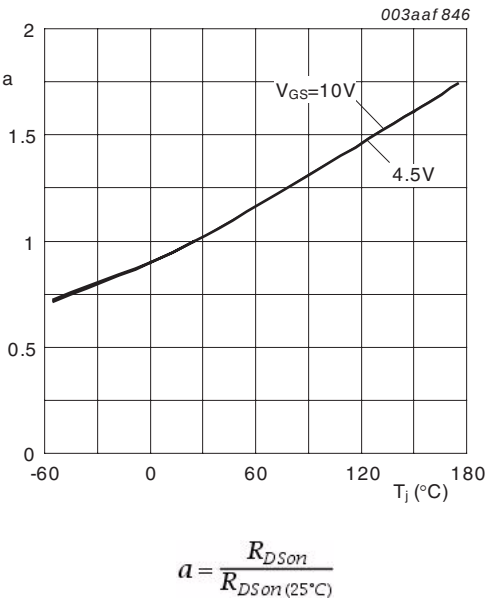


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

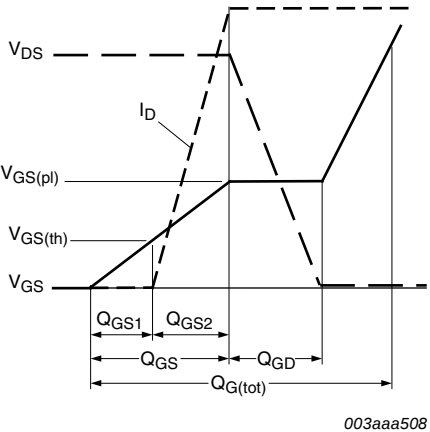


Fig 14. Gate charge waveform definitions

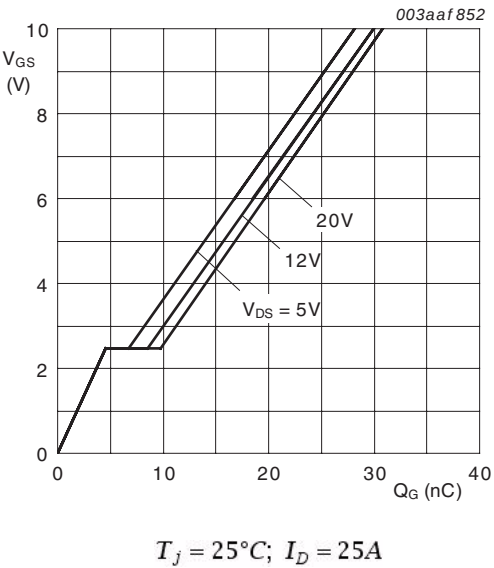


Fig 15. Gate-source voltage as a function of gate charge; typical values

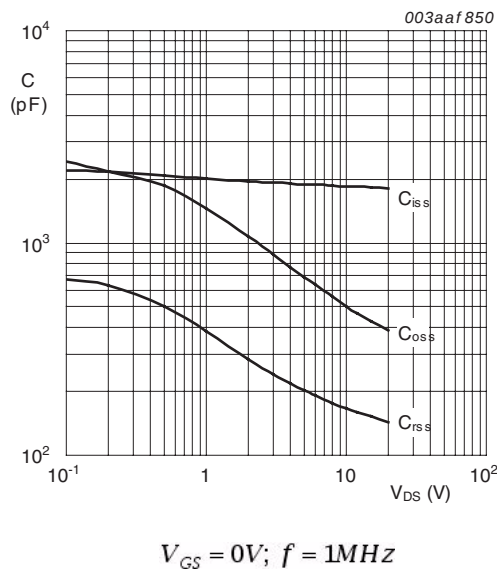


Fig 16. Input, output and reverse transfer capacitance as a function of drain-source voltage; typical values

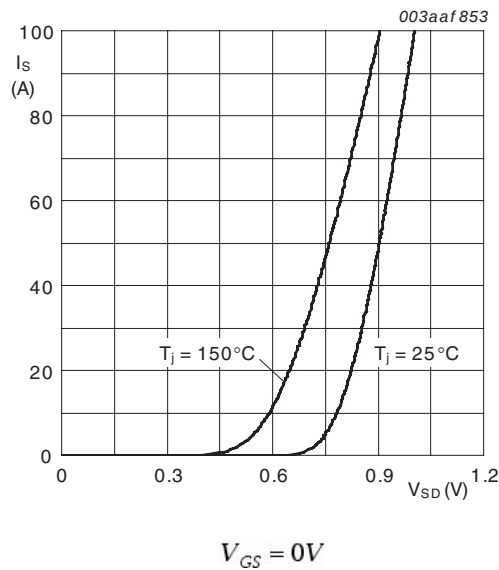


Fig 17. Source current as a function of source-drain voltage; typical values

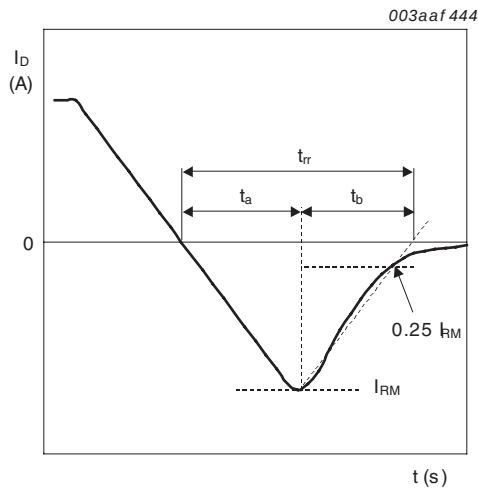


Fig 18. Reverse recovery timing definition

8. Package outline

Plastic single-ended surface-mounted package (LPAK; Power-SO8); 4 leads SOT669

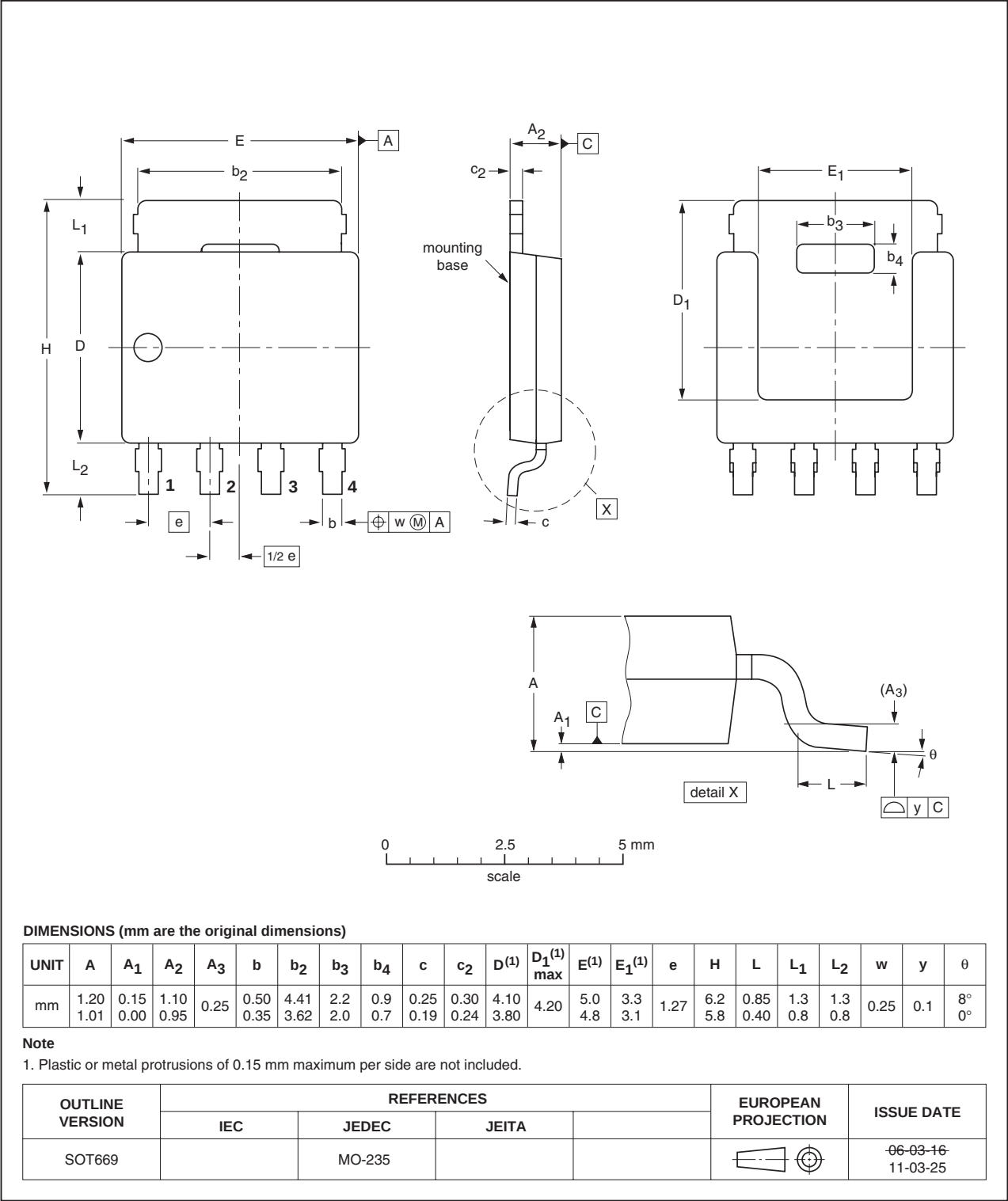


Fig 19. Package outline SOT669 (LPAK; Power-SO8)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN3R2-25YLC v.1	20110502	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status ^[1] ^[2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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