MPM3620

24V Input 2A Module Synchronous Step-Down Converter with Integrated Inductor

The Future of Analog IC Technology

DESCRIPTION

The MPM3620 is a synchronous rectified, step-down module converter with built-in power MOSFETs, inductor, and two capacitors. It offers a compact solution that requires only 5 external components to achieve a 2A continuous output current with excellent load and line regulation over a wide input-supply range. Also, it provides fast load transient response. An external AAM pin provides selectable power-save mode and forced PWM mode.

Full protection features include over-current protection(OCP) and thermal shut down(TSD).

MPM3620 eliminates design and manufacturing risks while dramatically improving time-to-market.

The MPM3620 is available in a space-saving QFN-20 (3mmx5mmx1.6mm) package.

FEATURES

- 4.5V-to-24V Operating Input Range
- 2A Continuous Load Current
- 200μA Low Quiescent Current
- 90mΩ/40mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Integrated Inductor
- Integrated V_{CC} and Bootstrap Capacitors
- External AAM for Power-Save Mode Programming
- Over-Current Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in QFN-20 (3mmx5mmx1.6mm) Package
- Total solution size 6.7mmx6.3mm

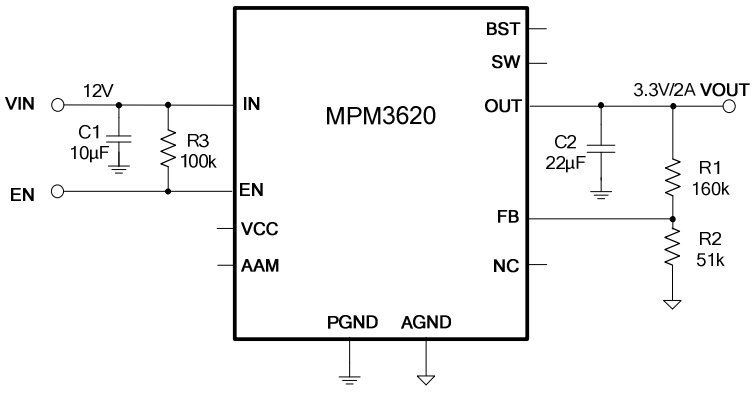
APPLICATIONS

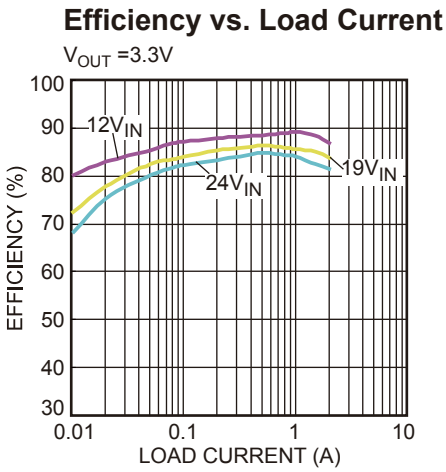
- Industrial Controls
- Medical and Imaging Equipment
- Telecom and Networking Applications
- LDO Replacement
- Space and Resource-limited Applications

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3620GQV	QFN-20 (3mmx5mmx1.6mm)	*See Below*

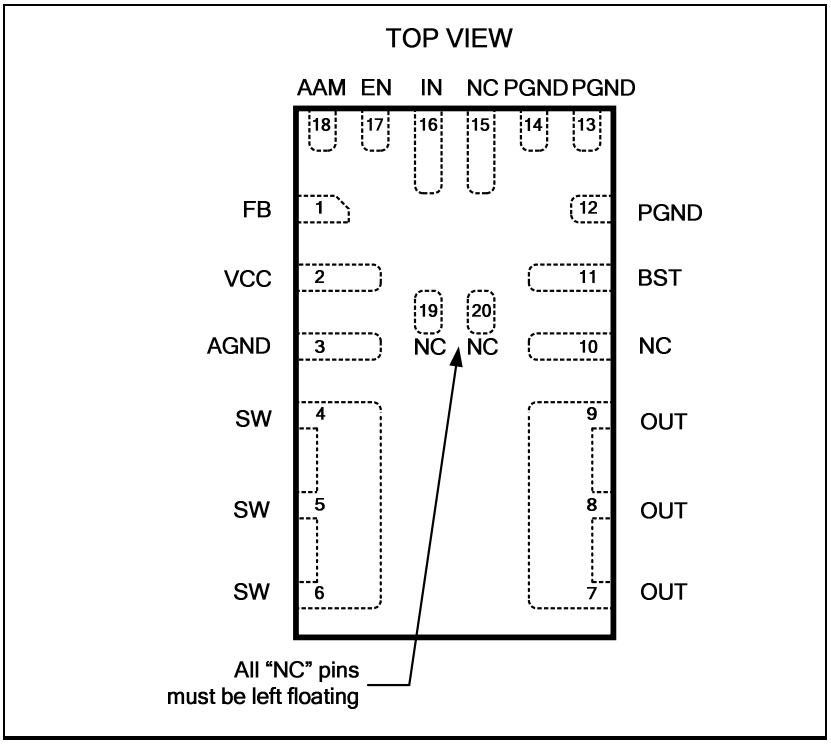
* For Tape & Reel, add suffix –Z (e.g. MPM3620GQV–Z);

TOP MARKING

MPYW
3620
LLL
M

MP: MPS prefix:
Y: year code;
W: week code:
3620 first four digits of the part number;
LLL: lot number;
M: module

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 28V
V_{OUT} ..... -0.3V to 28V
V_{SW} .....
-0.3V (-5V for <10ns) to 28V (30V for <10ns)
V_{BST} ..... V_{SW}+6V
All Other Pins..... -0.3V to 6V (2)
Continuous Power Dissipation (T_A = +25°C) (3)
.....2.7W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 4.5V to 24V
Output Voltage V_{OUT}.....0.8V to V_{IN}*D_{MAX} (5)
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-20 (3mmx5mmx1.6mm)	46	10 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For additional details on EN pin's ABS MAX rating, please refer to the "Enable Control" section on page 14.
3) The maximum power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the converter to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) In practical design, the minimum V_{OUT} is limited by the minimum on-time. To allow a margin, a 50ns on-time is recommended for calculating. To set the output voltage above 5.5V, please refer to the application information on page 17.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C to +125°C [7], typical value is tested at T_J=+25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V,T_J=25°C			1	μA
Supply Current (Quiescent)	I_q	V_{FB} = 1V, V_{AAM}=0.5V		0.2		mA
		V_{FB} = 1V, V_{AAM}=5V		0.7		
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		90		mΩ
LS Switch-On Resistance	LS_{RDS-ON}	V_{CC} =5V		40		mΩ
Integrated Inductor Inductance[8]	L			1		μH
Inductor DC Resistance	L_{DCR}	T_J=+25°C	25	45	65	mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
Current Limit [8]	I_{LIMIT}	Under 40% Duty Cycle	3.8	4.8		A
Oscillator Frequency	f_{SW}	V_{FB}=0.75V, T_J=+25°C	1600	2000	2400	kHz
		V_{FB}=0.75V,T_J=-40°C to +125°C	1500	2000	2500	kHz
Fold-Back Frequency	f_{FB}	V_{FB}<400mV		0.3		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB}=700mV	77			%
Minimum On Time [8]	t_{ON_MIN}			35		ns
Feedback Voltage	V_{FB}	T_J=+25°C	786	798	810	mV
		T_J=-40°C to +125°C	782	798	814	mV
Feedback Current	I_{FB}	V_{FB}=820mV		10	50	nA
AAM Source Current	I_{AAM}	T_J=+25°C	5.6	6.2	6.8	μA
		T_J=-40°C to +125°C	4.3	6.2	7.9	μA
EN Rising Threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN Falling Threshold	$V_{EN_FALLING}$		1.05	1.25	1.45	V
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
VIN Under-Voltage Lockout Threshold—Rising	$INUV_{Vth}$		3.65	3.9	4.15	V
VIN Under-Voltage Lockout Threshold—Hysteresis	$INUV_{HYS}$			650		mV
VCC Regulator	V_{CC}			5		V
VCC Load Regulation		I_{CC}=5mA		1.5		%
Soft-Start Time	t_{SS}	V_{OUT} from 10% to 90%		1.5		ms
Thermal Shutdown [8]				150		°C
Thermal Hysteresis [8]				20		°C

Notes:

7) Not tested in production; guaranteed by over-temperature correlation.
8) Guaranteed by characterization test.

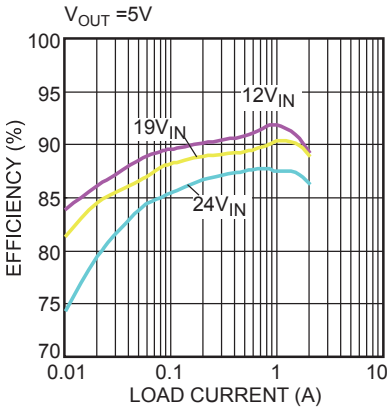
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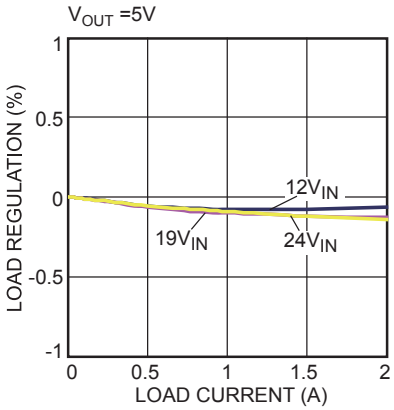
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

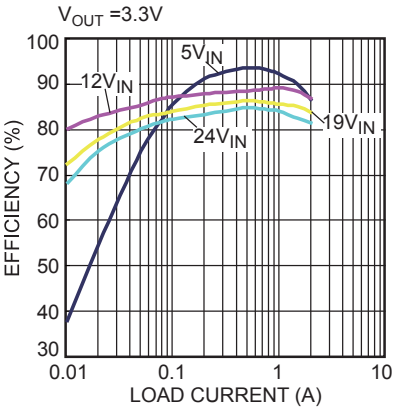
Efficiency vs. Load Current



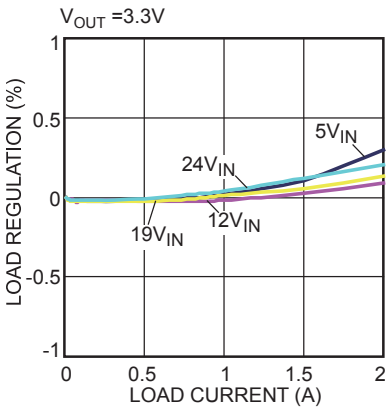
Load Regulation



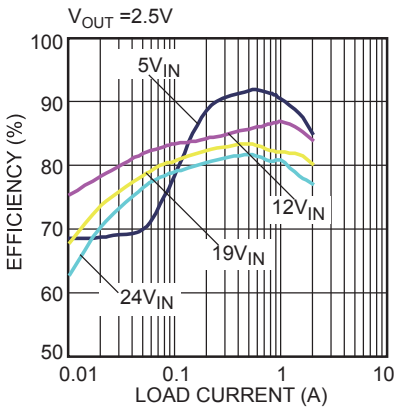
Efficiency vs. Load Current



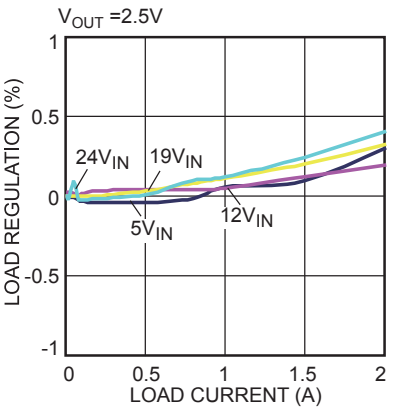
Load Regulation



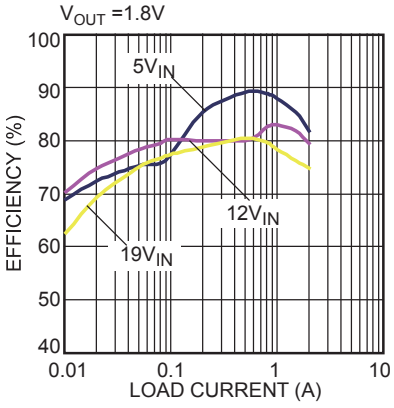
Efficiency vs. Load Current



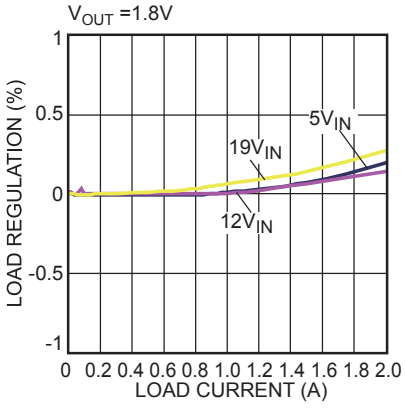
Load Regulation



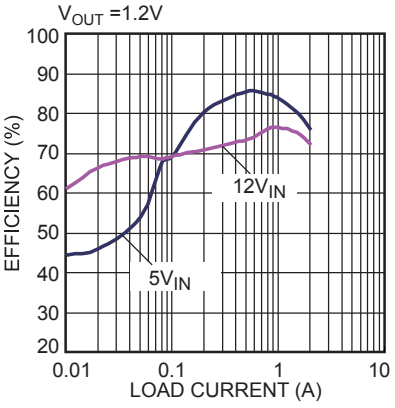
Efficiency vs. Load Current



Load Regulation



Efficiency vs. Load Current



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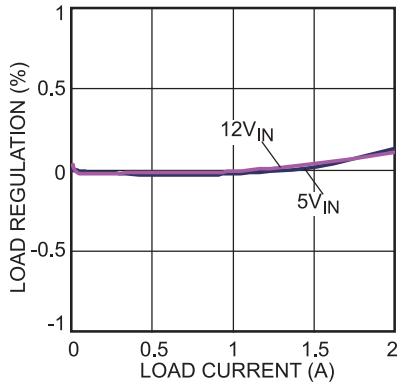
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TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

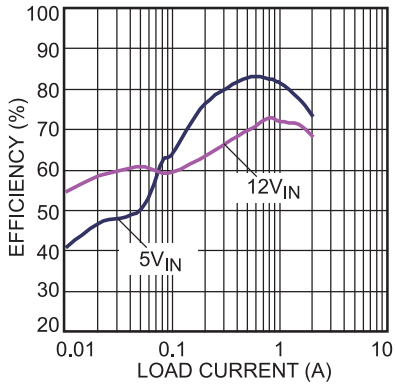
Load Regulation

V_{OUT} = 1.2V



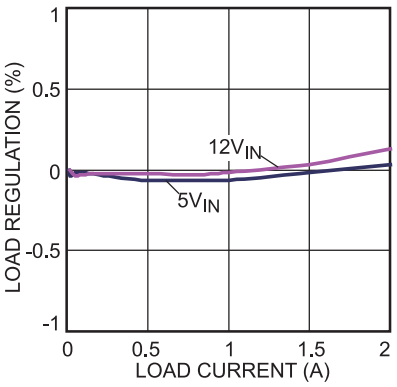
Efficiency vs. Load Current

V_{OUT} = 1V



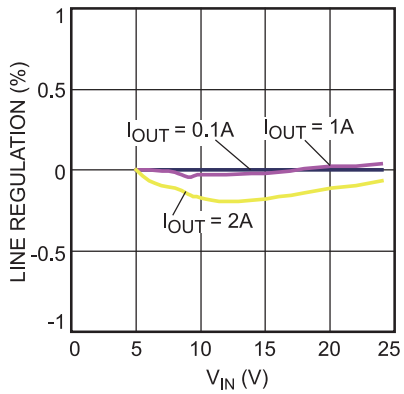
Load Regulation

V_{OUT} = 1V

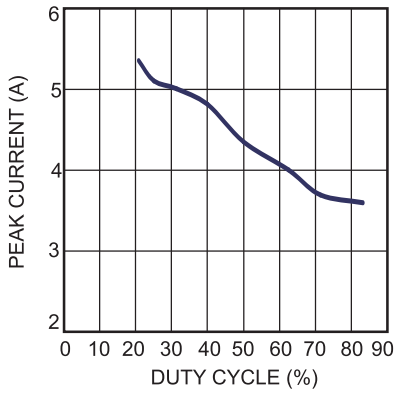


Line Regulation

V_{OUT} = 3.3V

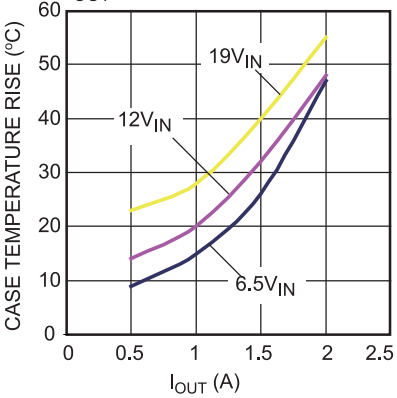


Inductor Peak-Current Limit vs. Duty Cycle



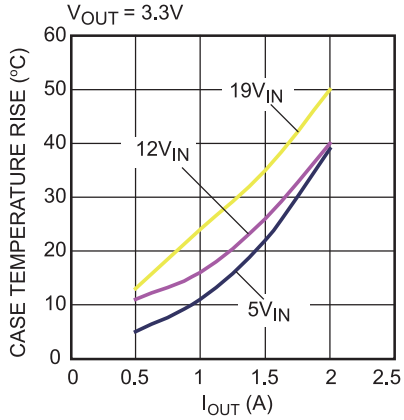
Case Temperature Rise vs. I_{OUT}

V_{OUT} = 5V



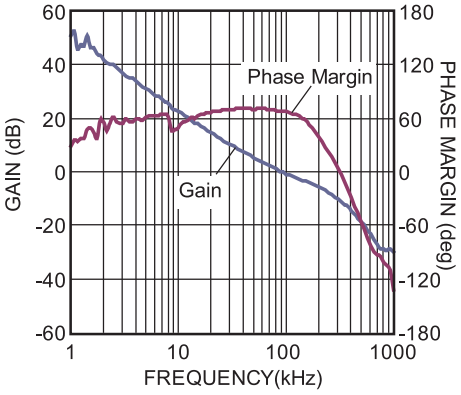
Case Temperature Rise vs. I_{OUT}

V_{OUT} = 3.3V

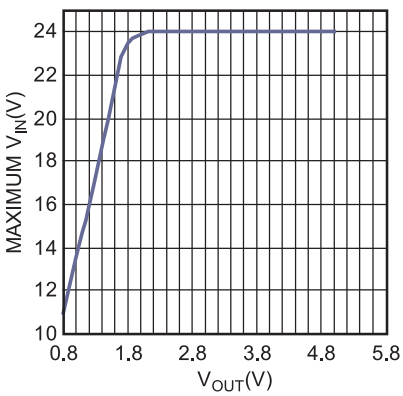


Bode Plot

I_{OUT} = 2A



Maximum V_{IN} vs. V_{OUT}



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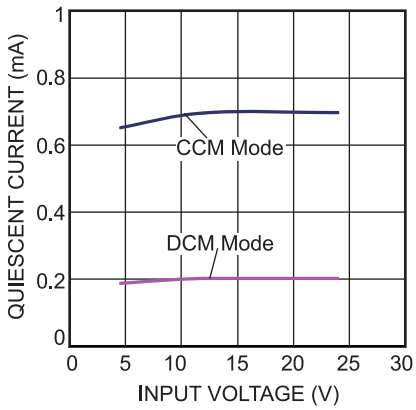
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TYPICAL CHARACTERISTICS *(continued)*

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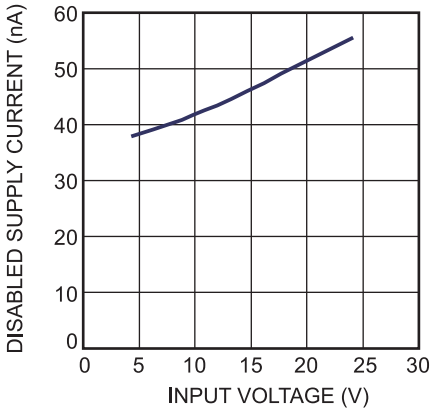
Quiescent Current vs. Input Voltage

V_{IN}=4.5V to 24V, V_{FB}=0.9V



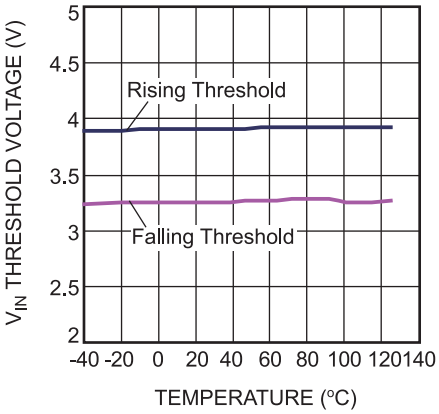
Disabled Supply Current vs. Input Voltage

V_{IN}=4.5V to 24V, EN=0V



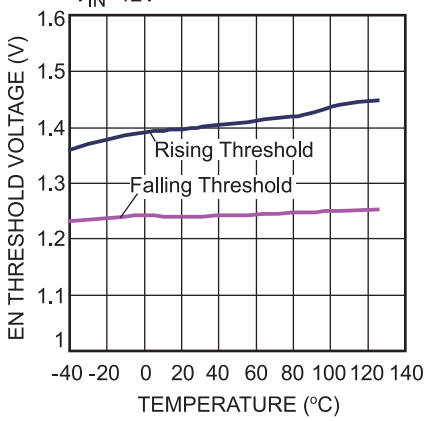
V_{IN} Threshold vs. Temperature

EN=5V

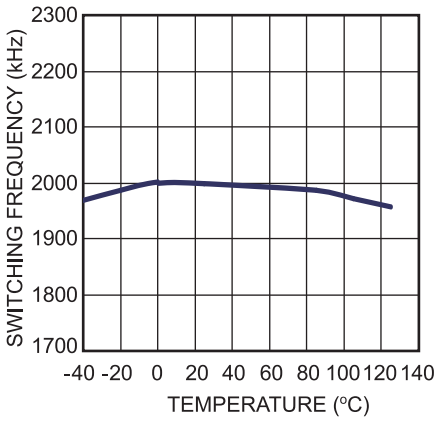


EN Threshold vs. Temperature

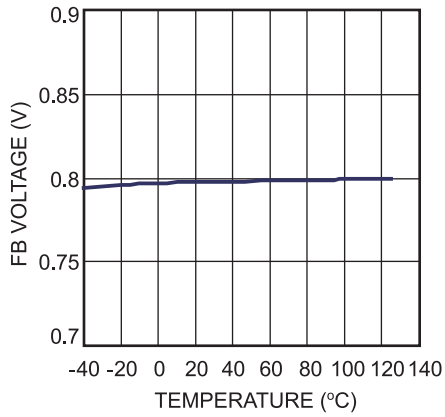
V_{IN}=12V



Switching Frequency vs. Temperature

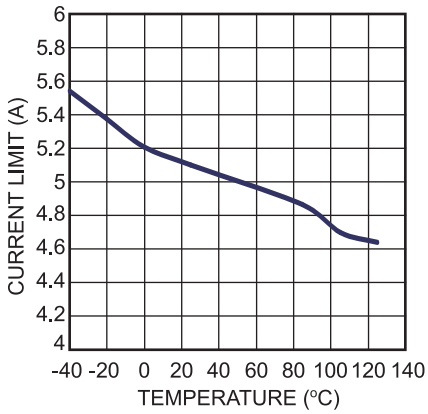


FB Voltage vs. Temperature



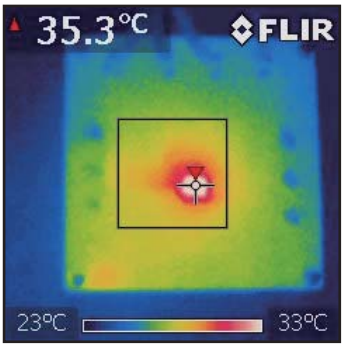
Inductor Peak-Current Limit vs. Temperature

Duty Cycle=25%



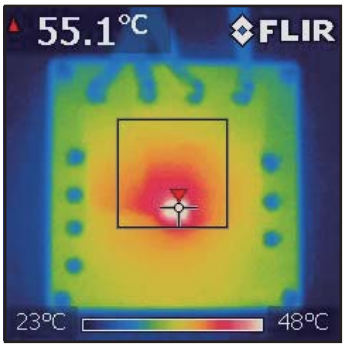
Thermal Test

V_{OUT}=1.5V, I_{OUT}=1A,
Test on EVM3620-Q-00B, T_A=25°C,
No Air Flow



Thermal Test

V_{OUT}=1.5V, I_{OUT}=2A,
Test on EVM3620-Q-00B, T_A=25°C,
No Air Flow



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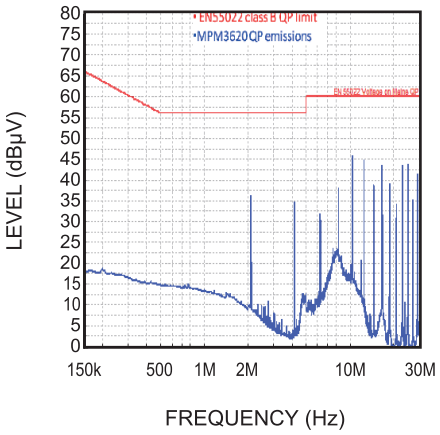
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TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

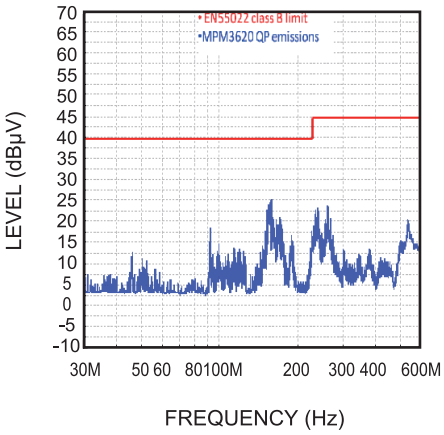
Conduction-EMI

I_{OUT}=2A
C_{IN}=64µF+10nF/0402



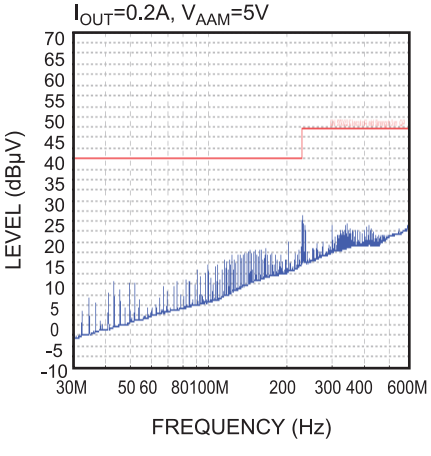
Radiatied-EMI

I_{OUT}=2A
C_{IN}=64µF+10nF/0402



Radiatied-EMI with RC Snubber

R_S=5.6Ω, C_S=330pF,
I_{OUT}=0.2A, V_{AAM}=5V



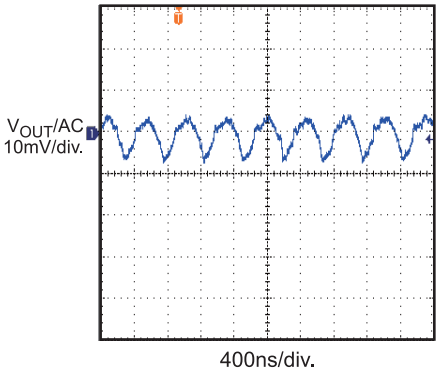
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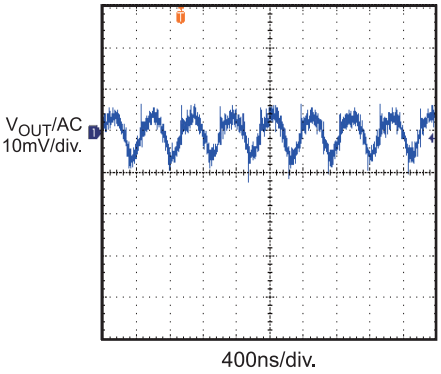
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, C_{OUT}=22µF, T_A = 25°C, unless otherwise noted.

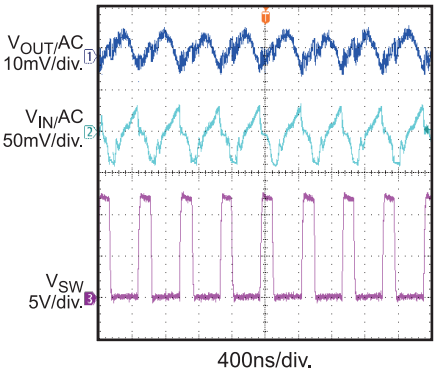
Output Ripple
Bandwidth=20MHz,
I_{OUT} = 2A



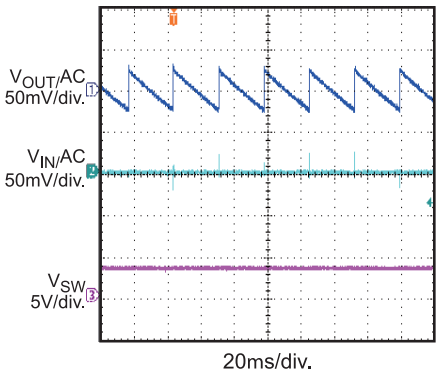
Output Ripple
Bandwidth=150MHz,
I_{OUT} = 2A



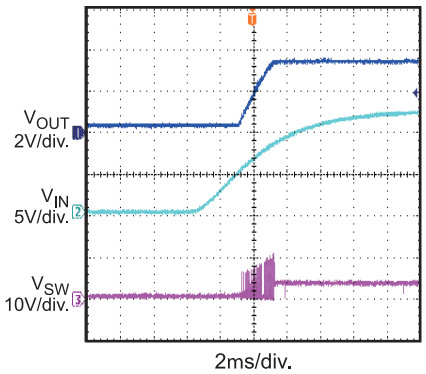
Input/Output Ripple
I_{OUT}=2A



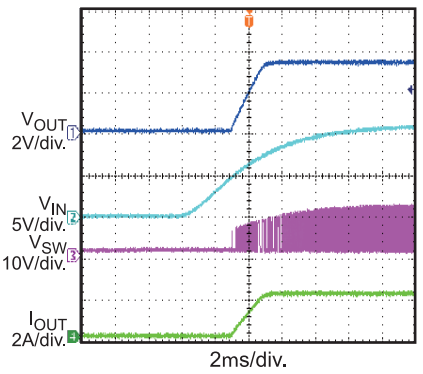
Input/Output Ripple
I_{OUT}=0A



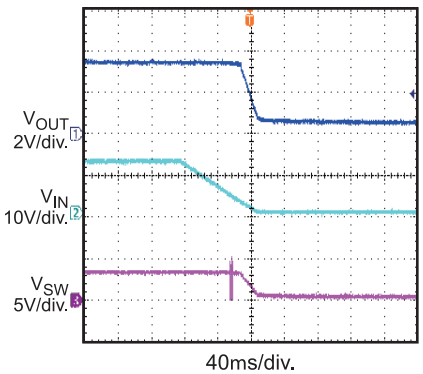
Start-Up through Input Voltage
I_{OUT} = 0A



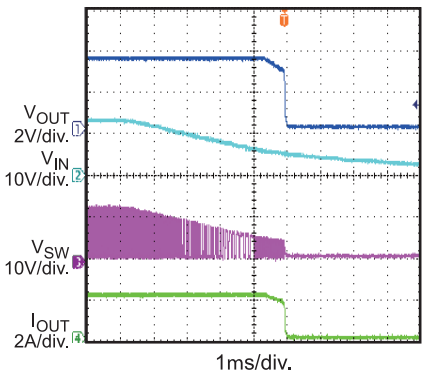
Start-Up through Input Voltage
I_{OUT} = 2A



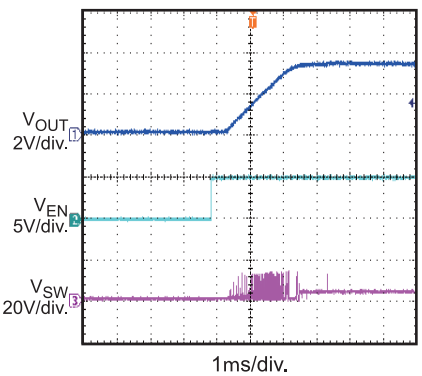
Shutdown through Input Voltage
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 2A



Start-Up through Enable
I_{OUT} = 0A



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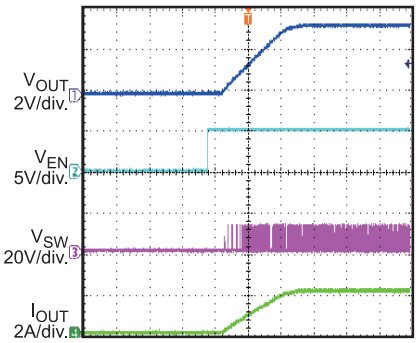
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, C_{OUT}=22µF, T_A = 25°C, unless otherwise noted.

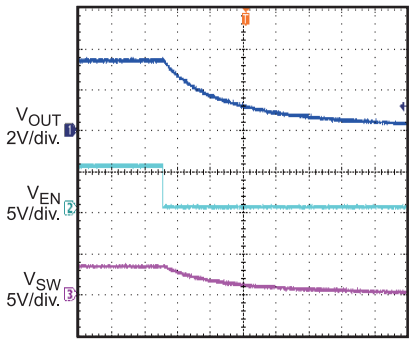
Start-Up through Enable

I_{OUT} = 2A



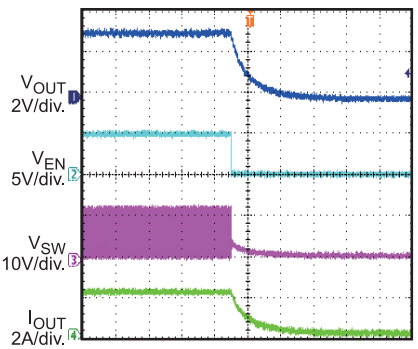
Shutdown through Enable

I_{OUT} = 0A



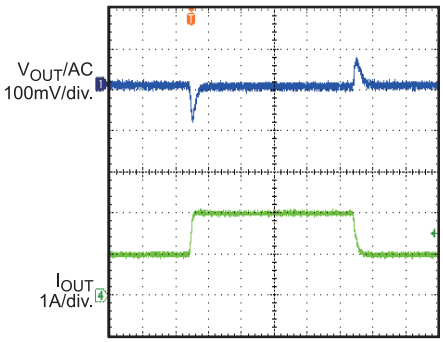
Shutdown through Enable

I_{OUT} = 2A

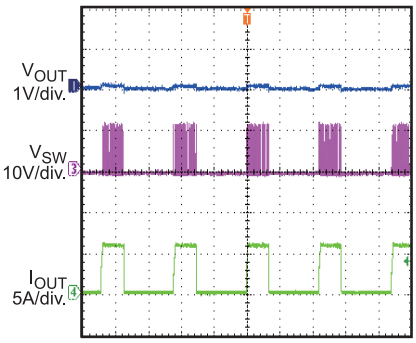


Load Transient Response

I_{OUT} transient from 1A to 2A

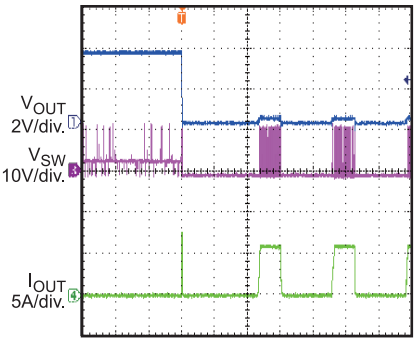


Short-Circuit Steady State



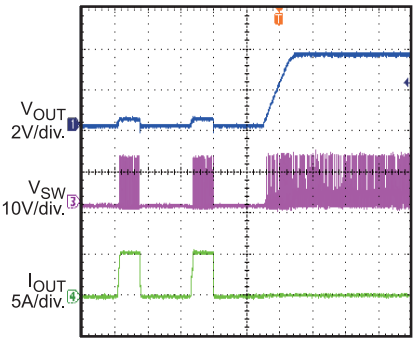
Short-Circuit Entry

I_{OUT}=0A



Short-Circuit Recovery

I_{OUT}=0A



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PIN FUNCTIONS

Package Pin #	Name	Description
1	FB	Feedback. Connect FB to the tap of an external resistor divider from the output to AGND to set the output voltage. To prevent current-limit runaway during a short-circuit fault, the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV. Place the resistor divider as close as possible to FB. Avoid placing vias on the FB traces.
2	VCC	Internal 5V LDO Output. The module integrates a LDO output capacitor, so there is no need to add an external capacitor.
3	AGND	Analog Ground. Reference ground of logic circuit. AGND is connected internally to PGND, so there is no need to add any external connections to PGND.
4, 5, 6	SW	Switch Output. A large copper plane is recommended on pins 4, 5, and 6 to improve thermal performance.
7, 8, 9	OUT	Power Output. Connect load to OUT. An output capacitor is needed.
10, 15, 19, 20	NC	No Connection. DO NOT CONNECT. NC must be left floating.
11	BST	Bootstrap. A bootstrap capacitor is integrated internally, so an external connection is not needed.
12, 13, 14	PGND	Power Ground. Reference ground of the power device. PCB layout requires extra care (please see recommended “PCB Layout Guidelines” on page 19). For best results, connect to PGND with copper and vias.
16	IN	Supply Voltage. IN supplies power for the internal MOSFET and regulator. The MPM3620 operates from a +4.5V to +24V input rail. It requires a low ESR and low-inductance capacitor to decouple the input rail. Place the input capacitor very close to IN and connect it with wide PCB traces and multiple vias.
17	EN	Enable. EN=high to enable the module. Leave EN floating or connect it to GND to disable the module.
18	AAM	Advanced Asynchronous Modulation. AAM sources a 6.2μA current from an internal 5V supply. Float AAM or drive AAM high (>2.5V) to force the MPM3620 to operate in continuous conduction mode (CCM). If AAM mode is required under light load, connect a resistor to ground to program AAM voltage in the range of 0V to1V.

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FUNCTIONAL BLOCK DIAGRAM

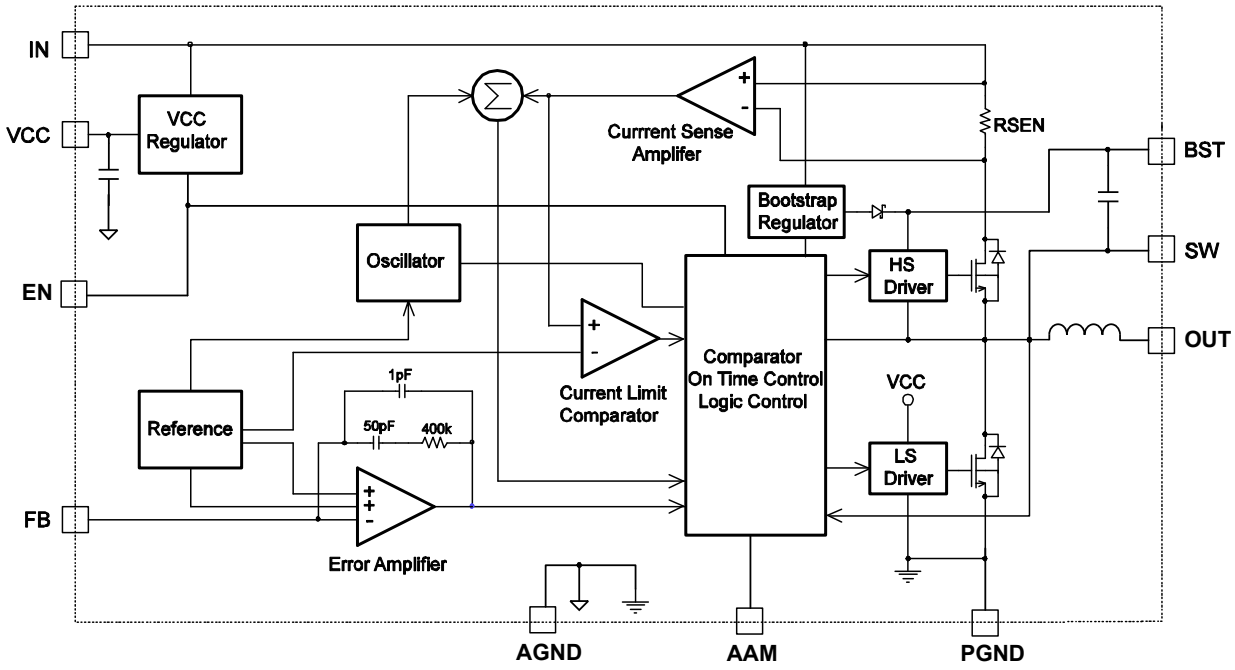


Figure 1: Functional Block Diagram

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OPERATION

The MPM3620 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs, inductor, and two capacitors. It offers a compact solution that achieves a 2A continuous output current with excellent load and line regulation over a 4.5V to 24V input-supply range.

The MPM3620 has three working modes: advanced asynchronous modulation (AAM), similar to PFM mode, discontinuous conduction mode (DCM), and continuous conduction mode (CCM). The load current increases as the device transitions from AAM mode to DCM to CCM. If AAM is floated or pulled high (>2.5V), the MPM3620 operates in CCM.

AAM Control Operation

In a light-load condition, MPM3620 operates in AAM mode (see Figure 2). Connect a resistor from AAM to GND to set V_{AAM}. V_{COMP} is the error-amplifier output, which represents the peak inductor current information. When V_{COMP} is lower than V_{AAM}, the internal clock is blocked. This causes the MPM3620 to skip pulses, achieving the light-load power save. Refer to AN032 for additional details.

The internal clock re-sets every time V_{COMP} exceeds V_{AAM}. Simultaneously, the high-side MOSFET (HS-FET) turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

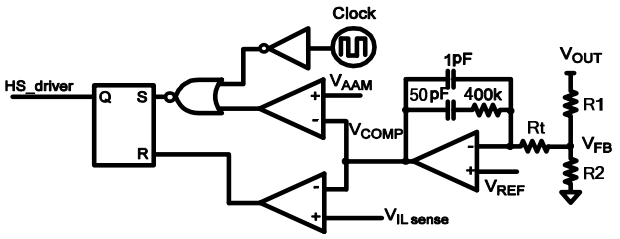


Figure 2. Simplified AAM Control Logic

DCM Control Operation

The V_{COMP} ramps up as the output current increases. When its minimum value exceeds V_{AAM}, the device enters DCM. In this mode the internal 2MHz clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and then the low-side MOSFET (LS-FET) turns on and remains on until the inductor-current value decreases to zero. The device repeats the same operation in every clock cycle to regulate the output voltage (see Figure 3).

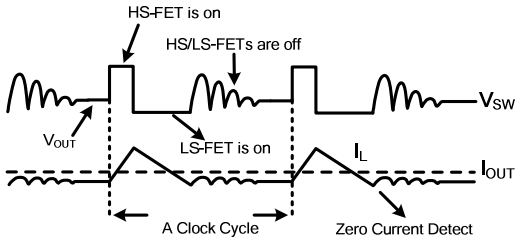


Figure 3. DCM Control Operation

CCM Control Operation

The device enters CCM from DCM once the inductor current no longer drops to zero in a clock cycle. In CCM, the internal 2MHz clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and then the LS-FET turns on and remains on until the next clock cycle starts. The device repeats the same operation in every clock cycle to regulate the output voltage.

If $V_{ILsense}$ does not reach the value set by V_{COMP} within 77% of one PWM period, the HS-FET will be forced off.

Internal V_{CC} Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5V, the output of the regulator is in full regulation. If V_{IN} is less than 5V, the output decreases. The device integrates an internal decoupling capacitor, so adding an external VCC output capacitor is unnecessary.

Error Amplifier (EA)

The error amplifier compares the FB voltage to the internal 0.798V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form the COMP voltage; the COMP voltage controls the power MOSFET current. The optimized, internal compensation network minimizes the external component count and simplifies control loop design.

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Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient input-supply voltage. The MPM3620 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.9V while its falling threshold is 3.25V.

Enable Control (EN)

EN turns the converter on and off. Drive EN high to turn on the converter; drive EN low to turn off the converter. An internal 1MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

EN is clamped internally using a 6.5V series-Zener-diode (see Figure 4).

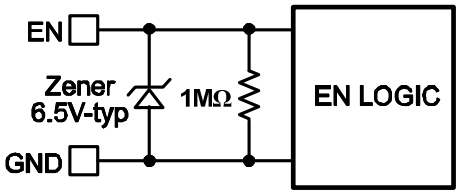


Figure 4. 6.5V Zener Diode Connection

Connecting EN to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

Connecting the EN input through a pull-up resistor to the voltage on the V_{IN} pin limits the EN input current to less than 100μA.

For example, with 12V connected to Vin, $R_{PULLUP} \geq (12V – 6.5V) \div 100\mu A = 55k\Omega$.

Internal Soft-Start (SS)

Soft-start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 5V. When SS is lower than V_{REF} (0.798V), the error amplifier uses SS as the reference. When SS is higher than V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is set internally to 1.5ms (V_{OUT} from 10% to 90%).

Pre-Bias Start-Up

The MPM3620 is designed for a monotonic start-up into a pre-biased output voltage. If the output is pre-biased to a certain voltage during start-up, the voltage on the soft-start capacitor is charged. When the soft-start capacitor's voltage exceeds the sensed output voltage at FB, the device turns on the HS-FET and the LS-FET sequentially. Output voltage ramps up following the soft-start slew rate.

Over-Current Protection (OCP) and Hiccup

The MPM3620 has a cycle-by-cycle over-current limiting control. When the inductor current-peak value exceeds the internal peak current-limit threshold, the HS-FET turns off and the LS-FET turns on, remaining on until the inductor current falls below the internal valley current-limit threshold. The valley current-limit circuit is employed to decrease the operation frequency (after the peak current-limit threshold is triggered). Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (50% below the reference, typically). Once UV is triggered, the MPM3620 enters hiccup mode to re-start the part periodically. This protection mode is useful when the output is dead-shorted to ground and greatly reduces the average short-circuit current to alleviate thermal issues and protect the converter. The MPM3620 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown (TSD)

To prevent thermal damage, MPM3620 stops switching when the die temperature exceeds 150°C. As soon as the temperature drops below its lower threshold (130°C, typically), the power supply resumes operation.

Floating Driver and Bootstrap Charging

An internal bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1, and C2 (see Figure 5). If (V_{BST}-V_{SW}) exceeds 5V, U1 regulates M1 to maintain a 5V voltage across C4.

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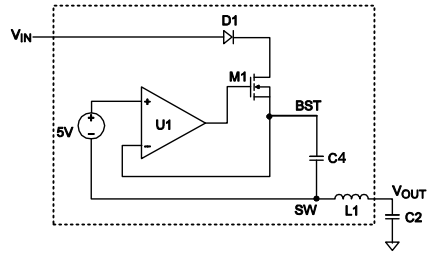


Figure 5. Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltage, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events shut down the chip: V_{IN} low, V_{EN} low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Additional RC Snubber Circuit

An additional RC snubber circuit can be chosen to clamp the voltage spike and damp the ringing voltage for better EMI performance.

The power dissipation of the RC snubber circuit is estimated by the formula below:

$$P_{Loss} = f_S \times C_S \times V_{IN}^2$$

Where f_S is the switching frequency, C_s is the snubber capacitor, and V_{IN} is the input voltage.

For improved efficiency, the value of C_S should not be set too high. Generally, a 5.6Ω R_S and a 330pF C_S are recommended to generate the RC snubber circuit (see Figure 6).

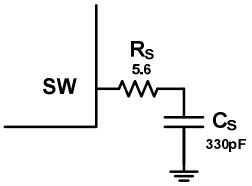


Figure 6. Additional RC Snubber Circuit

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see "Typical Application" on page 1). Choose R1 (refer to Table 1); R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.798V} - 1}$$

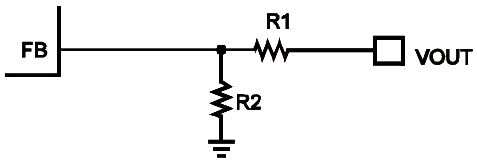


Figure 7. Feedback Network

See Table 1 and Figure 7 for the feedback network and a list of recommended feedback network parameters for common output voltages.

Table 1. Recommended Parameters for Common Output Voltages

			Small Solution Size(C_{IN}=10µF, C_{OUT}=22µF/0805/16V)						Low V_{OUT} Ripple(C_{IN}=10µF, C_{OUT}=2X22µF/0805/16V)				
V_{IN} (V)	V_{OUT} (V)	R_{AAM} (kΩ)	R1 (kΩ)	R2 (kΩ)	V_{OUT} PFM Ripple (mV)[9]	V_{OUT} PWM Ripple (mV)[10]	Load Transient (mV)[11]		R1 (kΩ)	R2 (kΩ)	V_{OUT} PFM Ripple (mV)[9]	V_{OUT} PWM Ripple (mV)[10]	Load Transient (mV)[11]
24	5	33.2	160	30.1	106	19.2	168		75	14.3	35	10.4	96
	3.3	16.5	160	51	79	13.6	137		82	26.1	33	7.6	75
	2.5	10	180	84.5	76	10.8	116		102	47.5	37	5.8	70
21	5	38.3	160	30.1	97	17.6	172		75	14.3	32	9.4	98
	3.3	22.1	160	51	84	12.4	146		82	26.1	34	7	79
	2.5	16.2	180	84.5	81	10	120		102	47.5	36	5.2	78
19	5	43.2	160	30.1	87	16.4	170		75	14.3	31	8.8	96
	3.3	29.4	160	51	84	11.4	141		82	26.1	45	6.6	83
	2.5	19.6	160	75	76	9.8	113		102	47.5	38	5	80
16	5	51.3	160	30.1	82	15.6	176		75	14.3	29	7.8	96
	3.3	37.4	160	51	91	10.6	146		82	26.1	42	6	83
	2.5	26.1	160	75	70	9.6	116		102	47.5	41	4.8	82
	1.8[12]	17.4	180	143	68	8.6	108		102	82	31	4	70
14	5	57.6	160	30.1	70	14.8	172		75	14.3	27	7.4	95
	3.3	45.3	160	51	89	10.2	149		82	26.1	41	5.6	81
	2.5	34	160	75	74	9.4	120		102	47.5	44	4.6	88
	1.8[12]	26.1	180	143	73	8.4	114		102	82	37	4.2	75
	1.5[12]	20.5	180	205	62	7.2	103		120	137	36	3.6	72
12	5	63.4	160	30.1	70	13.8	174		75	14.3	25	6.4	91
	3.3	56	160	51	82	9.4	152		82	26.1	37	5.2	82
	2.5	42.2	160	75	66	9	125		82	38.3	35	4.4	76
	1.8	32.4	160	127	64	7.8	112		102	82	36	4	75
	1.5[12]	25.5	160	180	60	6.6	104		102	115	33	3.4	72
	1.2[12]	21	300	604	81	6.2	155		143	280	38	3	88

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Table 1. Recommended Parameters For Common Output Voltages*(continued)*

			Small Solution Size(C_{IN}=10µF, C_{OUT}=22µF/0805/16V)						Low V_{OUT} Ripple(C_{IN}=10µF, C_{OUT}=2X22µF/0805/16V)				
V_{IN} (V)	V_{OUT} (V)	R_{AAM} (kΩ)	R1 (kΩ)	R2 (kΩ)	V_{OUT} PFM Ripple (mV) (9)	V_{OUT} PWM Ripple (mV) (10)	Load Transient (mV) (11)		R1 (kΩ)	R2 (kΩ)	V_{OUT} PFM Ripple (mV) (9)	V_{OUT} PWM Ripple (mV) (10)	Load Transient (mV) (11)
10	5	76.8	160	30.1	73	13.2	172		75	14.3	44	6.2	96
	3.3	63.4	143	45.3	78	8.4	136		82	26.1	35	4.8	87
	2.5	51	143	66.5	55	8.2	118		82	38.3	28	4	78
	1.8	38.3	143	113	54	7.2	106		102	82	32	3.6	81
	1.5(12)	33	160	180	57	6	111		102	115	31	3.2	76
	1.2(12)	26.7	221	442	78	5.4	140		102	200	31	2.8	74
	1(12)	21	221	887	61	4.8	134		160	649	39	2.6	106
8	5	88.7	160	30.1	82	9.2	166		75	14.3	38	5	93
	3.3	73.2	143	45.3	74	7.6	143		82	26.1	31	3.8	91
	2.5	59	143	66.5	56	7	124		82	38.3	28	3.4	77
	1.8	48.7	143	113	47	6.4	114		82	64.9	27	3	72
	1.5(12)	40.2	160	180	52	5.4	120		102	115	28	2.8	84
	1.2(12)	33.2	143	280	49	5	105		102	200	28	2.6	78
	1(12)	28.7	143	562	63	4.6	97		102	402	29	2.2	75
5	3.3	88.7	143	45.3	42	6	137		62	19.6	17	3.4	74
	2.5	78.7	143	66.5	49	5.8	140		75	34.8	22	3.2	76
	1.8	66.5	143	113	44	5.2	124		75	59	23	2.8	71
	1.5(12)	57.8	143	162	46	5	118		82	93.1	26	2.4	76
	1.2(12)	47.5	143	280	44	4.6	116		82	162	26	2.2	73
	1(12)	42.2	143	562	50	4.4	109		102	402	29	2	83

Notes:

9) V_{OUT} PFM ripple is tested when Io=0A, for those specs noted (12), the ripple is tested when Io=1mA.
10) V_{OUT} PWM ripple is tested when Io=2A.
11) Load transient from 1A to 2A, slew rate =0.8A/µs.
12) In these specs, BST operation current will charge the output voltage higher than the setting value when there is completely no load, due to a large divider resistor value. A 10µA load current can pull the output voltage to a normal regulation level.

Normally, it is recommended to set output voltage from 0.8V to 5.5V. However, it can be set larger than 5.5V. In this case, the output-voltage ripple is larger due to a larger inductor-ripple current. An additional output capacitor is needed to reduce the output-ripple voltage.

If output voltage is high, heat dissipation becomes more important. Please refer to the "PCB Layout Guidelines" section on page 19 to achieve better thermal performance.

For thermal consideration, the relationship curve between output voltage and maximum output current is shown in Figure 8:

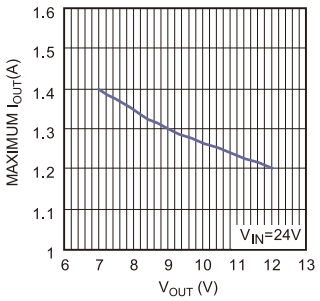


Figure 8: Maximum Output Current vs. Output Voltage

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Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for improved performance. Use ceramic capacitors with X5R or X7R dielectrics for optimum results because of their low ESR and small temperature coefficients. For most applications, use a 10µF capacitor.

Since C1 absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor is estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, make sure they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at input. The input-voltage ripple caused by capacitance can be estimated as:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Setting the AAM Voltage

The AAM voltage is used to set the transition point from AAM to CCM. AAM voltage should be chosen to provide the best combination of efficiency, stability, ripple, and transient. Drive AAM high(>2.5V) to force the MPM3620 always operate in CCM.

If the AAM voltage is set lower than the recommended value, then stability and ripple improve, however, efficiency during AAM mode and transient degrades. Likewise, if the AAM voltage is set higher than the recommended value, then the efficiency during AAM and transient improves, with stability and ripple degrading. Therefore calculate the optimal balance point of AAM voltage for good efficiency, stability, ripple, and transient.

Adjust the AAM threshold by connecting a resistor from AAM to ground (see Figure 9). An internal 6.2µA current source charges the external resistor.

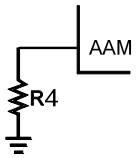


Figure 9. AAM Network

Generally, R4 is then given by:

$$V_{AAM} = R4 \times 6.2\mu A$$

Refer to Figure 10 when setting the AAM resistor.

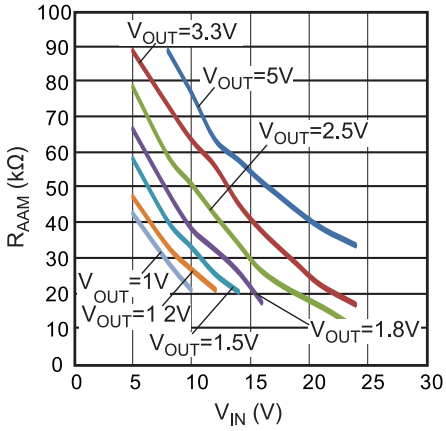


Figure 10. Recommended AAM Resistor Selection

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output-voltage ripple low. The output-voltage ripple is estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

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Where L_1 is the inductor value, R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor, and L_1=1µH.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency; the capacitance causes the majority of the output-voltage ripple. For simplification, the output-voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor affect the stability of the regulation system. The MPM3620 internal compensation is optimized for a wide range of capacitance and ESR values.

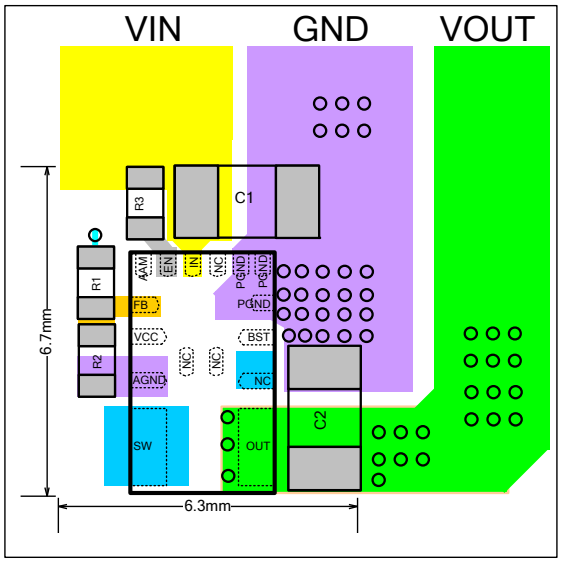
PCB Layout Guidelines [13]

Efficient PCB layout is critical to achieve stable operation, particularly for input capacitor placement. For best results, refer to Figure 11 and follow the guidelines below:

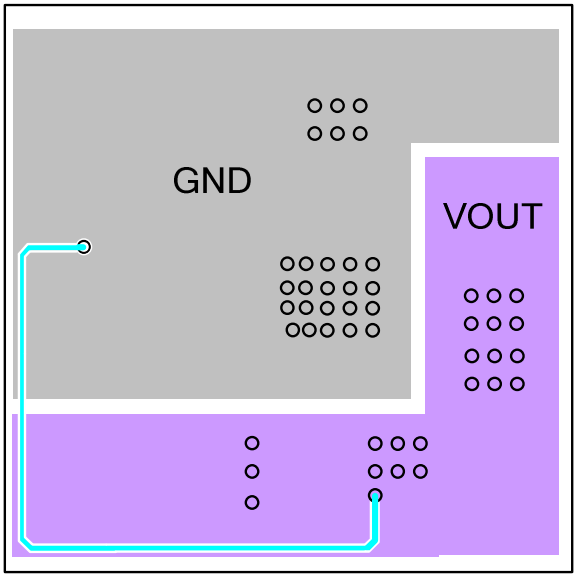
1. Use large ground plane to connect directly to PGND. If the bottom layer is ground plane, add vias near PGND.
2. The high-current paths (PGND, IN, and OUT) should have short, direct, and wide traces. Place the ceramic input capacitor close to IN and PGND. Keep the input capacitor and IN connection as short and wide as possible.
3. Place the external feedback resistors next to FB.
4. Keep the feedback network away from the switching node.

Notes:

13) The recommended layout is based on the "Typical Application Circuits" on pages 21-23.



Top Layer



Bottom Layer

Figure 11. Recommended PCB Layout

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Design Example

Table 2 below is a design example following the application guidelines for the specifications:

Table 2. Design Example

V_{IN}	12V
V_{OUT}	3.3V
Io	2A

The detailed application schematic is shown in Figure 13. The typical performance and circuit waveforms have been shown in the “Typical Performance Characteristics” section. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS (14)(15)

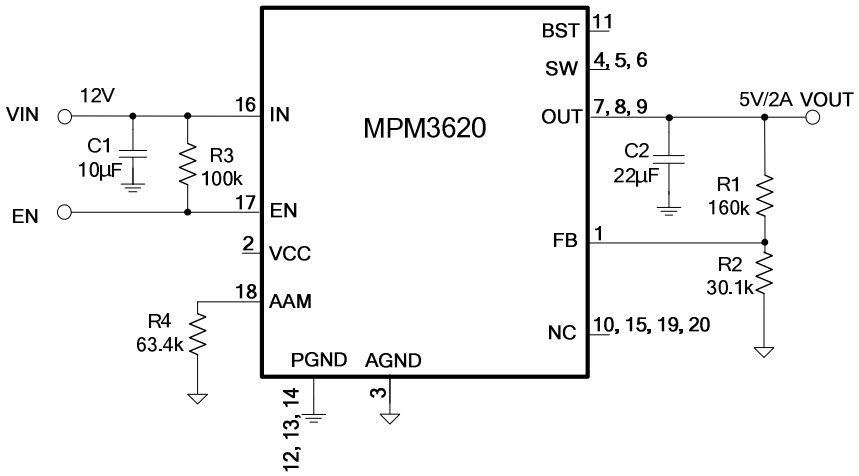


Figure 12. V_{OUT}=5V, I_{OUT}=2A

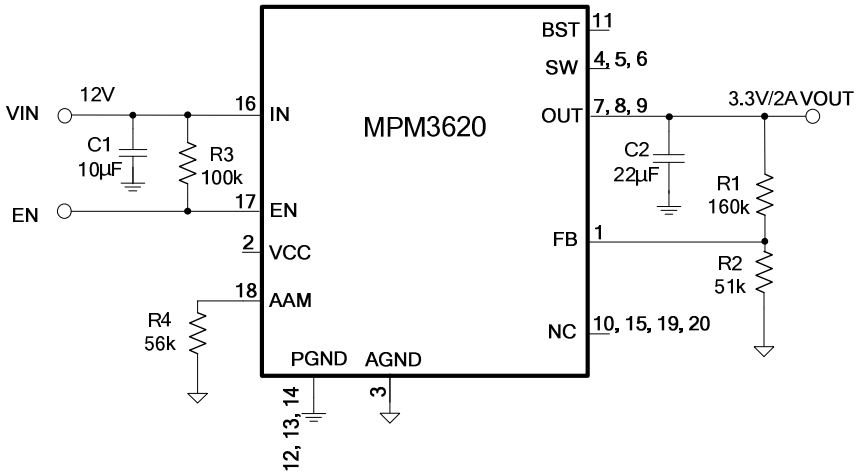


Figure 13. V_{OUT}=3.3V, I_{OUT}=2A

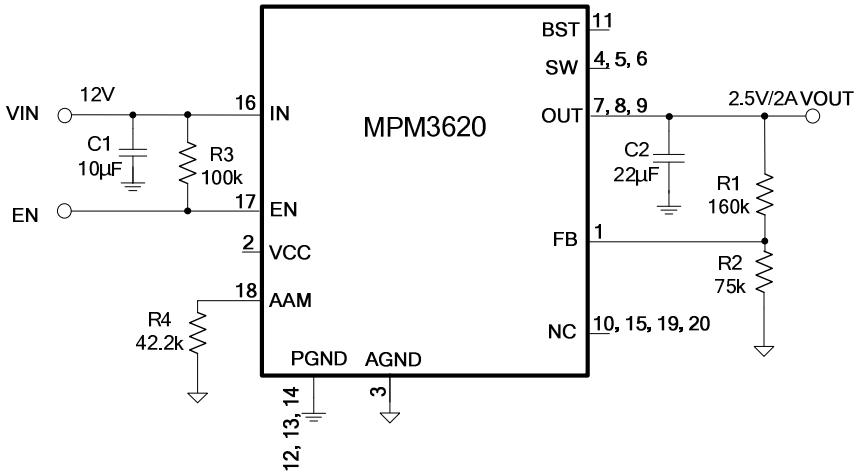


Figure 14. V_{OUT}=2.5V, I_{OUT}=2A

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TYPICAL APPLICATION CIRCUITS *(continued)*

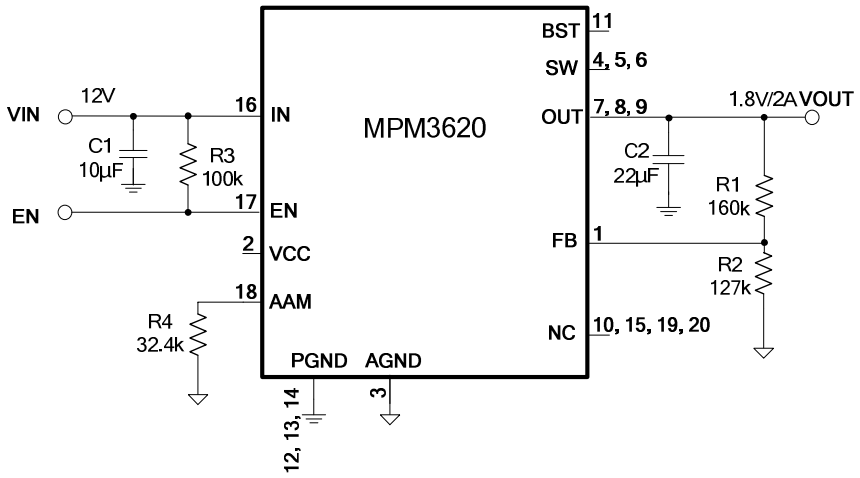


Figure 15. V_{OUT}=1.8V, I_{OUT}=2A

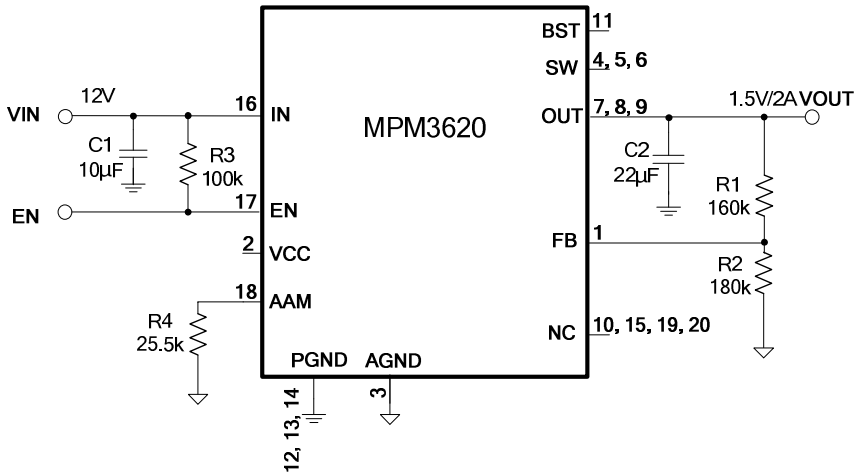


Figure 16. V_{OUT}=1.5V, I_{OUT}=2A

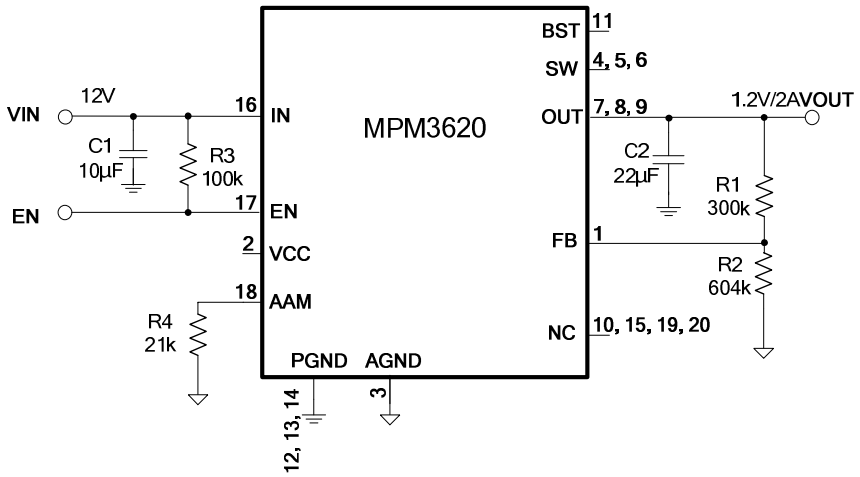


Figure 17. V_{OUT}=1.2V, I_{OUT}=2A

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TYPICAL APPLICATION CIRCUITS *(Continued)*

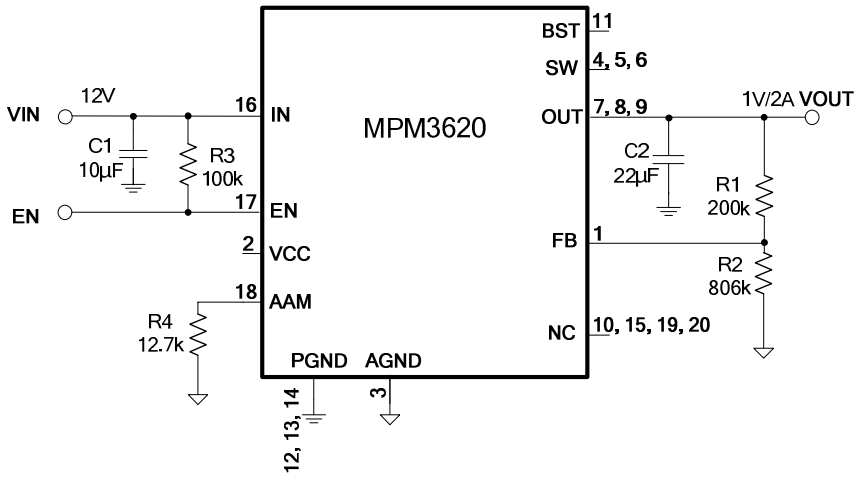


Figure 18. V_{OUT}=1V, I_{OUT}=2A

Notes:

14) In $12V_{IN}$ to $1V_{OUT}$ application conditions, the HS-FET's on-time is close to the minimum on-time; although the SW may have a little jitter, the output-voltage ripple is smaller than 15mV in PWM mode.

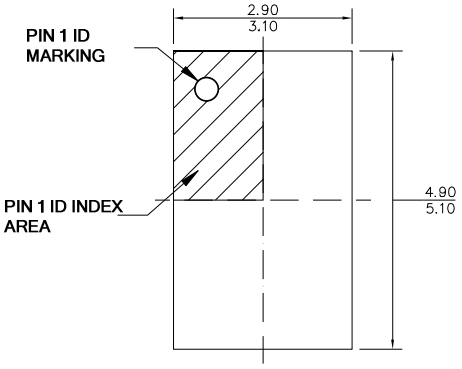
15) In $12V_{IN}$ to 1.5/1.2/1 V_{OUT} application conditions, the BST operation current will charge the output voltage higher than the setting value when there is completely no load, due to a large divider resistor value. A 10µA load current can pull the output voltage to a normal regulation level.

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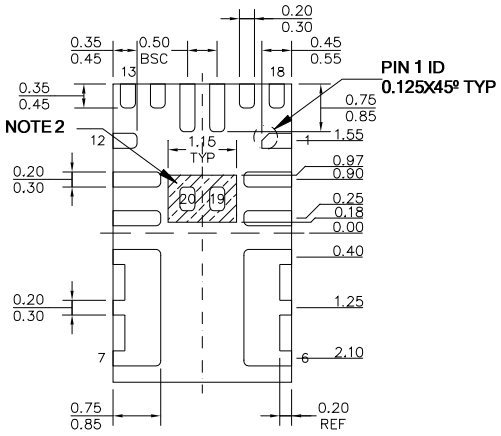
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PACKAGE INFORMATION

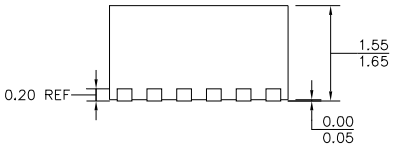
QFN-20 (3mmx5mmx1.6mm)



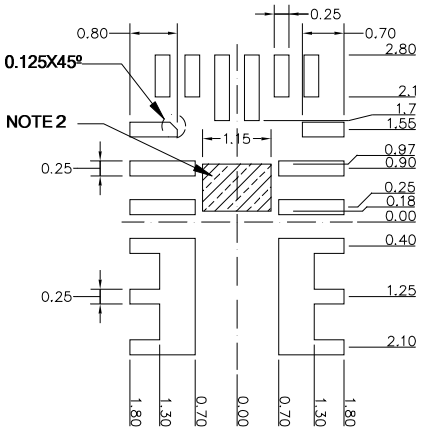
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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