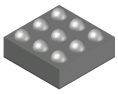
# Regulator - Fixed-Output, Synchronous, TINYBOOST®, 2.5 MHz

# FAN48611



WLCSP9 1.215x1.215x0.581
CASE 567QW

## Description

The FAN48611 is a low−power boost regulator designed to provide a minimum voltage regulated rail from a standard single−cell Li−Ion battery and advanced battery chemistries. Even below the minimum system battery voltage, the device maintains output voltage regulation. The combination of built−in power transistors, synchronous rectification, and low supply current suit the FAN48611 for battery−powered applications.

The FAN48611 is available in a 9−bump, 0.4 mm pitch, Wafer−Level Chip−Scale Package (WLCSP).

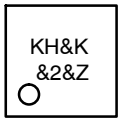
## Features

- Input Voltage Range: 2.7 V to 4.8 V
- Output Voltage: 5.25 V
- 350 mA Maximum Output Current
- Internal Synchronous Rectification
- True Load Disconnect
- Short−Circuit Protection
- 9−Bump, 1.215 mm x 1.215 mm, 0.4 mm Pitch, WLCSP
- Three External Components: 2012 1 μH Inductor, 0402 Case Size Input / Output Capacitors
- This Device is Pb−Free, Halide Free and is RoHS Compliant

## Applications

- Class−D Audio Amplifier and USB OTG Supply
- Boost for Low−Voltage Li−Ion Batteries
- Smart Phones, Tablets, Portable Devices, and Wearables

## MARKING DIAGRAM




KH = Specific Device Code
&K = 2−Digits Lot Run Traceability Code
&2 = 2−Digit Date Code
&Z = Assembly Plant Code

## TYPICAL APPLICATION

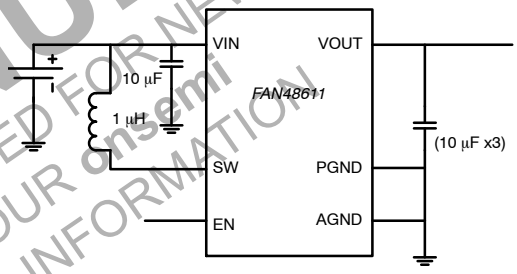



Figure 1. Typical Application

## ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

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## BLOCK DIAGRAM

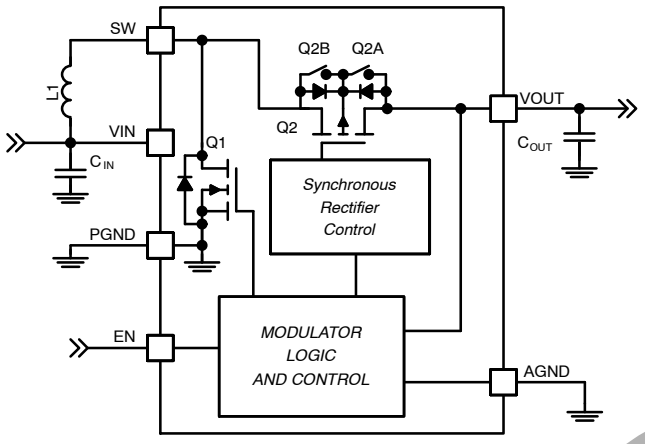


**Figure 2. IC Block Diagram**

**Table 1. Recommended Components**

| Component | Description | Vendor | Parameter | Typ. | Unit |
|---|---|---|---|---|---|
| L1 | 2012, 1.9 A, 0.6 mm Max. Height | PIXC20120F1R0MDR | L | 1 | µH |
| | | | DCR (Series R) | 175 | mΩ |
| CIN | 20%, 6.3 V, X5R, 0402 | C1005X5R0J106M050BC TDK | C | 10 | µF |
| COUT | 20%, 6.3 V, X5R, 0402 | C1005X5R0J106M050BC TDK | C | 10 | µF |

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## PIN CONFIGURATION

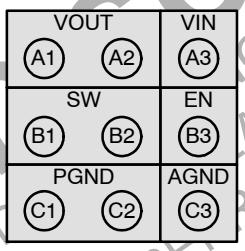


**Figure 3. Top View**

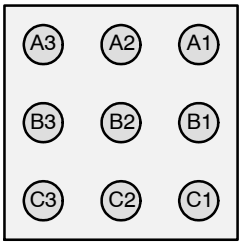


**Figure 4. Bottom View**

### PIN DEFINITIONS

| Pin # | Name | Description |
|---|---|---|
| A1, A2 | VOUT | *Output Voltage*. This pin is the output voltage terminal; connect directly to $C_{OUT}$. |
| A3 | VIN | *Input Voltage*. Connect to the Li−Ion battery input power source and the bias supply for the gate drivers. |
| B1, B2 | SW | *Switching Node*. Connect to inductor. |
| B3 | EN | *Enable*. When this pin is HIGH, the circuit is enabled. Connection to a logic voltage of 1.8 V and delivery voltage after UVLO typical voltage of 2.2 V is recommended. |
| C1, C2 | PGND | *Power Ground*. This is the power return for the IC. $C_{OUT}$ capacitor should be returned with the shortest path possible to these pins. |
| C3 | AGND | *Analog Ground*. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin. Connect to PGND at a single point. |



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## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IN}$ | Voltage on VIN Pin | | −0.3 | 6.0 | V |
| $V_{OUT}$ | Voltage on VOUT Pin | | −0.3 | 6.0 | V |
| $V_{SW}$ | Voltage on SW Node | DC | −0.3 | 6.0 | V |
| | | Transient: 10 ns, 3 MHz | −1.0 | 8.0 | |
| $V_{CC}$ | Voltage on Other Pins | | −0.3 | 6.0 (Note 1) | V |
| ESD | Electrostatic Discharge Protection Level | Human Body Model, ANSI/ESDA/JEDEC JS−001−2012 | 2 | | kV |
| | | Charged Device Model per JESD22−C101 | 2 | | |
| $T_J$ | Junction Temperature | | −40 | +150 | °C |
| $T_{STG}$ | Storage Temperature | | −65 | +150 | °C |
| $T_L$ | Lead Soldering Temperature, 10 Seconds | | − | +260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Lesser of 6.0 V or $V_{IN}$ + 0.3 V.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IN}$ | Supply Voltage | 2.7 | 4.8 | V |
| $I_{OUT}$ | Maximum Output Current | 350 | − | mA |
| $T_A$ | Ambient Temperature | −40 | +85 | °C |
| $T_J$ | Junction Temperature | −40 | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**THERMAL PROPERTIES** (Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with four− layer 2s2p boards with vias in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature, $T_{J(max)}$, at a given ambient temperature, $T_A$.)

| Symbol | Characteristic | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | Junction−to−Ambient Thermal Resistance | 50 | °C/W |

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**ELECTRICAL CHARACTERISTICS** (Recommended operating conditions, unless otherwise noted, circuit per Figure 1, VOUT= 5.25 V, VIN = 2.7 V to 4.8 V, and TA = −40°C to 85°C. Typical values are given VIN = 3.7 V and TA = 25°C.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $I_Q$ | $V_{IN}$ Quiescent Current | $V_{IN}$ = 3.7 V, $I_{OUT}$ = 0, EN = $V_{IN}$ | – | 90 | 140 | μA |
| | | Shutdown: EN = 0, $V_{IN}$ = 3.7 V, $V_{OUT}$ = 0 V | – | 2.7 | 10.0 | |
| $V_{UVLO}$ | Under−Voltage Lockout | $V_{IN}$ Rising | – | 2.2 | 2.3 | V |
| $V_{UVLO_HYS}$ | Under−Voltage Lockout Hysteresis | | – | 150 | – | mV |
| **INPUTS** | | | | | | |
| $V_{IH}$ | Enable HIGH Voltage | | 1.2 | – | – | V |
| $V_{IL}$ | Enable LOW Voltage | | – | – | 0.4 | V |
| $I_{PD}$ | Current Sink Pull−Down | EN Pin, Logic HIGH | – | 100 | | nA |
| $R_{LOW}$ | Low−State Active Pull−Down | EN Pin, Logic LOW | 200 | 300 | 400 | kΩ |
| **OUTPUTS** | | | | | | |
| $V_{REG}$ | Output Voltage Accuracy DC (Note 2) | Referred to $V_{OUT}$ | −2 | – | 4 | % |
| $I_{LK_OUT}$ | VIN−to−VOUT Leakage Current | $V_{OUT}$ = 0, EN = 0, $V_{IN}$ = 2.7 V | – | – | 1 | μA |
| $I_{LK}$ | VOUT−to−VIN Reverse Leakage Current | $V_{OUT}$ = 5.3 V, EN = 0, $V_{IN}$ = 2.7 V | – | – | 3.5 | μA |
| $V_{RIPPLE}$ | Output Ripple (Note 3) | 0 mA to 300 mA | – | 30 | – | mV |
| $V_{TRLOAD}$ | Load Transient (Note 3) | $I_{LOAD}$ = 0 mA <−−> 120 mA, $t_R$ = $t_F$ = 1 μs | – | ±30 | – | mV |
| | | $I_{LOAD}$ = 0 mA <−−> 285 mA, $t_R$ = $t_F$ = 8 μs | – | ±90 | – | |
| $V_{TRLINE}$ | Line Transient (Note 3) | $V_{IN}$ = 3.2 V <−−> 3.9 V, $I_{LOAD}$ = 120 mA, $t_R$ = $t_F$ = 7 μs | – | ±50 | – | mV |
| η | Efficiency (Note 3) | $V_{IN}$ = 3 V, $I_{LOAD}$ = 5 mA | – | 85 | – | % |
| | | $V_{IN}$ = 3 V, $I_{LOAD}$ = 200 mA | – | 90 | – | |
| | | $V_{IN}$ = 3.6 V, $I_{LOAD}$ = 200 mA | – | 91 | – | |
| | | $V_{IN}$ = 3.6 V, $I_{LOAD}$ = 300 mA | – | 92 | – | |
| **TIMING** | | | | | | |
| $f_{SW}$ | Switching Frequency | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.25 V, $I_{LOAD}$ = 300 mA | 2.0 | 2.5 | 3.0 | MHz |
| $t_{SS}$ | Soft−Start EN HIGH to Regulation (Note 3) | $V_{IN}$ = 3.0 V, $V_{OUT}$ = 5.25 V, $I_{LOAD}$ = 0 mA, $C_{OUT}$ = 3 x 10 μF | – | 1000 | – | μs |
| $I_{SS}$ | Input Peak Current | | – | 90 | 200 | mA |
| $t_{RST}$ | FAULT Restart Timer (Note 3) | | – | 20 | – | ms |
| **POWER STAGE** | | | | | | |
| $R_{DS(ON)N}$ | N−Channel Boost Switch $R_{DS(ON)}$ | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.25 V | – | 80 | 130 | mΩ |
| $R_{DS(ON)P}$ | P−Channel Sync. Rectifier $R_{DS(ON)}$ | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.25 V | – | 65 | 115 | mΩ |
| $I_{V_LIM}$ | Boost Valley Current Limit | $V_{OUT}$ = 5.25 V | – | 750 | – | mA |
| $I_{V_LIM_SS}$ | Boost Soft−Start Valley Current Limit | $V_{IN}$ < $V_{OUT}$ < $V_{OUT_TARGET}$ | – | 375 | – | A |
| $T_{150T}$ | Over−Temperature Protection (OTP) | | – | 150 | – | °C |
| $T_{150H}$ | OTP Hysteresis | | – | 20 | – | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. DC $I_{LOAD}$ from 0 to 0.35 A. $V_{OUT}$ measured from mid−point of output voltage ripple. Effective capacitance of $C_{OUT} \geq 6$ μF.
3. Guaranteed by design and characterization; not tested in production.

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## TYPICAL PERFORMANCE CHARACTERISTICS

(Unless otherwise specified; $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.25 V, $T_A$ = 25°C, and circuit according to Figure 1.)

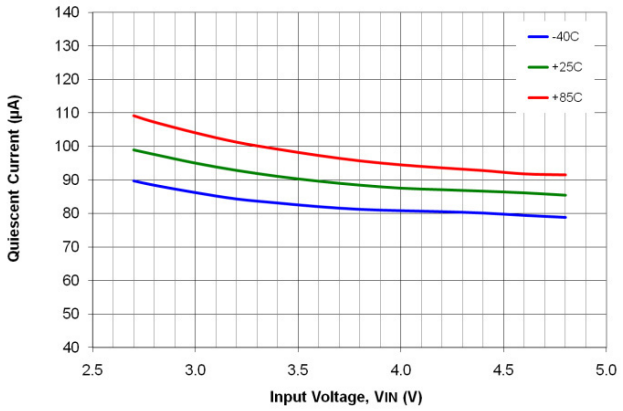


**Figure 5. Quiescent Current vs. Input Voltage and Temperature**

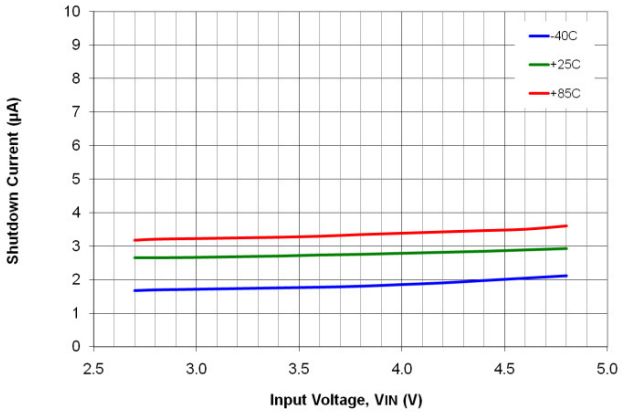


**Figure 6. Shutdown Current vs. Load Voltage and Temperature**

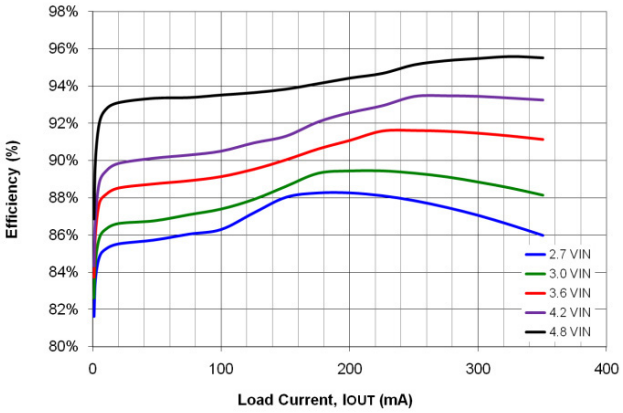


**Figure 7. Efficiency vs. Load Current and Input Voltage**

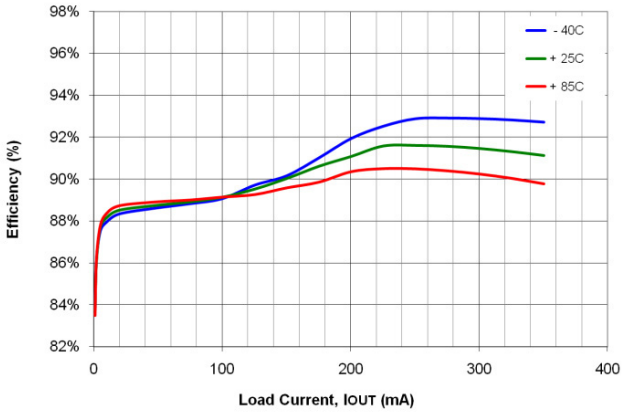


**Figure 8. Efficiency vs. Load Current and Temperature**

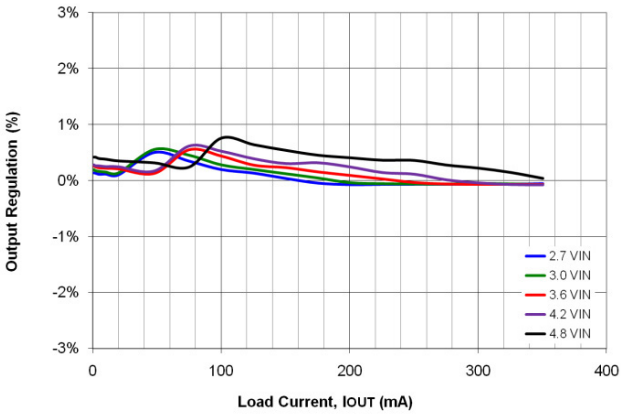


**Figure 9. Output Regulation vs. Load Current and Input Voltage**

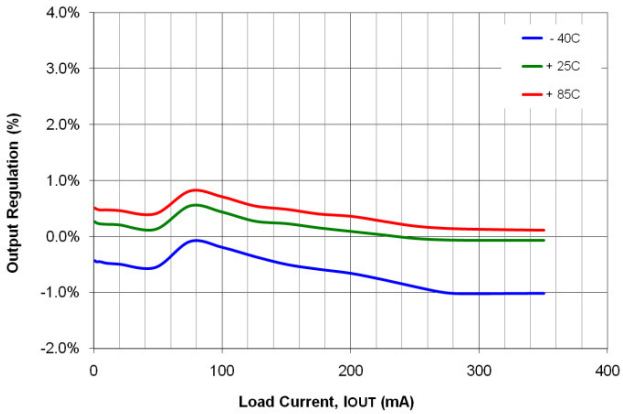


**Figure 10. Output Regulation vs. Load Current and Temperature**



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## TYPICAL PERFORMANCE CHARACTERISTICS

(Unless otherwise specified; $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.25 V, $T_A$ = 25°C, and circuit and components according to Figure 1.)

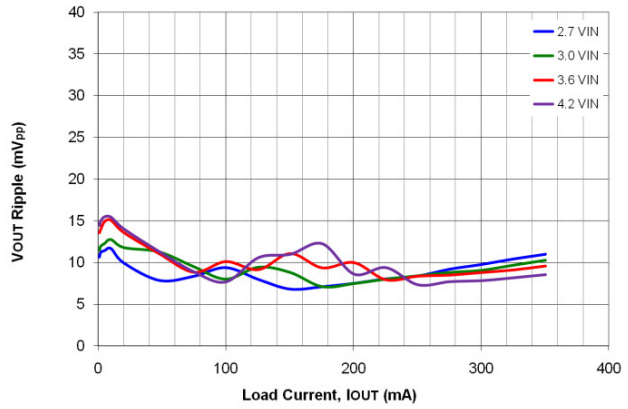


**Figure 11. Output Ripple vs. Load Current and Input Voltage**

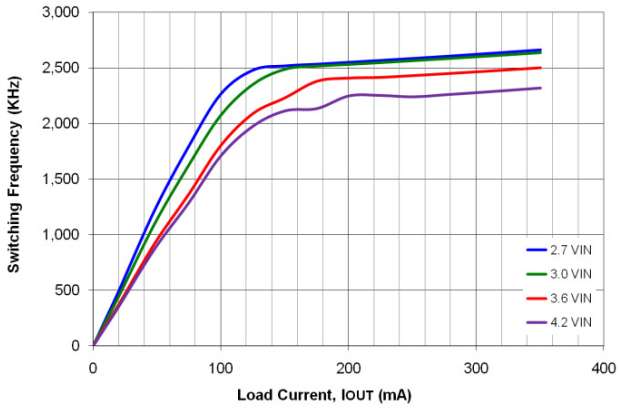


**Figure 12. Switching Frequency vs. Load Current and Temperature**

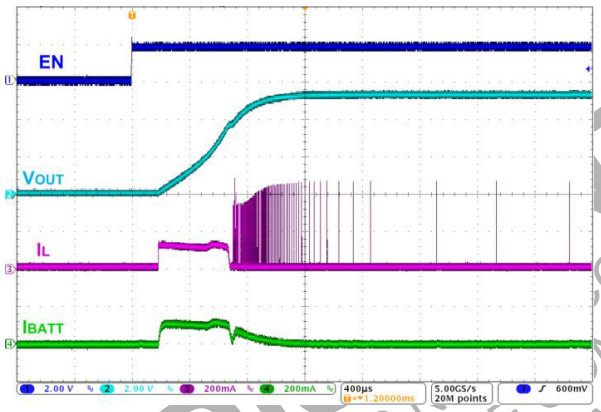


**Figure 13. Startup, No Load**

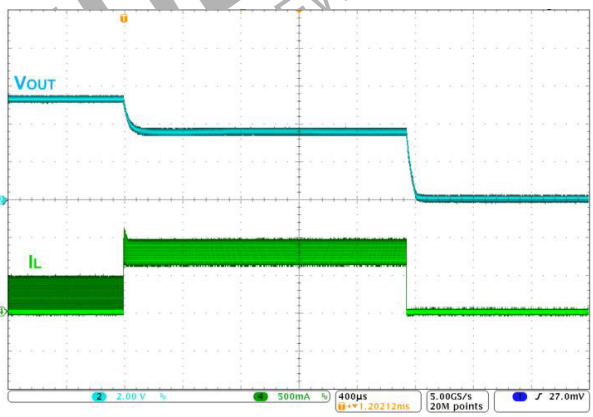


**Figure 14. Overload Protection**

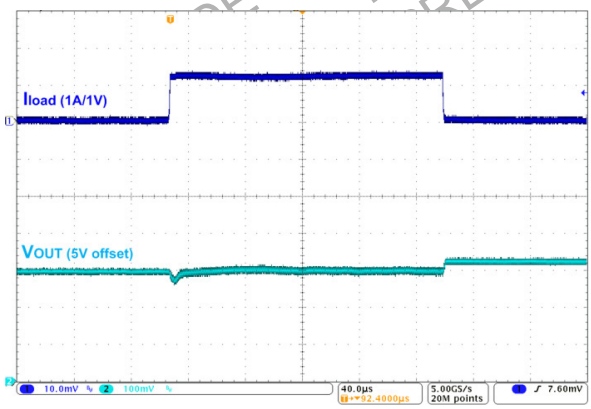


**Figure 15. Load Transient, 0 <–>120 mA, 1 μs Edge**

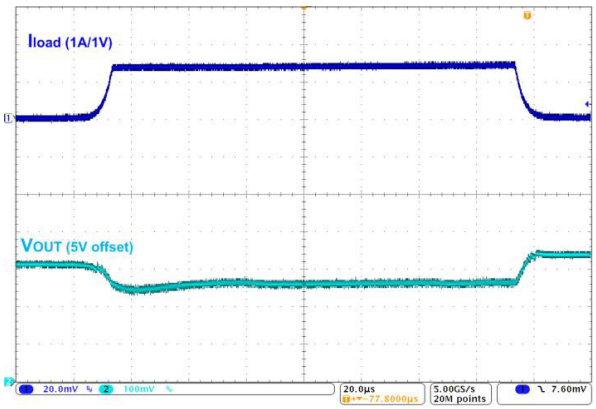


**Figure 16. Load Transient, 0 <–> 285 mA, 8 μs Edge**



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## TYPICAL PERFORMANCE CHARACTERISTICS

(Unless otherwise specified; $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.25 V, $T_A$ = 25°C, and circuit and components according to Figure 1.)

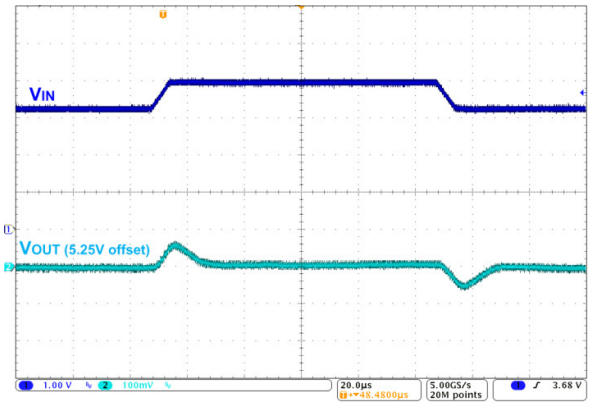


**Figure 17. Line Transient, 3.2 <–> 3.9 $V_{IN}$, 7 µs Edge, 120 mA Load**

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## FUNCTIONAL DESCRIPTION

FAN48611 is a synchronous boost regulator, typically operating at 2.5 MHz in Continuous Conduction Mode (CCM), which occurs at moderate to heavy load current and low $V_{IN}$ voltage.

**Table 2. OPERATING MODES**

| Mode | Description | Invoked When: |
|---|---|---|
| LIN | Linear Startup | $V_{IN} > V_{OUT}$ |
| SS | Boost Soft−Start | $V_{IN} < V_{OUT} < V_{OUT(TARGET)}$ |
| BST | Boost Mode | $V_{OUT} = V_{OUT(TARGET)}$ |

### Boost Mode Regulation

The current−mode modulator achieves excellent transient response and smooth transitions between CCM and DCM operation. During CCM operation, the device maintains a switching frequency of about 2.5 MHz. In light−load operation (DCM), frequency is naturally reduced to maintain high efficiency.

### Startup and Shutdown

When EN is LOW, all bias circuits are off and the regulator enters Shutdown Mode. During shutdown, current flow is prevented from VIN to VOUT, as well as reverse flow from VOUT to VIN. It is recommended to keep load current draw below 50 mA until the device successfully executes startup. Table 3 describes the startup sequence.

**Table 3. BOOST STARTUP SEQUENCE**

| Start Mode | Entry | Exit | End Mode | Timeout (μs) |
|---|---|---|---|---|
| LIN1 | $V_{IN} > V_{UVLO}$, EN=1 | $V_{OUT} > V_{IN}$−300 mV | SS | – |
| | | TIMEOUT | LIN2 | 512 |
| LIN2 | LIN1 Exit | $V_{OUT} > V_{IN}$−300 mV | SS | – |
| | | TIMEOUT | FAULT | 1024 |
| SS | LIN1 or LIN2 Exit | $V_{OUT} = V_{OUT(TARGET)}$ | BST | – |
| | | OVERLOAD TIMEOUT | FAULT | 64 |

### LIN Mode

When EN is HIGH and $V_{IN} > V_{UVLO}$, the regulator attempts to bring VOUT within 300 mV of $V_{IN}$ using the internal fixed−current source from VIN (Q2). The current is limited to the $I_{ss}$ set point, which is typically 90 mA. The linear charging current is limited to a maximum of 200 mA to prevent any “brownout” situations where the system voltage drops too low.

During LIN1 Mode, if $V_{OUT}$ reaches $V_{IN}$−300 mV, SS Mode is initiated. Otherwise, LIN1 Mode expires after 512 μs and LIN2 Mode is entered.

In LIN2 Mode, the current source is equal to LIN1 current source $I_{ss}$, typically 90 mA. If $V_{OUT}$ fails to reach $V_{IN}$−300 mV after 1024 μs, a fault condition is declared and the device waits 20 ms ($t_{RST}$) to attempt an automatic restart.

### Soft−Start (SS) Mode

Upon the successful completion of LIN Mode (VOUT ≥ $V_{IN}$−300 mV), the regulator begins switching with boost pulses current limited to 50% of nominal level.

During SS Mode, if VOUT fails to reach regulation during the SS ramp sequence for more than 64 μs, a fault is declared. If a large $C_{OUT}$ is used, the reference is automatically stepped slower to avoid excessive input current draw.

### Boost (BST) Mode

This is a normal operating mode of the regulator.

### Fault State

The regulator enters Fault State under any of the following conditions:

- $V_{OUT}$ fails to achieve the voltage required to advance from LIN Mode to SS Mode.
- $V_{OUT}$ fails to achieve the voltage required to advance from SS Mode to BST Mode.
- Boost current limit triggers for 2 ms during BST Mode.
- $V_{IN} - V_{OUT} > 300$ mV; this fault can occur only after successful completion of the soft−start sequence.
- $V_{IN} < V_{UVLO}$.

Once a fault is triggered, the regulator stops switching and presents a high−impedance path between VIN and VOUT. After 20 ms, automatic restart is attempted.

### Over−Temperature

The regulator shuts down if the die temperature exceeds 150°C. Restart occurs when the IC has cooled by approximately 20°C.

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## APPLICATION INFORMATION

### Output Capacitance ($C_{OUT}$)

The effective capacitance ($C_{EFF}$ (Note 4)) of small, high−value ceramic capacitors decreases as the bias voltage increases, as illustrated in Figure 18.

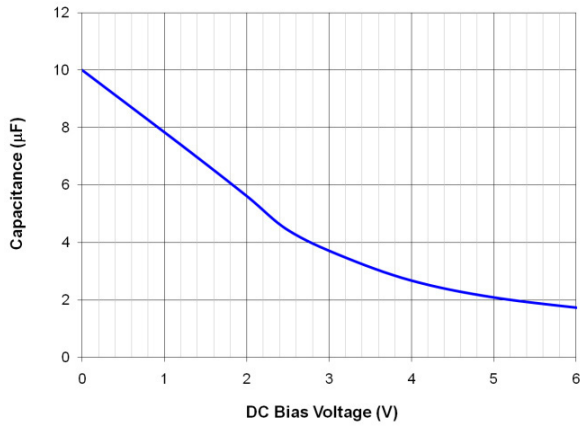


**Figure 18. $C_{EFF}$ for 10 µF, 0402, X5R, 6.3 V−Rated Capacitor (TDK C1005X5R0J106M050BC)**

FAN48611 is guaranteed for stable operation with the minimum value of $C_{EFF}$ ($C_{EFF(MIN)}$) outlined in Table 4.

**Table 4. MINIMUM $C_{EFF}$ REQUIRED FOR STABILITY**

| Operating Conditions | | | $C_{EFF(MIN)}$ (µF) |
|---|---|---|---|
| $V_{OUT}$ (V) | $V_{IN}$ (V) | $I_{LOAD}$ (mA) | |
| 5.25 | 2.7 to 4.8 | 0 to 350 | 6.0 |

4. $C_{EFF}$ varies by manufacturer, capacitor material, and case size.

### Inductor Selection

Recommended nominal inductance value is 1 µH.

The FAN48611 employs valley−current limiting, so peak inductor current can reach 1.2 A for a short duration during overload conditions. Saturation causes the inductor current ripple to increase under high loading, as only the valley of the inductor current ripple is controlled.

### Startup

Input current limiting is active during soft−start, which limits the current available to charge $C_{OUT}$ and any additional capacitance on the $V_{OUT}$ line. If the output fails to achieve regulation within the limits described in the Soft−Start section above, a fault occurs, causing the circuit to shut down. It waits about 20 ms before attempting a restart. If the total combined output capacitance is very high, the circuit may not start on the first attempt, but eventually achieves regulation if no load is present. If a high current load and high capacitance are both present during soft−start, the circuit may fail to achieve regulation and continually attempt soft−start, only to have the output capacitance discharged by the load when in Fault State.

### Output Voltage Ripple

Output voltage ripple is inversely proportional to $C_{OUT}$. During $t_{ON}$, when the boost switch is on, all load current is supplied by $C_{OUT}$.

$$V_{RIPPLE(P-P)} = t_{ON} \cdot \frac{I_{LOAD}}{C_{OUT}} \quad \text{(eq. 1)}$$

and

$$t_{ON} = t_{SW} \cdot D = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad \text{(eq. 2)}$$

therefore:

$$V_{RIPPLE(P-P)} = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \cdot \frac{I_{LOAD}}{C_{OUT}} \quad \text{(eq. 3)}$$

$$t_{SW} = \frac{1}{f_{SW}} \quad \text{(eq. 4)}$$

The maximum $V_{RIPPLE}$ occurs when $V_{IN}$ is minimum and $I_{LOAD}$ is maximum. For better ripple performance, more output capacitance can be added.

### Layout Recommendations

The layout recommendations below highlight various top−copper pours by using different colors.

To minimize spikes at VOUT, $C_{OUT}$ must be placed as close as possible to PGND and VOUT, as shown below.

For best thermal performance, maximize the pour area for all planes other than SW. The ground pour, especially, should fill all available PCB surface area and be tied to internal layers with a cluster of thermal vias.

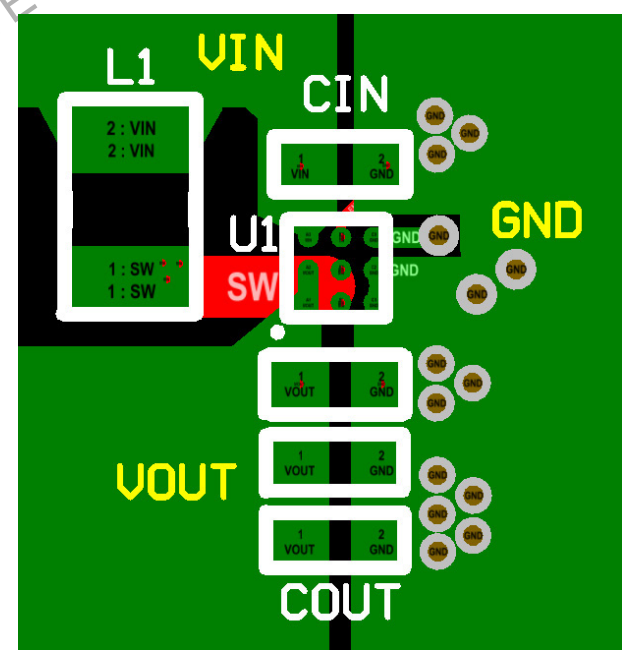


**Figure 19. Layout Recommendation**

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## ORDERING INFORMATION

| Part Number | Device Marking | $V_{OUT}$ | Operating Temperature | Package | Packing Method† |
|---|---|---|---|---|---|
| FAN48611UC53X | KH | 5.25 V | −40 to 85°C | WLCSP9 1.215x1.215x0.581 (Pb−Free and Halide Free) | 3000 / Tape and Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

The table below pertains to the Package Information on the following page.

**Table 5. PRODUCT−SPECIFIC PACKAGE DIMENSIONS**

| D | E | X | Y |
|---|---|---|---|
| 1.215 ±0.030 mm | 1.215 ±0.030 mm | 0.2075 mm | 0.2075 mm |

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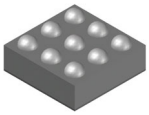
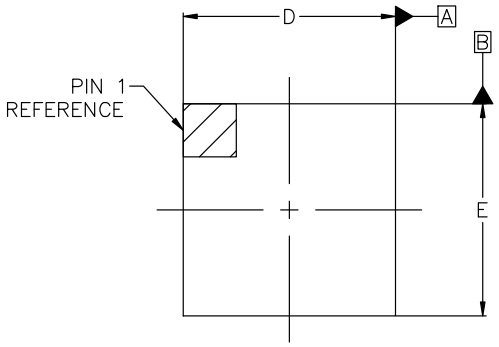
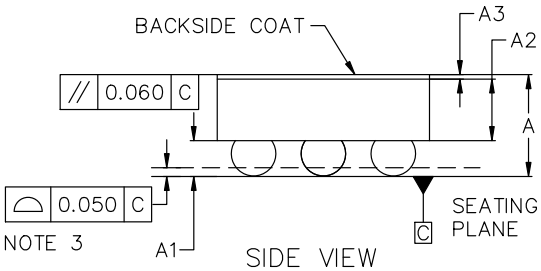


**WLCSP−9 1.22x1.22x0.38, 0.40P**
CASE 567QW
ISSUE C

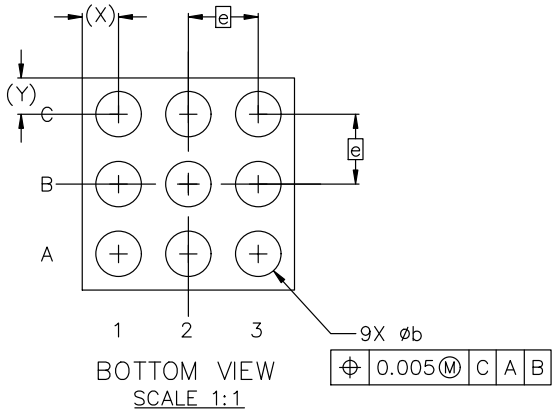
DATE 11 MAY 2026




TOP VIEW
SCALE 1:1




SIDE VIEW
SCALE 1:1

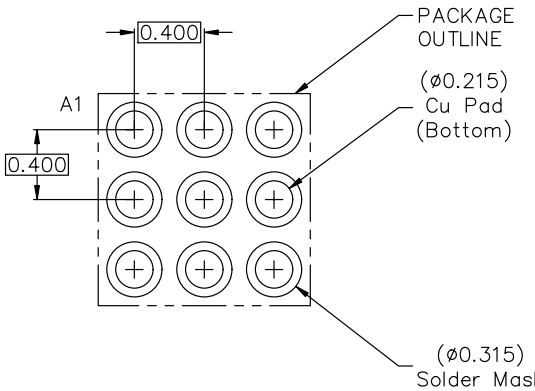



BOTTOM VIEW
SCALE 1:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.542 | 0.581 | 0.620 |
| A1 | 0.183 | 0.203 | 0.223 |
| A2 | 0.335 | 0.353 | 0.371 |
| A3 | 0.022 | 0.025 | 0.027 |
| b | 0.240 | 0.260 | 0.280 |
| D | 1.185 | 1.215 | 1.245 |
| E | 1.185 | 1.215 | 1.245 |
| e | 0.400 BSC | | |
| X | 0.208 REF. | | |
| Y | 0.208 REF. | | |




RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| | | |
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