IS31LT3948

PFM MODE BOOST LED DRIVER WITH THE EXTERNAL NMOS

February 2015

GENERAL DESCRIPTION

The IS31LT3948 is a PFM step-up DC-DC converter designed for driving the white LED arrays for large size LCD panel backlighting applications. It can deliver stable constant output current from a few milliamps up to 2A, programmed via an external resistor.

The IS31LT3948 utilizes a control scheme in which the output is automatically adjusted to the optimum output voltage for the system, maximizing the efficiency. Furthermore, the control scheme is inherently stable removing the need to provide additional loop compensation.

The device features external PWM dimming, which allows the flexible control of the back-lighting luminance.

The IS31LT3948 has a wide input voltage range from 5V to 100V (Note). An integrated OVP circuit protects the chip and the system even under no-load conditions.

The chip is assembled in SOP-8 package. It operates from 5V to 100V over two temperature ranges of -40°C to +85°C and -40°C to +125°C.

Note: The IS31LT3948 has an internal 5V shunt regulator connected to the VCC pin. A dropping resistor must be connected between the VCC pin and VIN to limit current flow. VIN voltages above 100V are allowed but care must be taken to ensure that the output voltage remains greater than VIN, and that the NMOS voltage rating is sufficiently large.

FEATURES

- Wide input voltage range: 5V~100V
- Constant current output limited only by external component selection (Note)
- No loop compensation required
- Internal over-voltage protection
- Internal over-temperature protection
- Operating temperature range -40°C to +85°C (IS31LT3948-GRLS2-TR)
- Operating temperature range -40°C to +125°C (IS31LT3948-GRLS4-TR)
- SOP-8 package

Note: The maximum output current is determined by V_{OUT}/V_{IN} ratio as well as the external components. If output current and V_{OUT}/V_{IN} ratio is high, high current components of inductor and NMOS are needed.

APPLICATIONS

- TV monitor backlighting
- Notebook
- Automotive
- Street lamp
- LED lighting

TYPICAL APPLICATION CIRCUIT

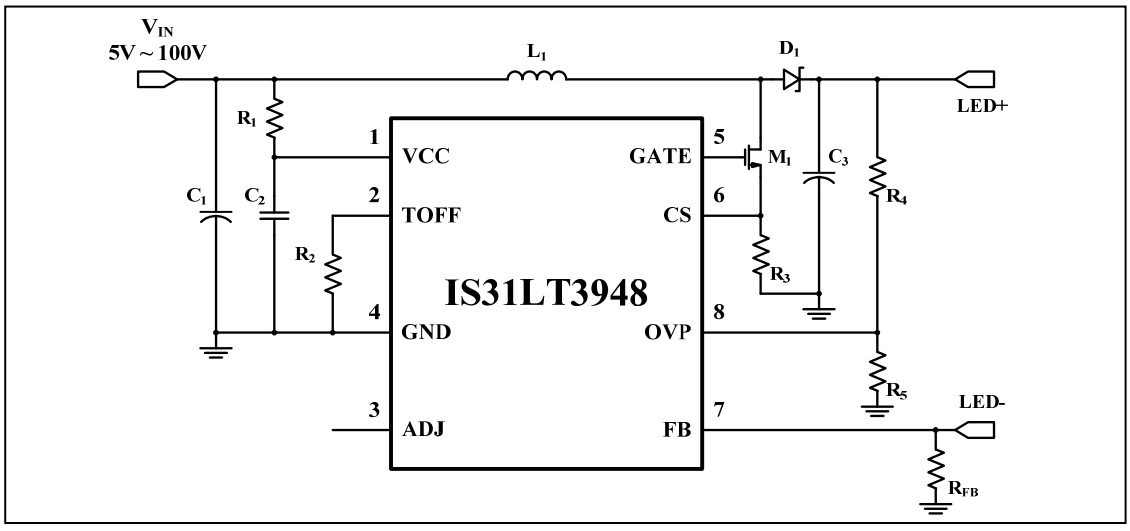
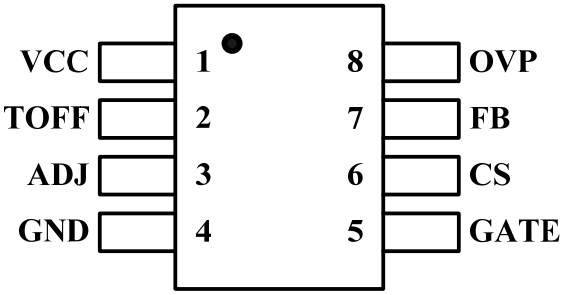


Figure 1 Typical Application Circuit

PIN CONFIGURATIONS

Package	Pin Configuration (Top View)
SOP-8	

PIN DESCRIPTIONS

No.	Pin	Description
1	VCC	Positive power supply input pin. Internally clamped at 5V (Typ.).
2	TOFF	Off time setting pin. An external resistor connected to this pin forms an RC discharge path to generate a constant minimum off time of the NMOS.
3	ADJ	Enable and input peak current control pin. Pulled up to 4.5V internally to set V_{CS_TH} =0.24V when ADJ is floating. If V_{ADJ}<0.5V, NMOS will always shutdown. If 0.5≤V_{ADJ}≤2.4V, V_{CS_TH} = V_{ADJ}/10. If V_{ADJ}>2.4V, V_{CS_TH} =0.24V. Note: During the start up (V_{CC} voltage is rising), ADJ must not be connected to low (recommended floating).
4	GND	Ground.
5	GATE	Driver's output for the gate of the external NMOS.
6	CS	Current sense input for the boost, peak current control loop.
7	FB	Feedback voltage input pin. Used to regulate the current of LEDs by keeping V_{FB}=0.3V.
8	OVP	Overvoltage protection input pin, if the voltage of OVP exceed 1V, gate will always shutdown.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31LT3948-GRLS2-TR	SOP-8, Lead-free	2500

Part No. Rules

IS (ISSI Prefix)
31 (Product Family) - Analog and mix signal
LT (Product Type) - Lighting LED driver
3948 (Part Number) - 3948
GR (Package Code) - SOP
L (Solder Type) - Lead-free (RoHS compliant)
S2 (Temperature Grade) - Industrial temperature (-40°C ~ +85°C)
TR (Packing Option) - Tape & Reel

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31LT3948-GRLS4-TR	SOP-8, Lead-free	2500

Part No. Rules

IS (ISSI Prefix)
31 (Product Family) - Analog and mix signal
LT (Product Type) - Lighting LED driver
3948 (Part Number) - 3948
GR (Package Code) - SOP
L (Solder Type) - Lead-free (RoHS compliant)
S4 (Temperature Grade) - Industrial temperature (-40°C ~ +125°C)
TR (Packing Option) - Tape & Reel

ABSOLUTE MAXIMUM RATINGS

VCC to GND	-0.3V to 6.0V
CS, ADJ,GATE,TOFF,OVP,FB	-0.3V to 6.0V
VCC Max. input current	10mA
Maximum operating junction temperature, T_{JMAX}	150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature, $T_A = T_J$	-40°C ~ +85°C, IS31LT3948-GRLS2-TR -40°C ~ +125°C, IS31LT3948-GRLS4-TR
ESD (HBM) ESD (CDM)	2kV 1kV

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=10V, R_{IN}=10kΩ, ADJ floating, T_A=25°C.

○ Parameter range based on T_A = -40°C ~ +125°C (Note 1)

The symbol in the table means these parameters are only available in the above temperature range.

Symbol	Parameter	Conditions	Tem.	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	Supply voltage connected to V_{CC} via a appropriate resistor (Note 2)		5		100	V
V_{CC}	V_{CC} clamp voltage	R_{IN}=10kΩ		4.3	5	5.6	V
			○	4.1	5	5.8	
V_{UVLO}	Undervoltage threshold	V_{CC} rising		2.2	2.7	3.0	V
			○	2.0	2.7	3.2	
V_{UVLO_HYS}	Undervoltage threshold hysteresis				300		mV
I_{CC}	Quiescent supply current	V_{CC}= V_{CC} clamp voltage			400	500	μA
			○		400	700	
	Quiescent supply current when V_{CC} undervoltage	V_{CC}=2.5V			50	75	μA
			○		50	145	
V_{CS_TH}	Peak current sense threshold	V_{ADJ}=5V		215	240	265	mV
			○	202	240	275	
t_{BLANK}	Peak current sense blank interval	V_{CS}=V_{CS_TH}+50mV			500		ns
t_{OFF}	Fixed turn-off interval	R_{EXT}=250kΩ			10		μs

ELECTRICAL CHARACTERISTICS (CONTINUE)

Unless otherwise specified, V_{IN}=10V, R_{IN}=10kΩ, ADJ floating, T_A=25°C.

○ Parameter range based on T_A = -40°C ~ +125°C (Note 1)

The symbol in the table means these parameters are only available in the above temperature range.

Symbol	Parameter	Conditions	Tem.	Min.	Typ.	Max.	Unit
V_{ADJ}	Peak current control low threshold				0.5		V
	Peak current control high threshold				2.4		V
T_{SD}	Thermal shutdown threshold				150		°C
T_{SD_HYS}	Thermal shutdown hysteresis				20		°C
V_{FB_TH}	Feedback voltage threshold	IS31LT3948-GRLS2-TR		290	300	310	mV
		IS31LT3948-GRLS4-TR		292	300	310	
			○	285	300	315	
V_{OVP_TH}	Overvoltage input threshold			0.9	1.0	1.1	V

Note 1: Production testing of the device is performed at 25°C. Functional operation of the device and parameters specified over temperature range, are guaranteed by design, characterization and process control.

Note 2: V_{IN} is the input voltage. When V_{IN}≤5V, connect input voltage directly to V_{CC}. When V_{IN}>5V, input voltage should be connected to V_{CC} pin via an appropriately valued resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

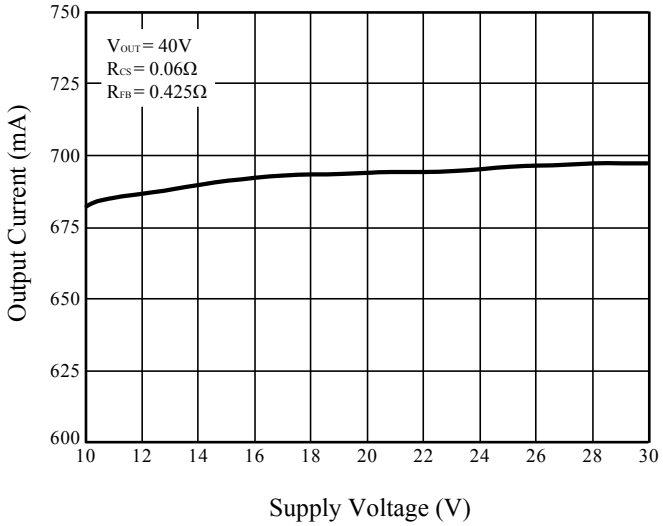


Figure 2 Supply Voltage vs. Output Current

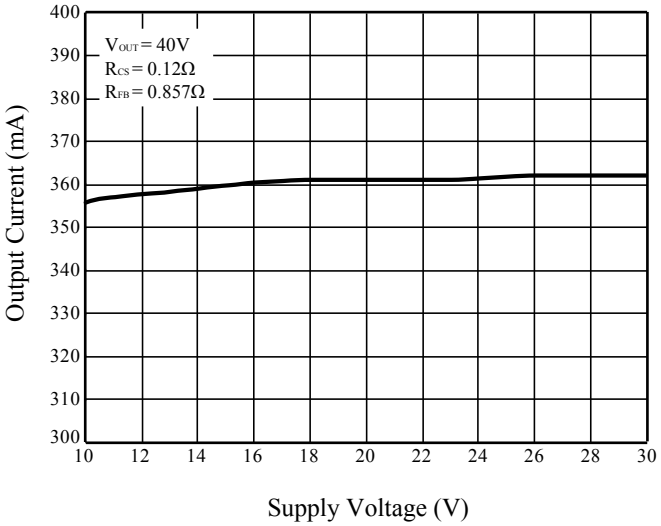


Figure 3 Supply Voltage vs. Output Current

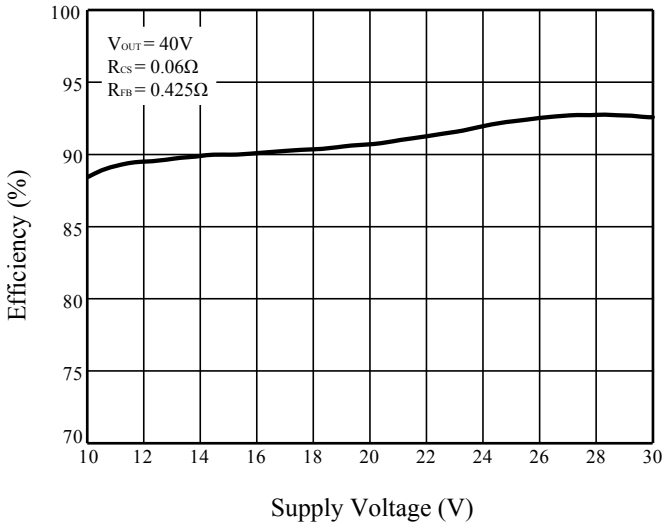


Figure 4 Supply Voltage vs. Efficiency

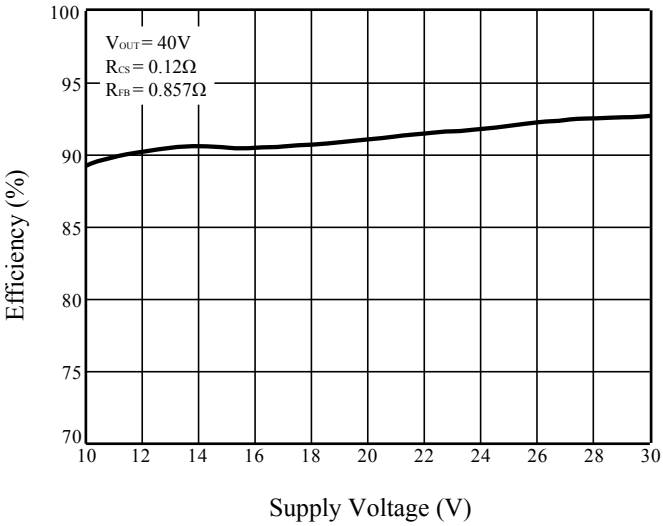


Figure 5 Supply Voltage vs. Efficiency

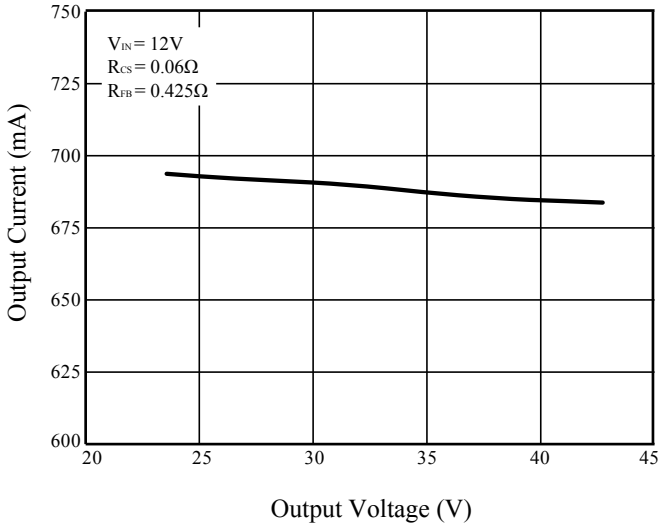


Figure 6 Output Voltage vs. Output Current

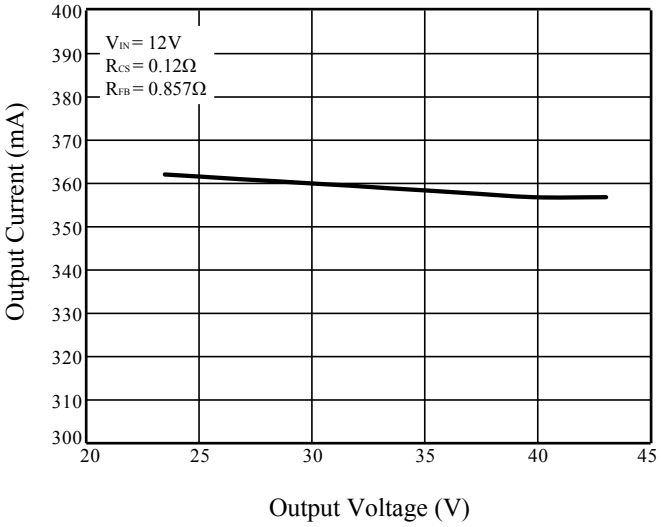


Figure 7 Output Voltage vs. Output Current

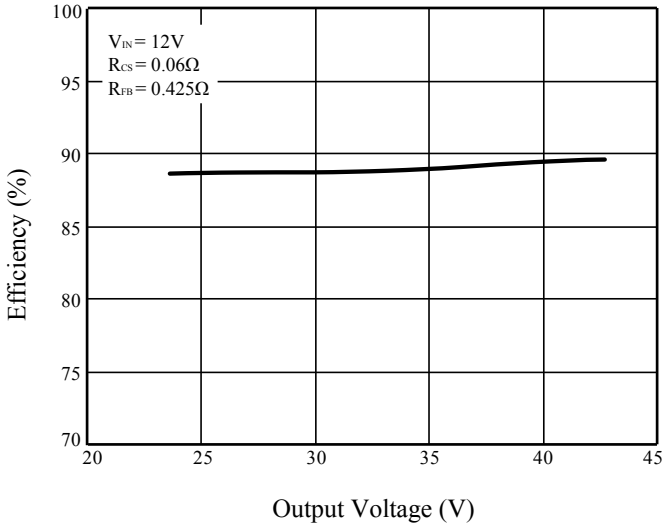


Figure 8 Output Voltage vs. Efficiency

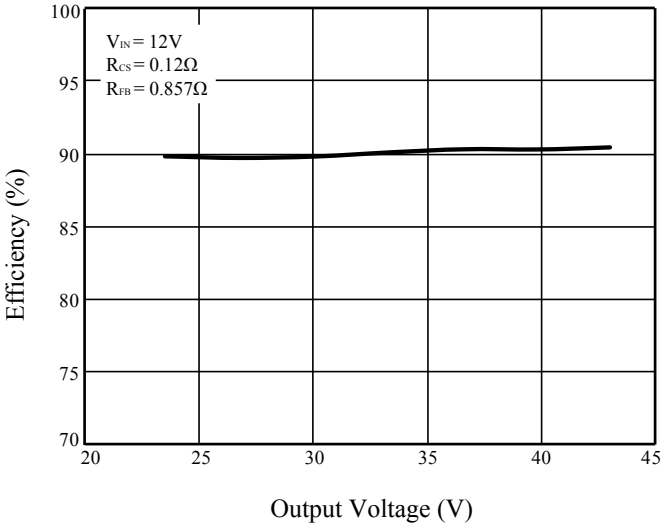


Figure 9 Output Voltage vs. Efficiency

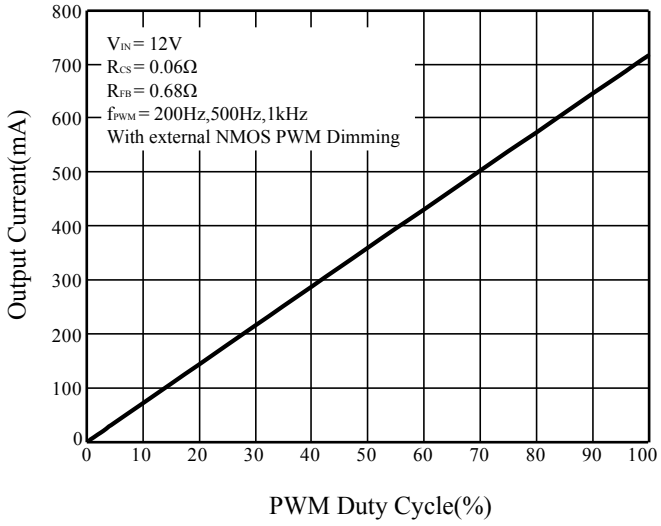


Figure 10 PWM Duty Cycle vs. Output Current

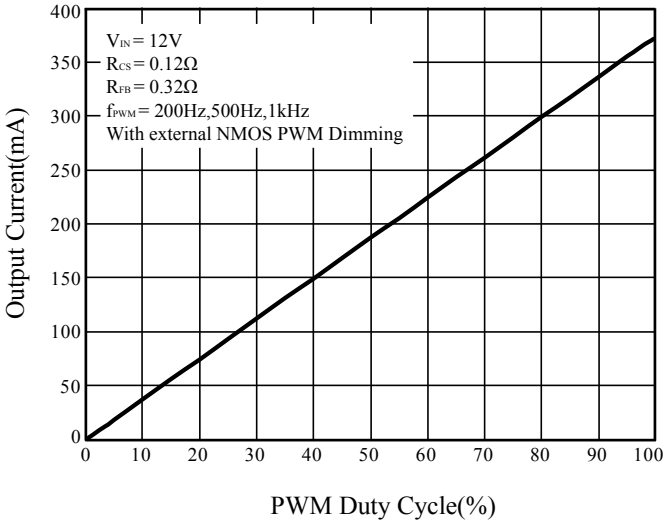


Figure 11 PWM Duty Cycle vs. Output Current

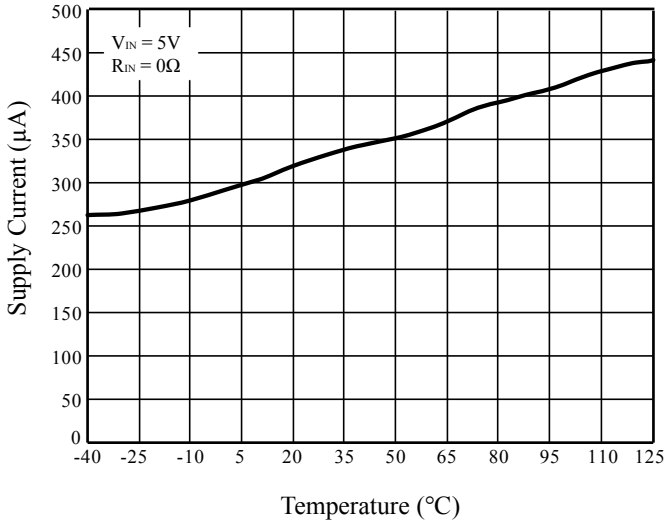


Figure 12 Temperature vs. Supply Current

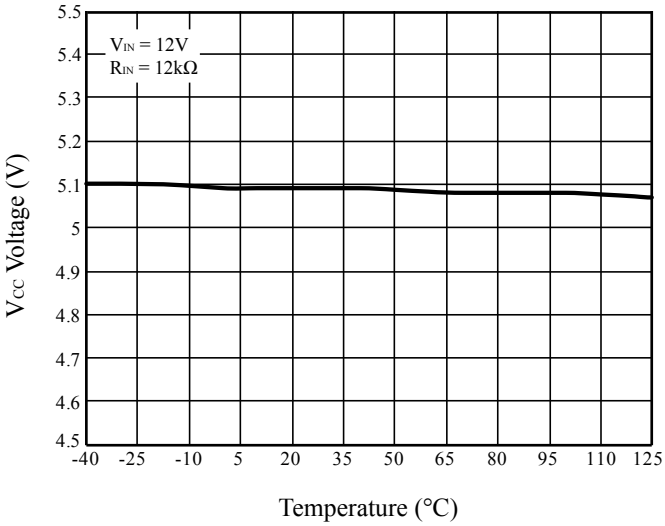


Figure 13 Temperature vs. V_{CC}

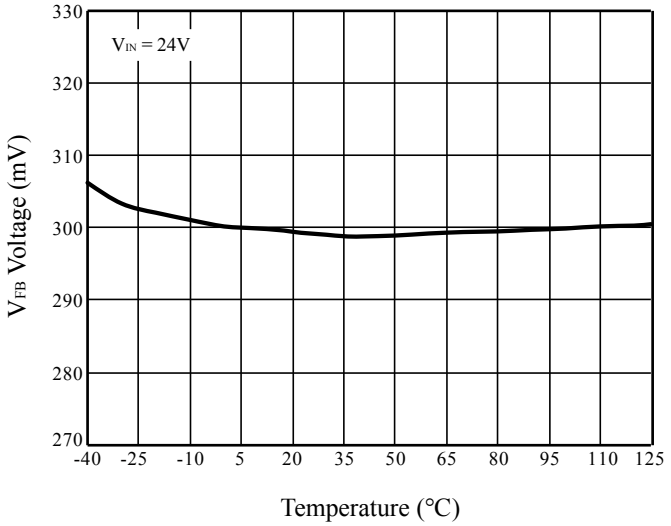


Figure 14 Temperature vs. V_{FB}

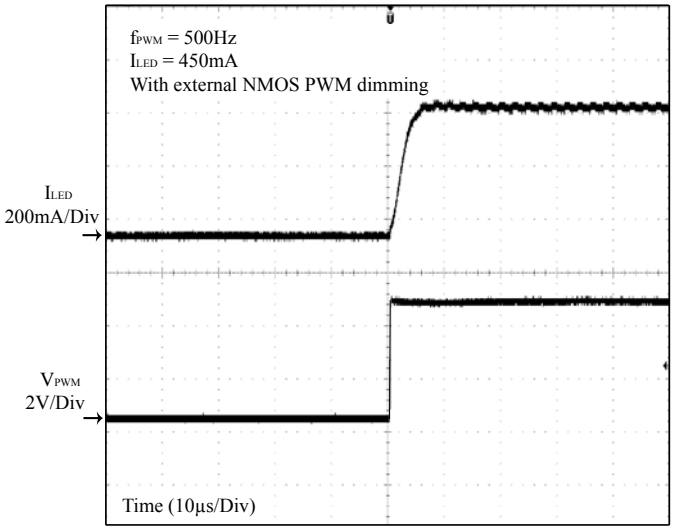


Figure 15 Output Current vs. V_{PWM} on Rising Time

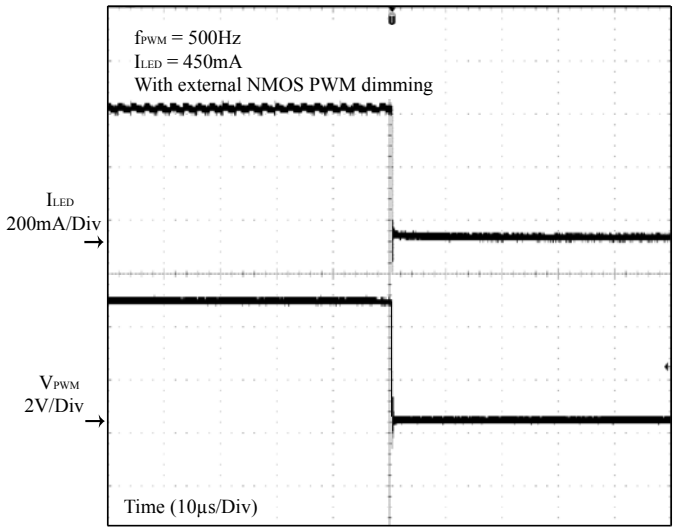
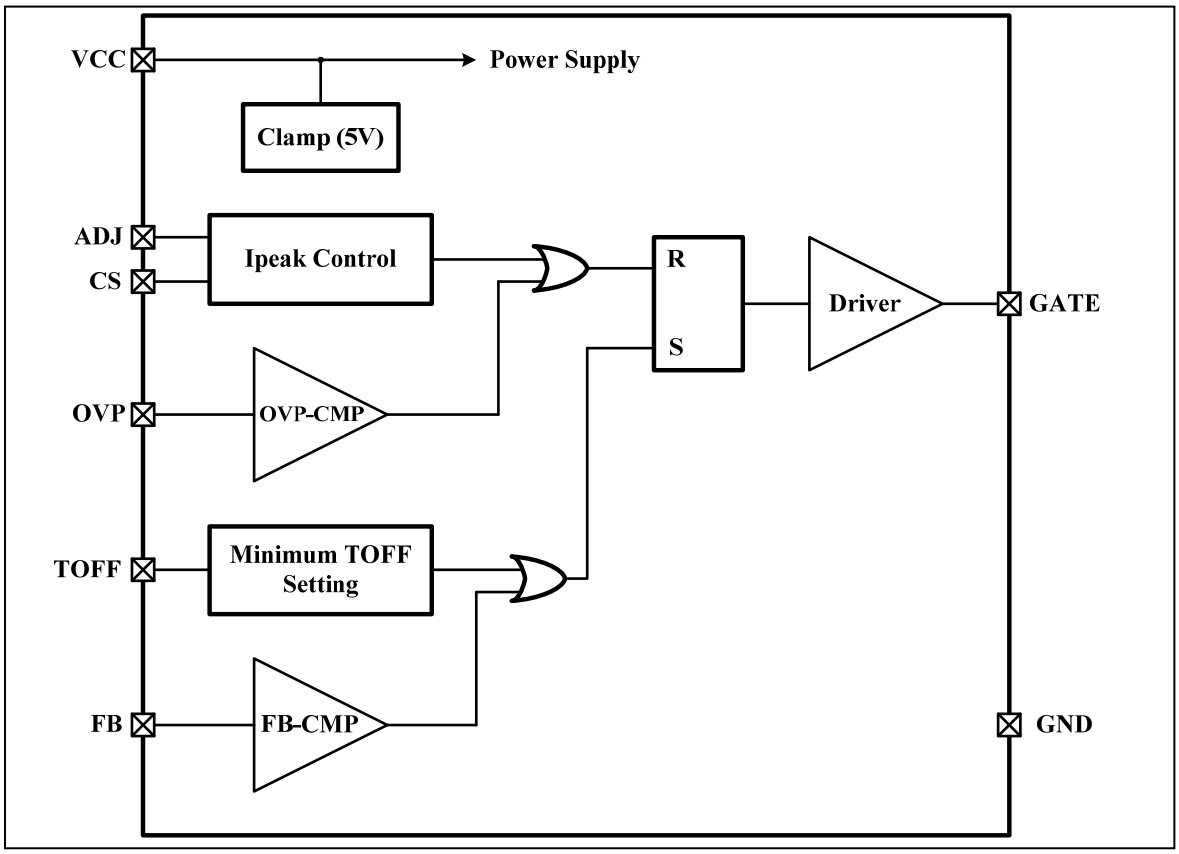


Figure 16 Output Current vs. V_{PWM} on Falling Time

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

INTERNAL 5V REGULATOR

The IS31LT3948 includes an internal shunt regulator of 5V (Typ.) connected to the V_{CC} pin. When the input voltage is higher than 5V, connect V_{CC} to VIN using an appropriately valued, current limiting resistor. The regulator maintains a 5V power supply for the internal NMOS switch gate driver and the internal control circuitry. In applications where the input voltage is 5V, connect the input voltage directly to V_{CC}. When V_{CC} is connected directly to VIN, VIN may not exceed 5V. Bypass the V_{CC} pin using a low ESR capacitor (recommended 10μF ceramic capacitor) to provide a high frequency path to GND.

The current required by IS31LT3948 is 0.4mA (Typ.) plus the switching current of the external switch. The switching frequency of the external NMOS affects the amount of current required, as does the NMOS's gate charge requirement (found on the NMOS data sheet).

$$I_{IN} \approx 0.4mA + Q_G \times f_S \qquad (1)$$

Where f_S is the switching frequency and Q_G is the external NMOS gate charge.

UNDER VOLTAGE LOCKOUT

IS31LT3948 features an under voltage lockout threshold of 2.7V (Typ.) with a hysteresis of 300mV. The chip is disabled when V_{CC} is lower than 2.4V and enabled when V_{CC} exceeds 2.7V.

STEP-UP CONVERTER

IS31LT3948's step-up converter uses a peak current mode topology wherein the CS pin voltage determines the peak current in the inductor of the converter and hence the duty cycle of the GATE switching waveform. The basic loop uses a pulse from an internal oscillator to set an RS flip-flop and turn on the external power NMOS. After the blanking time, the inductor current is sensed during the GATE on period by a sense resistor, R_{CS}, in the source of the external power NMOS. The current increases in the NMOS and inductor until the voltage across the sense resistor reaches the CS threshold, at which time NMOS is turned off. Once the NMOS is turned off, the inductor reverses polarity, providing the voltage boost, and the current of inductor will decrease until the FB pin voltage drops below internal reference voltage and the NMOS is then turned on again. This operation repeats each cycle.

Note, in the case where the FB pin voltage does not exceed the FB reference voltage of 0.3V, such as at start-up, the NMOS will remain off for the programmed minimum t_{OFF} time, then the NMOS is switched on again.

LED CURRENT CONTROL

IS31LT3948 regulates the LED current by sensing the voltage across an external sense resistor in series with the LEDs. The voltage is sensed via the FB pin where the internal feedback reference voltage is 0.3V (Typ.). The LED current can be set from following equation easily.

$$I_{OUT} = \frac{0.3}{R_{FB}} \qquad (2)$$

In order to have an accurate LED current, precision resistors are required (1% is recommended).

SETTING THE OVER VOLTAGE PROTECTION

The open string protection is achieved through the over voltage protection (OVP). In some cases, an LED string failure results in a feedback voltage that is always zero. If this happens, the part then keeps boosting the output voltage higher and higher. If the output voltage reaches the programmed OVP threshold, the protection will be triggered and stop the switching action. To make sure that the circuit functions properly, the OVP setting resistor divider must be set with an appropriate value. The recommended V_{OVP} point is about 1.2 times or 5V (choose the larger one) higher than the output voltage for normal operation.

$$V_{OVP} = V_{OVP\_TH} \times \frac{R_4 + R_5}{R_5} \qquad (3)$$

Where, V_{OVP_TH} is 1V, and V_{OVP} is the output voltage OVP level.

DIMMING CONTROL

There are two methods for dimming.

1) External NMOS PWM dimming:

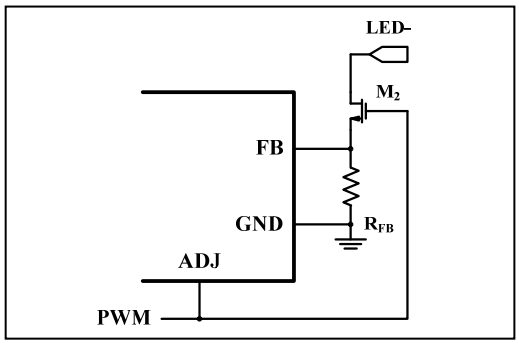


Figure 17 External PWM Dimming

When the PWM input is high (V_H>2.4V), M2 is on and IS31LT3948 operates normally to regulate the output current. When PWM is low logic (V_L<0.5V), M2 is off and IS31LT3948 is shutdown. Using a fixed frequency PWM signal and changing the duty cycle adjusts the average output current. The

recommended 5V PWM frequency is between 200Hz and 1kHz. M2 is recommended to use AP2306. The rising time depends on external component. The minimum on time of PWM signal is recommended to be over the rising time to achieve better dimming rate.

2) RC filter PWM dimming:

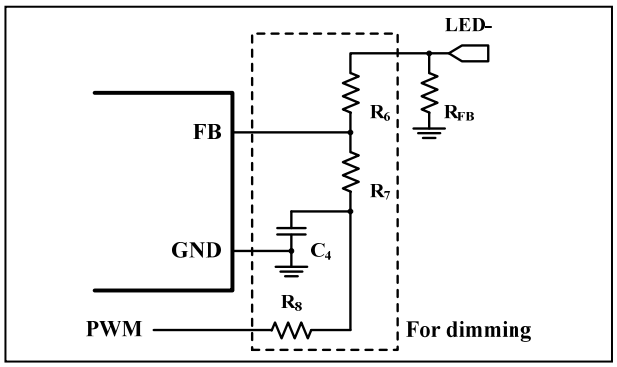


Figure 18 RC PWM Dimming

A filtered PWM signal can be used as an adjustable DC voltage for LED dimming control. The filtered PWM signal becomes DC voltage which is summed together with the FB voltage to regulate the output current. Fix the frequency of the PWM signal and change the duty cycle to adjust the LED current. The LED current can be calculated by the following equation:

$$I_{OUT} = \frac{V_{FB\_TH} - R_6 \times (V_{PWM} \times Duty - V_{FB\_TH})/(R_7 + R_8)}{R_{FB}} \quad (4)$$

The PWM duty cycle is inversely proportional to the LED current. That is, when the PWM signal is 100% duty cycle, the output current is minimum, ideally zero, and when the PWM signal is 0% duty cycle, the output current is maximum.

See details value in the Example section.

Note: When the V_{OUT}/V_{IN} ratio is less than 2, careful consideration must be given to ensure that V_{OUT} remains greater than V_{IN} at the minimum dimming level.

INPUT PEAK CURRENT CONTROL

IS31LT3948 limits the peak inductor current, and thus peak input current through the feedback of R_3 connected from source of NMOS to ground. The required average input current is based on the boost ratio, V_{OUT}/V_{IN}, and the designed value for average LED current. The required average input current can be calculated as:

$$I_{AVG\_IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (5)$$

η: assumed power conversion efficiency (the recommended value is 0.9)

Generally, setting the peak inductor current to 1.5 times the average input current is sufficient to maintain a good regulation of the output current.

$$I_{PEAK\_IN} = 1.5 \times I_{AVG\_IN} = \frac{V_{CS\_TH}}{R_{CS}} \quad (6)$$

V_{CS_TH}: If 0.5<V_{ADJ}<2.4V, V_{CS_TH} = V_{ADJ}/10. If V_{ADJ}>2.4V, V_{CS_TH} =0.24V. ADJ floating, V_{CS_TH}=0.24V.

INPUT CAPACITOR

The input capacitor of the IS31LT3948 will supply the transient input current of the power inductor. Value of 100μF or higher is recommended to prevent excessive input voltage ripple.

SETTING t_{OFF_MIN}

IS31LT3948 operates in a pulsed frequency modulation mode. The boost control loop is a constant off-time architecture. The off time is programmable and set by an external resistor connected between the t_{OFF} pin and GND. In most application, the recommended t_{OFF_MIN} is 1μs. The governing equation for the off time is:

$$t_{OFF\_MIN} = 40 \times 10^{-12} \times R_{EXT} \quad (7)$$

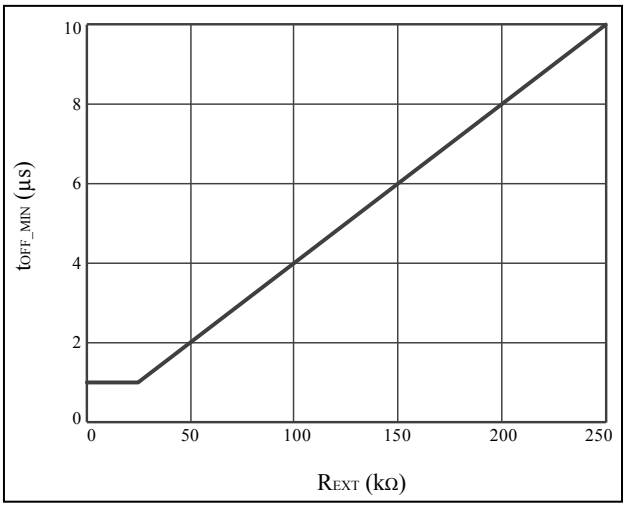


Figure 19 R_{EXT} vs. t_{OFF_MIN}

Note, the minimum t_{OFF_MIN} is 1μs.

INDUCTOR SELECTION

Inductor value directly determines the switching frequency of the converter. To the fixed condition and the larger inductor value the lower switching frequency. The higher frequency will reduce the value of inductor, but will increase the switching loss on NMOS.

The switching frequency can be calculated blow.

Switching frequency:

$$f = 1/(t_{ON} + t_{OFF}) \quad (8)$$

The current ripple in the inductor:

$$I_{RIPPLE} = 2 \times \left(I_{PEAK\_IN} - I_{AVG\_IN} \right) \quad (9)$$

NMOS on time:

$$t_{ON} = \frac{I_{RIPPLE} \times L}{V_{IN} - I_{AVG\_IN} \times (R_L + R_{DS\_ON} + R_{CS})} \quad (10)$$

NMOS off time:

$$t_{OFF} = \frac{I_{RIPPLE} \times L}{V_{OUT} + V_D - V_{IN} - I_{AVG\_IN} \times R_L} \quad (11)$$

Note, the selection of inductor must ensure that the t_{OFF} larger than the t_{OFF_MIN}, or else the converter can not output the required current.

Where:

V_{IN}: Input voltage (V)

V_{OUT}: Output voltage (V)

I_{RIPPLE}: Current ripple in the inductor (A)

L: inductor value (H)

I_{PEAK_IN}: Input peak current (A)

I_{AVG_IN}: Input average current (A)

R_L: Inductor DCR (Ω)

R_{DS_ON}: NMOS on resistance (Ω)

V_D: diode forward voltage at the required load current (V)

The recommended switching frequency: 20kHz < f < 200kHz (Lower than 20kHz will cause audio noice of the inductor and too high frequency will increase the switching loss on NMOS).

To the fixed V_{IN}, V_{OUT}, I_{AVG_IN}, I_{PEAK_IN} and the switching frequency is inversely proportional to the inductor value.

Select an inductor with a rating current over input average current and the saturation current over the calculated peak current. To calculate the worst case inductor peak current, use the minimum input voltage, maximum output voltage, and maximum total LED current. Also ensure that the inductor has a low DCR (copper wire resistance) to minimize I^2R power loss.

OUTPUT CAPACITOR

The output capacitor holds the output current during NMOS on. The capacitor directly impacts the line regulation and the loading regulation.

Low ESR capacitors using at the IS31LT3948 converter output can minimize output ripple voltage and improve output current regulation. For most applications, a 220μF low ESR capacitor will be sufficient. Proportionally lower ripple can be achieved with higher capacitor values.

SCHOTTKY RECTIFIER

The external diode for the IS31LT3948 must be a Schottky diode, with low forward voltage drop and fast switching speed. The diode's average current rating must exceed the application's average output current. The diode's maximum reverse voltage rating must exceed the over voltage protection of the application. For PWM dimming applications, be aware of the reverse leakage of the Schottky diode. Lower leakage current will drain the output capacitor less during PWM low periods, allowing for higher PWM dimming ratios.

Power NMOS Selection

The power NMOS selected should have a V_{DS} rating which exceeds the maximum over voltage protection (OVP) level programmed for the application. The V_{GS_TH} of NMOS should be not higher than 4V. The R_{DS_ON} of the NMOS will determine DC power loss. The DC power loss can be calculated by:

$$P_{loss} = I_{M1}^{\ 2} \times R_{DS\_ON} = \left(\frac{V_{OUT} \times I_{OUT} \times Duty}{V_{IN} \times \eta} \right)^2 \times R_{DS\_ON} \quad (12)$$

The recommended NMOS rating current is 5 times (or higher) to the input peak current (I_{PEAK_IN}). Be aware of the power dissipation within the NMOS and deciding if the thermal resistance of the NMOS package causes the junction temperature to exceed maximum ratings.

PCB LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems.

- Wide traces should be used for connection of the high current loop to minimize the EMI and unnecessary loss.
- The external components ground should be connected to IS31LT3948 ground as short as possible. Especially the R_{FB} ground to IS31LT3948 ground connection should be as short and wide as possible to have an accurate LED current.
- The capacitor C_1, C_2, C_3 should be placed as close as possible to IS31LT3948 for good filtering. Especially the output capacitor C_3 connection should be as short and wide as possible.
- NMOS drain is a fast switching node. The inductor and Schottky diode should be placed as close as possible to the drain and the connection

should be kept as short and wide as possible. Avoid other traces crossing and routing too long in parallel with this node to minimize the noise coupling into these traces. The feedback pin (e.g. CS, FB, OVP) should be as short as possible and routed away from the inductor, the Schottky diode and NMOS. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.

- The thermal pad on the back of NMOS package must be soldered to the large ground plane for ideal power dissipation.

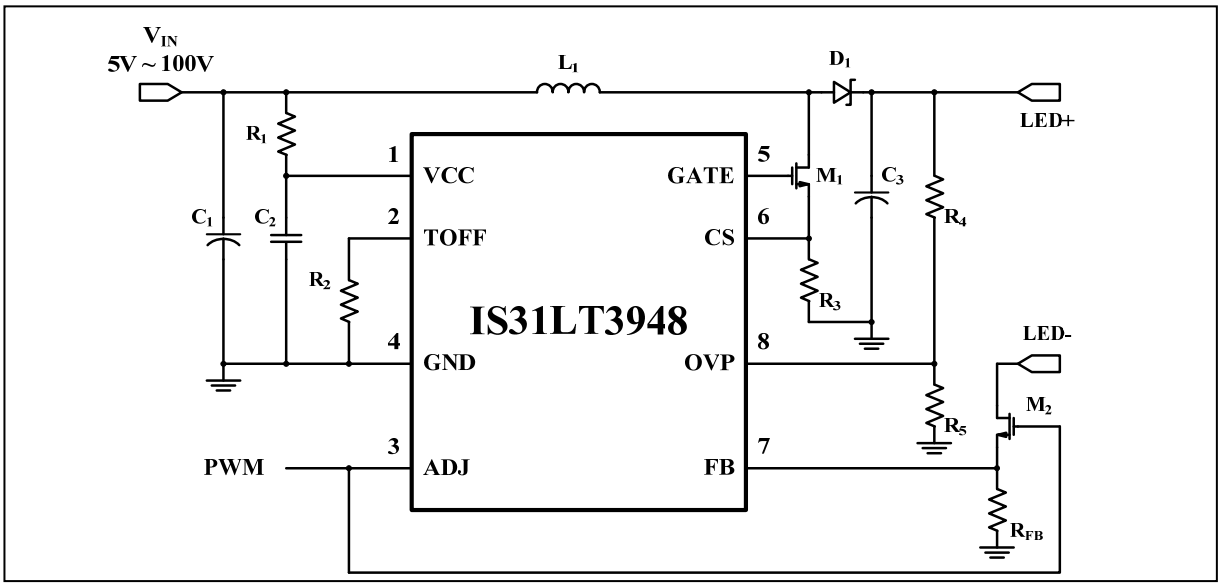


Figure 20 External NMOS PWM Dimming

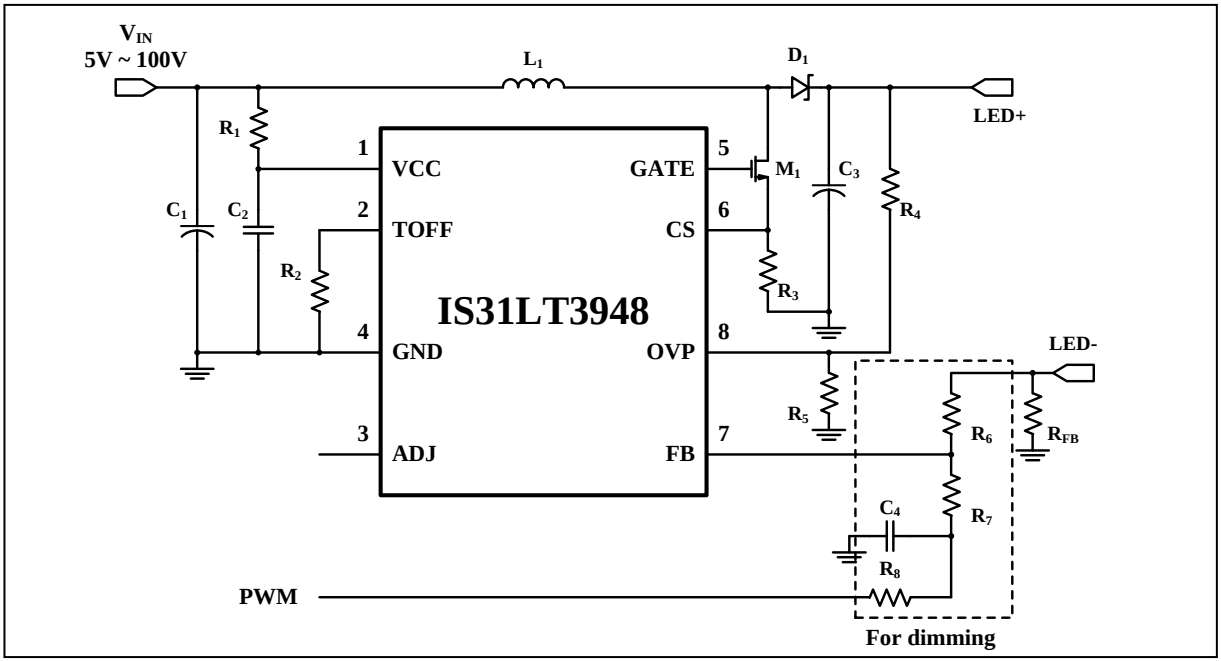


Figure 21 RC Filter PWM Dimming

EXAMPLE:

Input: V_{IN}=12V~24V

Output: I_{OUT}=350mA, V_{OUT}≈30V~40V (9~12LEDs, V_{FB}=3.3V)

To calculate the worst case parameter, use the minimum input voltage, the maximum output voltage, and maximum output current. So choose: V_{IN}=12V, I_{OUT}=350mA, V_{OUT}≈40V (12LEDs, V_{FB}=3.3V)

1. R_1, C_1 and C_2

Assume I_{IN} = 2.5mA,

$$R_1 = \frac{V_{IN\_MIN} - V_{CC}}{I_{IN}} = \frac{12-5}{2.5} = 2.8k\Omega \approx 3k\Omega$$

Note: The maximum VCC input current at highest input voltage must not exceed 10mA.

I_{IN} = (V_{IN_MAX}-V_{CC})/R_1 <10mA

Choose C_1 as 220µF/35V, C_2 as 10µF/16V.

2. R_2 to Set t_{OFF_MIN}

The recommended value is 1µs,

$$t_{OFF\_MIN} = 40 \times 10^{-12} \times R_{EXT} = 1\mu s$$

Choose R_2=24kΩ.

3. R_{FB} to Set Output Current and C_3

$$R_{FB} = \frac{V_{FB\_TH}}{I_{OUT}} \approx 0.86\Omega$$

Choose C_3 as 220µF/63V (Low ESR electrolytic capacitor).

4. R_6, R_7, R_8 and C_4

R_6, R_7 and R_8 can be calculated by:

$$I_{OUT} = \frac{V_{FB\_TH} - R_6 \times (V_{PWM} \times Duty - V_{FB\_TH})/(R_7 + R_8)}{R_{FB}}$$

Take Duty=100%, V_{PWM}=5V and I_{OUT}=0A into the equation, then we have:

$$0 = \frac{0.3 - R_6 \times (5 \times 100\% - 0.3)/(R_7 + R_8)}{0.86}$$

Which simplifies to: $15.66 \times R_6 = R_7 + R_8$

The low-pass filter formed by R_8 and C_4 must have a corner frequency much lower than the PWM frequency. As the corner frequency of the filter decreases, the response time of the LED current to changes in PWM increases. Choose a corner frequency 50 times lower than f_{PWM}.

$$R_8 \times C_4 \geq \frac{50}{2\pi \times f_{PWM}}$$

Assuming f_{PWM} is 200Hz (or higher), and choosing C_4=0.1µF, we find R_8≥400kΩ.

Choose C_4=0.1µF, R_8=400kΩ.

Choose a nominal value for R_7, then compute R_6.

Choose R_7=10kΩ, then R_6=26.2kΩ

Take Duty=0, V_{PWM} = 5V and I_{OUT}=350mA into the equation, then we have:

$$I_{OUT} = \frac{V_{FB\_TH} - R_6 \times (V_{PWM} \times Duty - V_{FB\_TH})/(R_7 + R_8)}{R_{FB}}$$

$$= \frac{0.3 - 26.2 \times (5 \times 0\% - 0.3)/(400 + 10)}{R_{FB}} = 0.35A$$

So R_{FB}=0.91Ω (With the RC filter PWM dimming, the R_{FB} will be different from the no dimming application.)

4. R_3 to Set Input Peak Current

Assume $I_{PEAK\_IN} = 1.5 \times I_{AVG\_IN}$

$$I_{PEAK\_IN} = 1.5 \times I_{AVG\_IN} = 1.5 \times \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

$$= 1.5 \times \frac{40 \times 0.35}{12 \times 0.9} \approx 1.95A$$

η: assumed power conversion efficiency (the recommended value is 0.9).

$$R_{CS} = \frac{V_{CS\_TH}}{I_{PEAK\_IN}} = 0.123\Omega$$

Choose R_3=0.123Ω, I_{PEAK}=1.95A

5. L_1 to Set Frequency

Input average current is

$$I_{AVG\_IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} = 1.3A$$

The current ripple in the inductor:

$$I_{RIPPLY} = 2 \times (I_{PEAK\_IN} - I_{AVG\_IN}) = 1.3A$$

According to t_{OFF} >t_{OFF_MIN}:

$$t_{OFF} = \frac{I_{RIPPLE} \times L}{V_{OUT} + V_D - V_{IN} - I_{AVG\_IN} \times R_L} > 1\mu s$$

This gives L>22µH.

Assuming L=22µH and

$$R_L + R_{DS\_ON} + R_{CS} = 0.4\Omega.$$

$$t_{ON} = \frac{I_{RIPPLE} \times L}{V_{IN} - I_{AVG\_IN} \times (R_L + R_{DS\_ON} + R_{CS})} \approx 2.5\mu s$$

Then the assumed switching frequency:

$$f' = 1/(t_{ON} + t_{OFF}) \approx 285kHz$$

The recommended switching frequency:

20kHz<f<200kHz, according to the switching frequency is inversely proportional to the inductor value, choose L=100μH. Therefore:

$$f = f' \times \frac{22}{100} \approx 63kHz$$

The saturation current of the inductor must exceed the input peak current (I_{PEAK_IN}).

6. R_4, R_5 to Set OVP

Set $V_{OVP} = V_{OUT} + 5V = 45V$

$$V_{OVP} = V_{OVP\_TH} \times \frac{R_4 + R_5}{R_5}$$

Choose R_5=10kΩ, then R_4 = 470kΩ.

7. NMOS M_1 and Diode D_1

$I_{1(NMOS)} > I_{PEAK\_IN}$

$V_{1(NMOS)} > V_{OVP}$

Lower R_{DS_ON} NMOS can improve the converter efficiency. The recommended NMOS rating current is 5 times (or higher) to the input peak current (I_{PEAK_IN}).

Choose 13N10L as M_1.

The average and peak current of diode must exceed the output average current and input peak current. The diode's maximum reverse voltage rating must exceed the over voltage protection of the application.

Choose SS310 as D_1.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

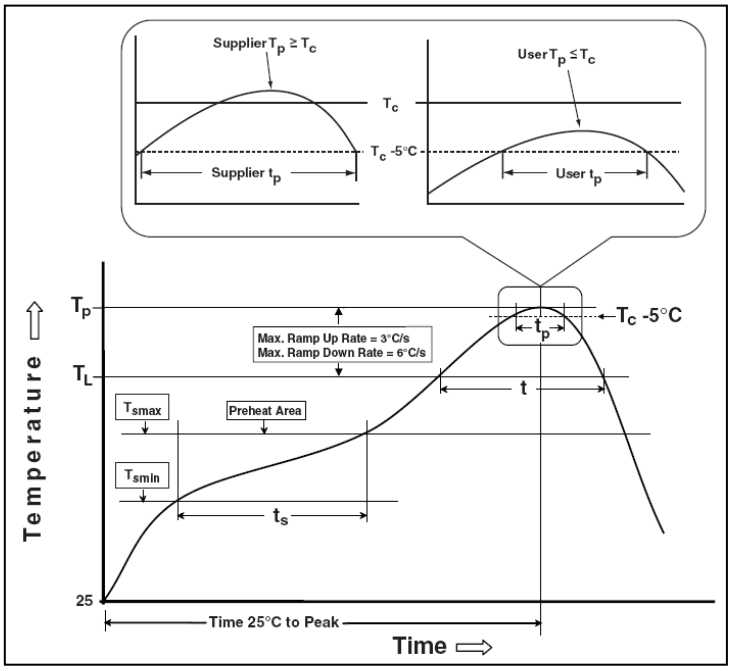
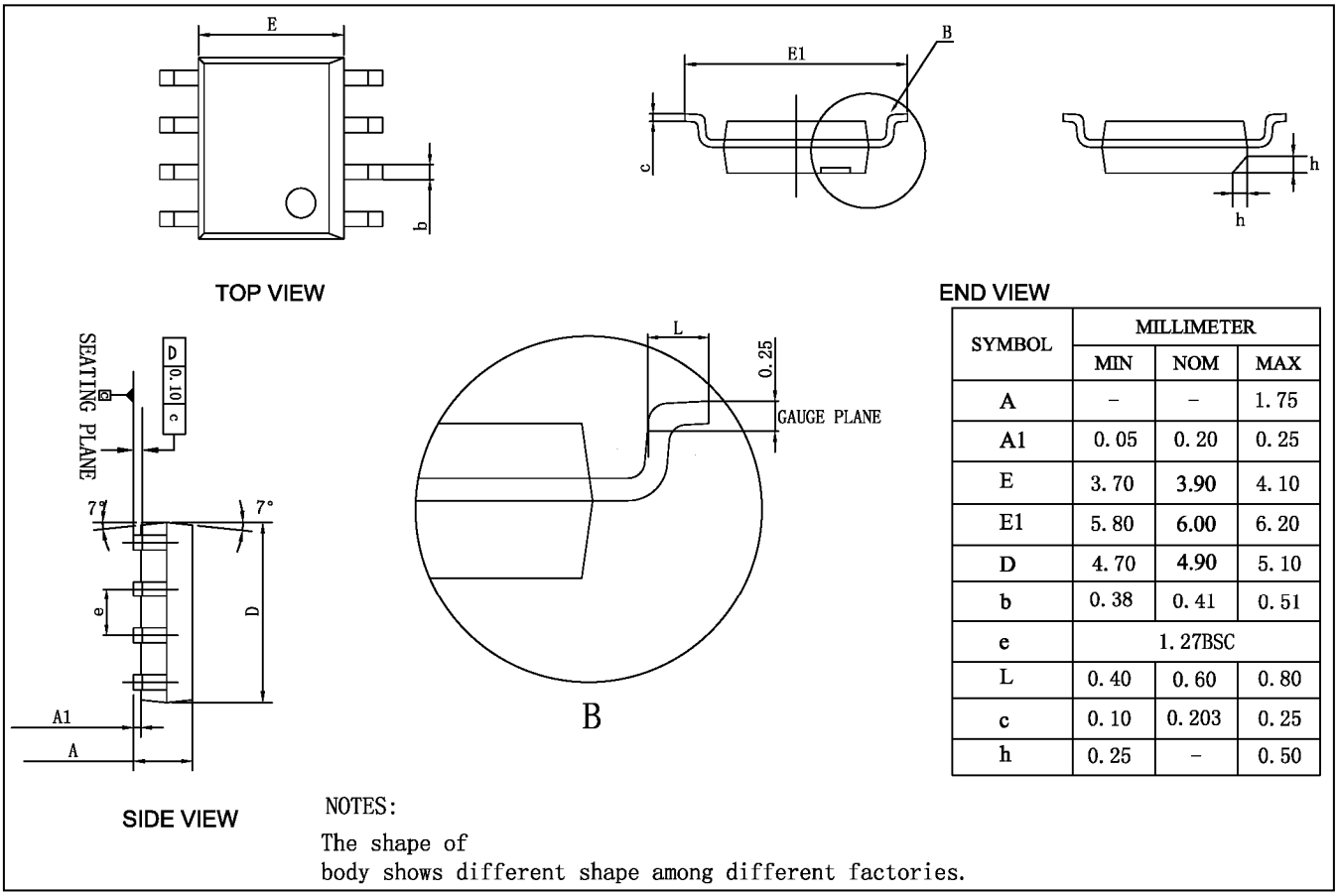


Figure 22 Classification Profile

PACKAGE INFORMATION

SOP-8

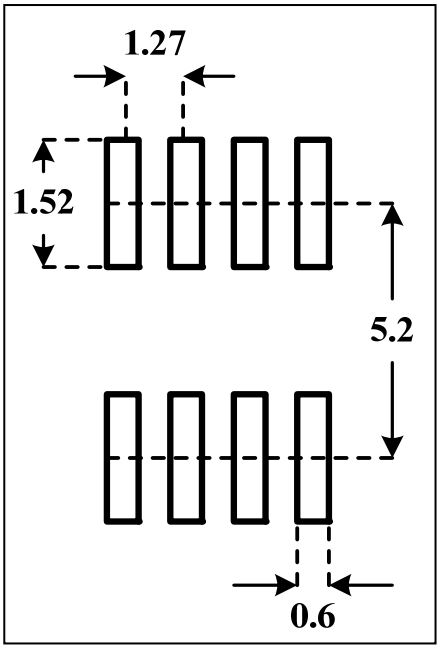


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.75
A1	0.05	0.20	0.25
E	3.70	3.90	4.10
E1	5.80	6.00	6.20
D	4.70	4.90	5.10
b	0.38	0.41	0.51
e	1.27BSC		
L	0.40	0.60	0.80
c	0.10	0.203	0.25
h	0.25	–	0.50

NOTES:

The shape of
body shows different shape among different factories.

LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.