Microprocessor Supervisory Circuit

FEATURES

- Guaranteed Reset Assertion at V_{CC} = 1V
- 1.5mA Maximum Supply Current
- Fast (35ns Max.) Onboard Gating of RAM Chip Enable Signals
- Conditional Battery Backup Extends Battery Life
- 4.65V Precision Voltage Monitor
- Power OK/Reset Time Delay: 200ms
- External Reset Control
- Minimum External Component Count
- 1µA Maximum Standby Current
- Voltage Monitor for Power Fail or Low Battery Warning
- Thermal Limiting
- Performance Specified Over Temperature
- All the LTC695 Features Plus Conditional Battery Backup and External Reset Control

APPLICATIONS

- Critical µP Power Monitoring
- Intelligent Instruments
- Battery-Powered Computers and Controllers
- Automotive Systems

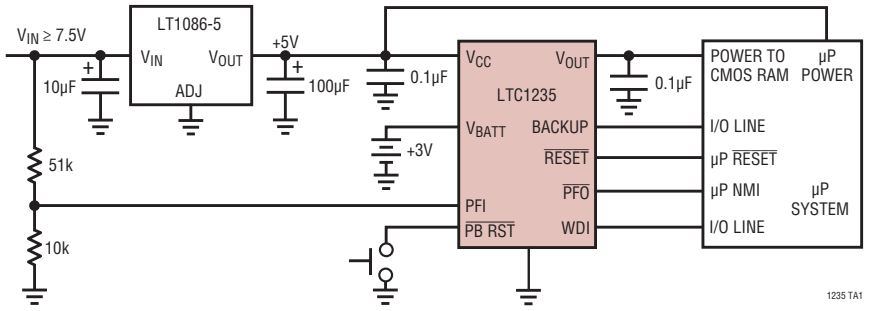
DESCRIPTION

The LTC®1235 provides complete power supply monitoring and battery control functions for microprocessor reset, battery backup, RAM write protection, power failure warning and watchdog timing. The LTC1235 has all the LTC695 features plus conditional battery backup and external reset control. When an out-of-tolerance power supply condition occurs, the reset outputs are forced to active states and the Chip Enable output write-protects external memory. The $\overline{\text{RESET}}$ output is guaranteed to remain logic low with V_{CC} as low as 1V. External reset control is provided by a debounced pushbutton reset input.

The LTC1235 powers the active CMOS RAMs with a charge pumped NMOS power switch to achieve low dropout and low supply current. When primary power is lost, auxiliary power, connected to the battery input pin, provides backup power to the RAMs. The LTC1235 can be programmed by a P signal to either back up the RAMs or not. This extends the battery life in situations where RAM data need not always be saved when power goes down.

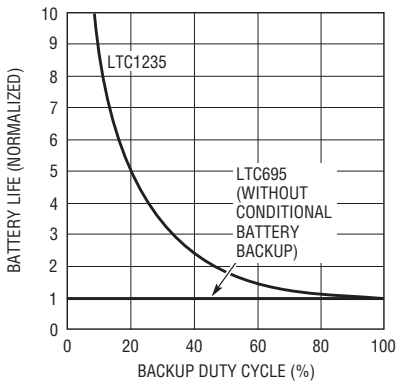
For an early warning of impending power failure, the LTC1235 provides an internal comparator with a user-defined threshold. An internal watchdog timer is also available, which forces the reset pins to active states when the watchdog input is not toggled prior to the time-out period.

TYPICAL APPLICATION



THE LTC1235 EXTENDS BATTERY LIFE BY PROVIDING BATTERY POWER ONLY WHEN REQUIRED TO BACK UP RAM DATA. IT SAVES THE BATTERY WHEN NO DATA BACKUP IS NEEDED. THE µP REQUESTS BACKUP WITH THE BACKUP PIN.

Battery Life vs Backup Duty Cycle



ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Terminal Voltage

V_{CC} ..... –0.3V to 6.0V

V_{BATT} ..... –0.3V to 6.0V

All Other Inputs .....–0.3V to (V_{CC} + 0.3V)

Input Current

V_{CC} 200mA

V_{BATT} 50mA

V_{OUT} Output Current ..... Short Circuit Protected

Power Dissipation 500mW

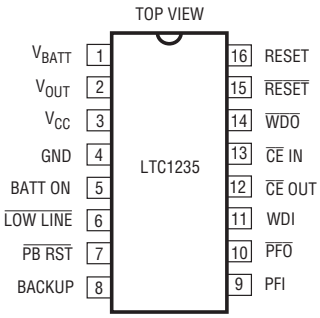
Operating Temperature Range

LTC1235C ..... 0°C to 70°C

Storage Temperature Range..... –65°C to 150°C

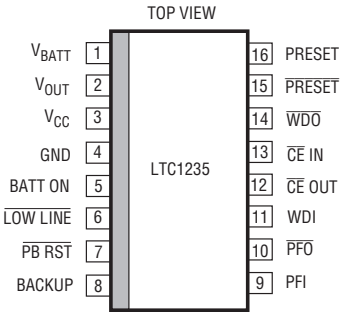
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PIN CONFIGURATION



N PACKAGE
16-LEAD PLASTIC DIP

T_{JMAX} = 110°C, θ_{JA} = 130°C/W



SW PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

CONDITIONS:PCB MOUNT ON FR4 MATERIAL,
STILL AIR AT 25°C COPPER TRACE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1235CN#PBF	LTC1235CN#TRPBF	LTC1235CN	16-Lead Plastic DIP	0°C to 70°C
LTC1235CSW#PBF	LTC1235CSW#TRPBF	LTC1235CSW	16-Lead Plastic SOL	0°C to 70°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

PRODUCT SELECTION GUIDE

	PINS	RESET	WATCHDOG TIMER	BATTERY BACKUP	POWER FAIL WARNING	RAM WRITE PROTECT	PUSH-BUTTON RESET	CONDITIONAL BATTERY BACKUP
LTC1235	**16**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
LTC690	8	X	X	X	X			
LTC691	16	X	X	X	X	X		
LTC694	8	X	X	X	X			
LTC695	16	X	X	X	X	X		
LTC699	8	X	X					
LTC1232	8	X	X				X	

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = Full Operating Range, V_{BATT} = 2.8V, Backup = No Connection, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Backup Switching						
Operating Voltage Range V_{CC} V_{BATT}			 4.75 2.00		 5.50 4.25	 V V
V_{OUT} Output Voltage	I_{OUT} = 1mA I_{OUT} = 50mA	 ● 	V_{CC} – 0.05 V_{CC} – 0.1 V_{CC} – 0.5	V_{CC} – 0.005 V_{CC} – 0.005 V_{CC} – 0.25		V V V
BACKUP Input Threshold	V_{CC} > Reset Voltage Threshold Logic Low Logic High		 2.0		 0.8 	 V V
BACKUP Pullup Current (Note 4)				3		µA
V_{OUT} in Battery Backup Mode (Note 5)	I_{OUT} = 250µA, V_{CC} < V_{BATT}		V_{BATT} – 0.1	V_{BATT} – 0.02		V
V_{OUT} in Battery Saving Mode (Note 5)	V_{CC} < V_{BATT} 1MΩ Pulldown on V_{OUT}			0		V V
V_{CC} Supply Current (excluding I_{OUT})	I_{OUT} ≤ 50mA	 ●		0.6 0.6	1.5 2.5	mA mA
Battery Supply Current in Battery Backup Mode and Battery Saving Mode (Note 5)	V_{CC} = 0V, V_{BATT} = 2.8V	 ●		0.04 0.04	1 5	µA µA
Battery Standby Current (+ = Discharge, – = Charge)	5.5 > V_{CC} > V_{BATT} + 0.2V	 ●	–0.1 –1.0		+0.02 +0.10	µA µA
Battery Switchover Threshold V_{CC} – V_{BATT}	Power-Up Power-Down			70 50		mV mV
Battery Switchover Hysteresis				20		mV
BATT ON Output Voltage (Note 6)	I_{SINK} = 3.2mA				0.4	V
BATT ON Output Short Circuit Current (Note 6)	BATT ON = V_{OUT} Sink Current BATT ON = 0V Source Current		 0.5	35 1	 25	mA µA
Push-Button Reset						
$\overline{PB\ RST}$ Input Threshold	Logic Low Logic High		 2.0		0.8 	V V
$\overline{PB\ RST}$ Input Low Time (Notes 4, 7)		●	40			ms
Reset and Watchdog Timer						
Reset Voltage Threshold		●	4.5	4.65	4.75	V
Reset Threshold Hysteresis				40		mV
Reset Active Time	V_{CC} = 5V	 ●	60 140	200 200	240 280	ms ms
Watchdog Time-out Period	V_{CC} = 5V	 ●	1.2 1.0	1.6 1.6	2.00 2.25	sec sec
Reset Active Time PSRR				1		ms/V
Watchdog Time-out Period PSRR				8		ms/V
Minimum WDI Input Pulse Width	V_{IL} = 0.4V, V_{IH} = 3.5V	●	200			ns
$\overline{RESET}$ Output Voltage At V_{CC} = 1V	I_{SINK} = 10µA, V_{CC} = 1V			4	200	mV
$\overline{RESET}$ and $\overline{LOW\ LINE}$ Output Voltage (Note 6)	I_{SINK} = 1.6mA, V_{CC} = 4.25V I_{SOURCE} = 1µA, V_{CC} = 5V		 3.5		0.4 	V V
RESET and $\overline{WDO}$ Output Voltage (Note 6)	I_{SINK} = 1.6mA, V_{CC} = 5V I_{SOURCE} = 1µA, V_{CC} = 4.25V		 3.5		0.4 	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = Full Operating Range, V_{BATT} = 2.8V, Backup = No Connection, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RESET, $\overline{\text{RESET}}$, $\overline{\text{WDO}}$, $\overline{\text{LOW LINE}}$ Output Short Circuit Current (Note 6)	Output Source Current Output Sink Current		1	3 25	25	µA mA
WDI Input Threshold	Logic Low Logic High		 2.0		0.8	V V
WDI Input Current	WDI = V_{OUT} WDI = 0V	● ●	 –50	4 –8	50	µA µA
Power Fail Detector						
PFI Input Threshold	V_{CC} = 5V	●	1.25	1.3	1.35	V
PFI Input Threshold PSRR				0.3		mV/V
PFI Input Current				±0.01	±25	nA
$\overline{\text{PFO}}$ Output Voltage (Note 6)	I_{SINK} = 3.2mA I_{SOURCE} = 1A		 3.5		0.4	V V
$\overline{\text{PFO}}$ Short Circuit Source Current (Note 6)	PFI = HIGH, $\overline{\text{PFO}}$ = 0V PFI = LOW, $\overline{\text{PFO}}$ = V_{OUT}		1	3 30	25	µA mA
PFI Comparator Response Time (falling)	ΔV_{IN} = –20mV, V_{OD} = 15mV			2		µs
PFI Comparator Response Time (rising) (Note 6)	ΔV_{IN} = 20mV, V_{OD} = 15mV with 10kΩ Pullup			40 8		µs µs
Chip Enable Gating						
$\overline{\text{CE}}$ IN Threshold	V_{IL} V_{IH}		 2.0		0.8	V V
$\overline{\text{CE}}$ IN Pullup Current (Note 4)				3		µA
$\overline{\text{CE}}$ OUT Output Voltage	I_{SINK} = 3.2mA I_{SOURCE} = 3.0mA I_{SOURCE} = 1µA, V_{CC} = 0V		 V_{OUT} – 1.50 V_{OUT} – 0.05		0.4	V V V
$\overline{\text{CE}}$ Propagation Delay	V_{CC} = 5V, CL = 20pF	 ●		20 20	35 45	ns ns
$\overline{\text{CE}}$ OUT Output Short Circuit Current	Output Source Current Output Sink Current			30 35		mA mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: For military temperature range parts, consult the factory.

Note 4: The input pins of $\overline{\text{PB RST}}$, BACKUP and $\overline{\text{CE}}$ IN, have weak internal pullups which pull to the supply when the input pins are floating.

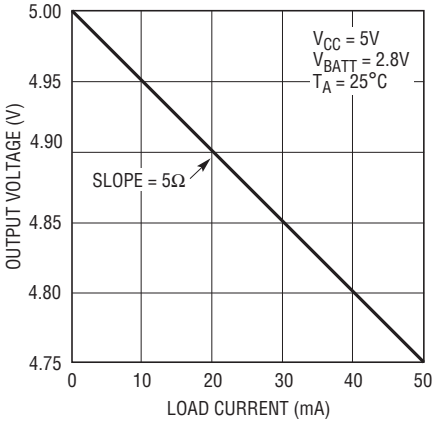
Note 5: The LTC1235 can be programmed either to provide or not to provide battery backup power to the V_{OUT} pin during power failure. The power down condition of V_{OUT} is selected by the logic level of the BACKUP pin which is latched internally when V_{CC} falls through the reset voltage threshold. If the latched logic level of the BACKUP pin is high, V_{OUT} will be in Battery Backup Mode and will be switched to V_{BATT} when V_{CC} falls below V_{BATT}. If the latched logic level of the BACKUP pin is low, V_{OUT} will be in Battery Saving Mode when V_{CC} falls below V_{BATT}.

Note 6: The output pins of BATT ON, $\overline{\text{LOW LINE}}$, $\overline{\text{PFO}}$, $\overline{\text{WDO}}$, $\overline{\text{RESET}}$ and RESET have weak internal pullups of typically 3A. However, external pullup resistors may be used when higher speed is required.

Note 7: The push-button reset input requires an active low signal. Internally, this input signal is debounced and timed for a minimum of 40ms. When this condition is satisfied, the reset outputs go to the active states. The reset outputs will remain in active states for a minimum of 140ms from the moment the push-button reset input is released from logic low level.

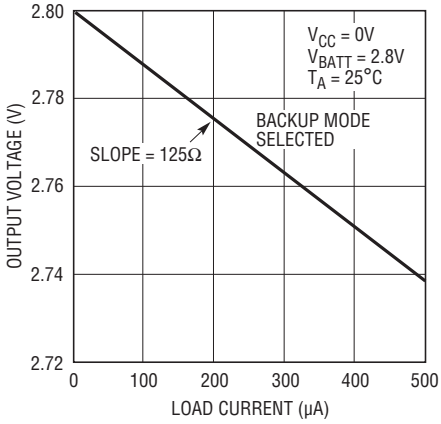
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OUT} vs I_{OUT}



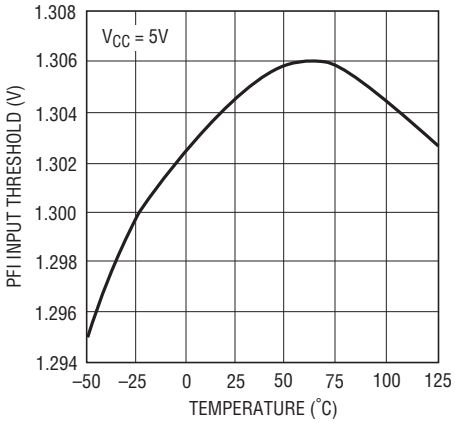
1235 G01

V_{OUT} vs I_{OUT}



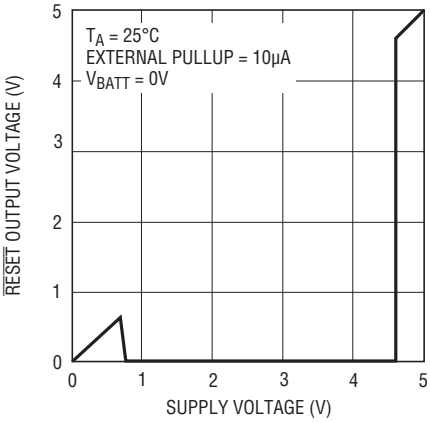
1235 G02

Power Failure Input Threshold vs Temperature



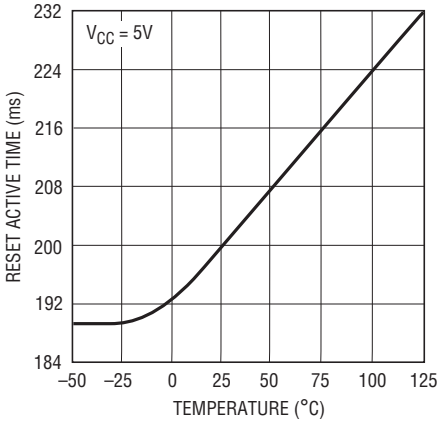
1235 G03

$\overline{RESET}$ Output Voltage vs SupplyVoltage



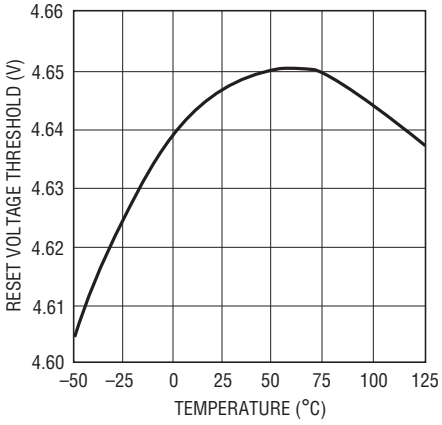
1235 G04

Reset Active Time vs Temperature



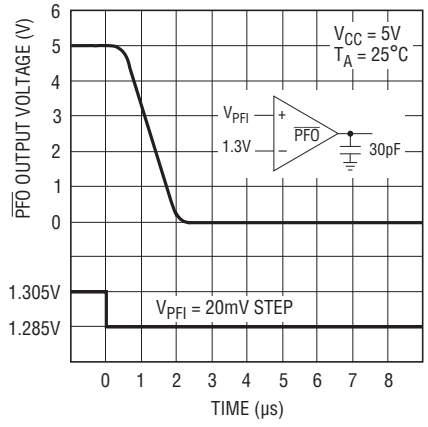
1235 G05

Reset Voltage Threshold vs Temperature



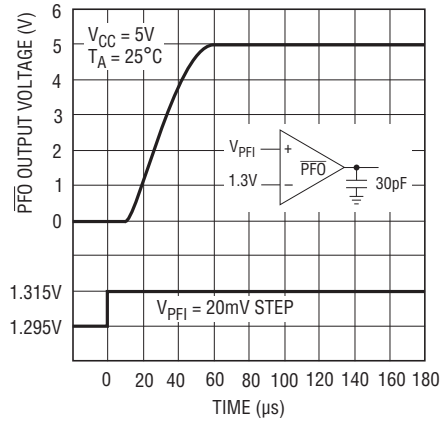
1235 G06

Power Fail Comparator Response Time



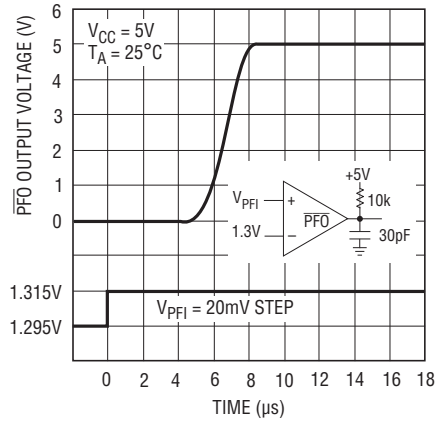
1235 G07

Power Fail Comparator Response Time



1235 G08

Power Fail Comparator Response Time with Pullup Resistor



1235 G09

PIN FUNCTIONS

V_{BATT} (Pin 1): Backup battery input. When V_{CC} falls below V_{BATT}, the status of the BACKUP pin stored in the Memory Logic controls M2. If the status is high, auxiliary power, connected to V_{BATT} is delivered to V_{OUT} through M2. If the status is low, the Memory Logic keeps M2 off and V_{OUT} is in Battery Saving Mode. If backup battery or auxiliary power is not used, V_{BATT} should be connected to GND.

V_{OUT} (Pin 2): Voltage output for backed up memory. Bypass with a capacitor of 0.1µF or greater. During normal operation, V_{OUT} obtains power from V_{CC} through an NMOS power switch, M1, which can deliver up to 50mA and has a typical on resistance of 5Ω. When V_{CC} is lower than V_{BATT}, the status of the BACKUP pin stored in Memory Logic controls M2. If the status is high, the Memory Logic turns on M2 and V_{OUT} is internally switched to V_{BATT} through M2. If the status is low, the Memory Logic keeps M2 off and V_{OUT} is in Battery Saving Mode. If V_{OUT} and V_{BATT} are not used, connect V_{OUT} to V_{CC}.

V_{CC} (Pin 3): +5V supply input. The V_{CC} pin should be bypassed with a 0.1µF capacitor.

GND (Pin 4): Ground pin.

BATT ON (Pin 5): Battery on logic output from comparator C2. BATT ON goes low when V_{OUT} is internally connected to V_{CC}. The output typically sinks 35mA and can provide base drive for an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}. BATT ON goes high when V_{CC} falls below V_{BATT}, if the status of the BACKUP pin stored in Memory Logic is high and V_{OUT} is switched to V_{BATT}.

$\overline{\text{LOW LINE}}$ (Pin 6): Logic output from comparator C1. $\overline{\text{LOW LINE}}$ indicates a low line condition at the V_{CC} input. When V_{CC} falls below the reset voltage threshold (4.65V typically), $\overline{\text{LOW LINE}}$ goes low. As soon as V_{CC} rises above the reset voltage threshold, $\overline{\text{LOW LINE}}$ returns high (see Figure 1). $\overline{\text{LOW LINE}}$ goes low when V_{CC} drops below V_{BATT} (see Table 1).

$\overline{\text{PB RST}}$ (Pin 7): Logic input for direct connection to a push-button. The push-button reset input requires an active low signal. Internally, this input signal is debounced and timed for a minimum of 40ms. When this condition is satisfied, the reset pulse generator forces $\overline{\text{RESET}}$ to active low. The $\overline{\text{RESET}}$ signal will remain active low for a minimum of 140ms from the moment the push-button reset input is released from logic low level. Pulled to V_{CC} with 60k.

Backup (Pin 8): Logic input to control the PMOS switch, M2, when V_{CC} is lower than V_{BATT}. While V_{CC} is falling through the reset voltage threshold, the status of the BACKUP pin (logic low or logic high) is latched in Memory Logic and used to turn on or off M2 when V_{CC} is below V_{BATT}. If the latched status of the BACKUP pin is high, the Memory Logic turns on M2 when V_{CC} falls to 50mV greater than V_{BATT}. If the latched status of the BACKUP pin is low, the Memory Logic keeps M2 off even after V_{CC} falls below V_{BATT}. If the BACKUP pin is left floating it will be pulled high by an internal pullup and the LTC1235 will provide battery backup when V_{CC} falls.

PFI (Pin 9): Power Failure Input. PFI is the noninverting input to the Power Fail Comparator, C3. The inverting input is internally connected to a 1.3V reference. The Power Failure Output remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. Connect PFI to GND or V_{OUT} when C3 is not used.

$\overline{\text{PFO}}$ (Pin 10): Power Failure Output from C3. $\overline{\text{PFO}}$ remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. When V_{CC} is lower than V_{BATT}, C3 is shut down and $\overline{\text{PFO}}$ is forced low.

WDI (Pin 11): Watchdog Input, WDI, is a three level input. Driving WDI either high or low for longer than the watchdog time-out period, forces both $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$ low. Floating WDI disables the Watchdog Timer. The timer resets itself with each transition of the Watchdog Input (see Figure 11).

$\overline{\text{CE}}$ OUT (Pin 12): Logic output from the Chip Enable gating circuit. When V_{CC} is above the reset voltage threshold, $\overline{\text{CE}}$ OUT is a buffered replica of $\overline{\text{CE}}$ IN. When V_{CC} is below the reset voltage threshold $\overline{\text{CE}}$ OUT is forced high (see Figure 6).

$\overline{\text{CE}}$ IN (Pin 13): Logic input to the Chip Enable gating circuit. $\overline{\text{CE}}$ IN can be derived from microprocessor's address line and/or decoder output. See Applications Information Section and Figure 6 for additional information.

$\overline{\text{WDO}}$ (Pin 14): Watchdog logic output. When the watchdog input remains either high or low for longer than the watchdog time-out period, $\overline{\text{WDO}}$ goes low. $\overline{\text{WDO}}$ is set

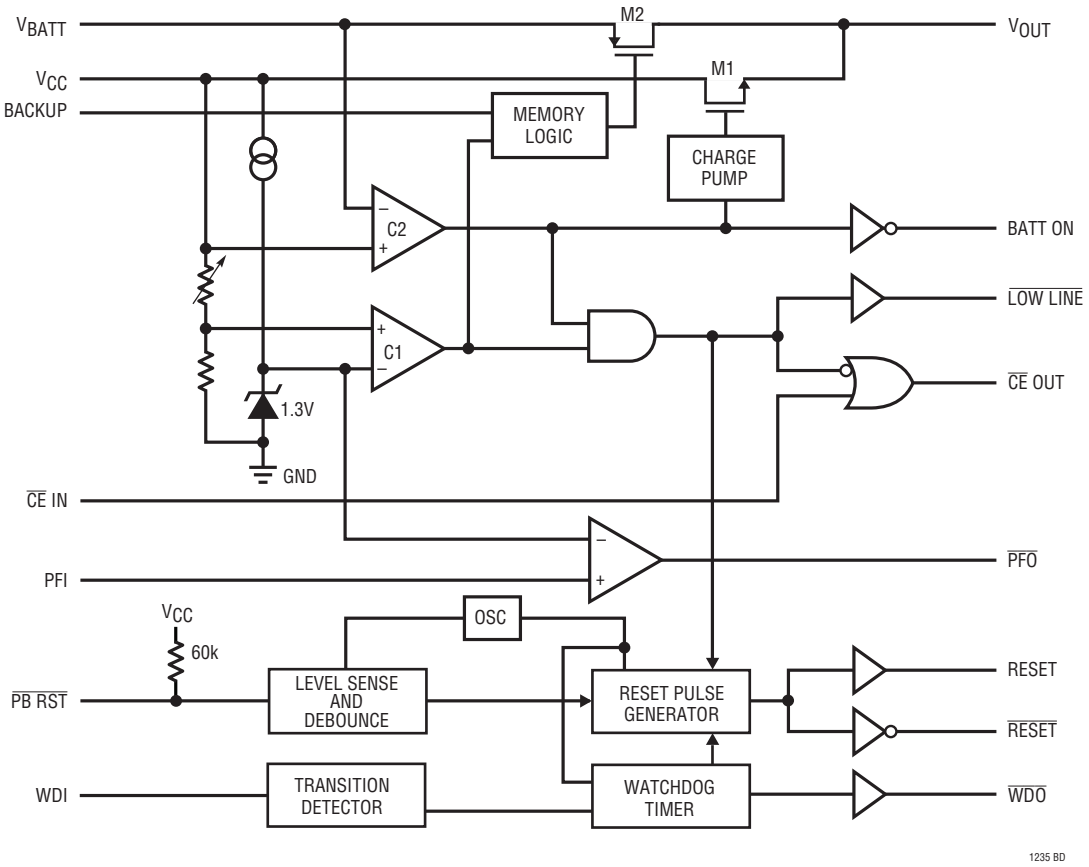
PIN FUNCTIONS

high when ever there is a transition on the WDI pin, or LOW LINE goes low. The watchdog timer can be disabled by floating WDI (see Figure 11).

RESET (Pin 15): Logic output for µP reset control. The LTC1235 provides three ways to generate µP reset. First, whenever V_{CC} falls below either the reset voltage threshold (4.65V, typically) or V_{BATT}, RESET goes active low. After V_{CC} returns to 5V, the reset pulse generator forces RESET to remain active low for a minimum of 140ms. Second, when the watchdog timer is enabled but not serviced prior to the time-out period, the reset pulse generator also forces RESET to active low for a minimum of 140ms for every time-out period (see Figure 11). Third, when the PB RST pin stays active low for a minimum of 40ms, RESET is forced low by reset pulse generator. The RESET signal will remain active low for a minimum of 140ms from the moment the push-button reset input is released from logic low level.

RESET (Pin 16): RESET is an active high logic output. It is the inverse of RESET.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Power Monitoring

The LTC1235 uses a bandgap voltage reference and a precision voltage comparator C1 to monitor the 5V supply input on V_{CC} (see Block Diagram). When V_{CC} falls below the reset voltage threshold, the reset outputs are forced to active states. The reset voltage threshold accounts for a 5% variation on V_{CC}, so the reset outputs become active when V_{CC} falls below 4.75V (4.65V typical). On power-up, the reset signals are held active states for a minimum of 140ms after the reset voltage threshold is reached to allow the power supply and microprocessor to stabilize. On power-down, the $\overline{\text{RESET}}$ signal remains active low even with V_{CC} as low as 1V. This capability helps hold the microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the $\overline{\text{RESET}}$ signal.

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at V_{CC} pin do not activate the reset outputs. Response time is typically 10µs.

To help prevent mistriggering due to transient loads, V_{CC} pin should be bypassed with a 0.1µF capacitor with the leads trimmed as short as possible.

$\overline{\text{LOW LINE}}$ is the output of the precision voltage comparator C1. When V_{CC} falls below the reset voltage threshold, $\overline{\text{LOW LINE}}$ goes low. $\overline{\text{LOW LINE}}$ returns high as soon as V_{CC} rises above the reset voltage threshold.

Push-Button Reset

The LTC1235 provides an logic input pin for direct connection to a push-button. The push-button reset input, $\overline{\text{PB RST}}$, requires an active low signal. Internally, this input signal is debounced and timed for a minimum of 40ms. When this condition is satisfied, the reset pulse generator forces the reset outputs to active states. The reset signals will remain in active states for a minimum of 140ms from the moment the push-button reset input is released from logic low level (Figure 2).

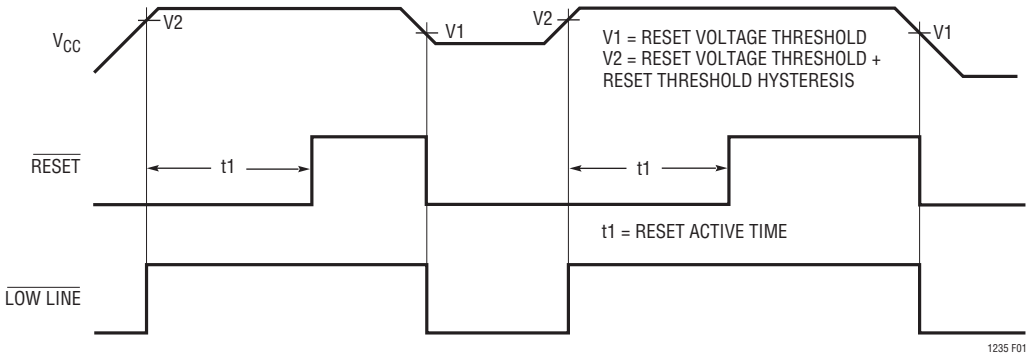


Figure 1. Reset Active Time

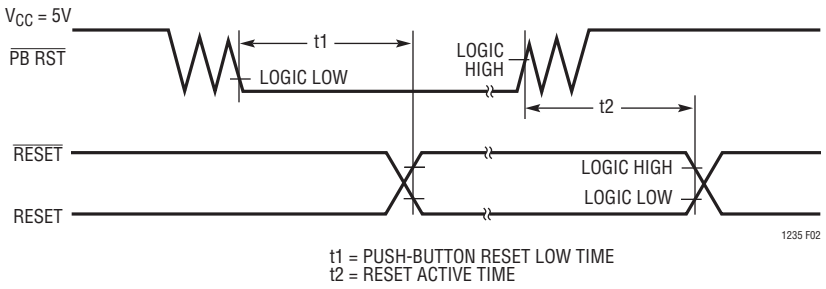


Figure 2. Push-Button Reset

APPLICATIONS INFORMATION

Voltage Output

During normal operation, the LTC1235 uses a charge pumped NMOS power switch to achieve low dropout and low supply current. This power switch can deliver up to 50mA to V_{OUT} from V_{CC} and has a typical on resistance of 5. The V_{OUT} pin should be bypassed with a capacitor of 0.1µF or greater to ensure stability. Use of a larger bypass capacitor is advantageous for supplying current to heavy transient loads.

When operating currents larger than 50mA are required from V_{OUT}, or a lower dropout (V_{CC} - V_{OUT} voltage differential) is desired, the LTC1235 provides BATT ON output to drive the base of external PNP transistor (Figure 3). Another alternative to provide higher current is to connect a high current Schottky diode from the V_{CC} pin to the V_{OUT} pin to supply the extra current.

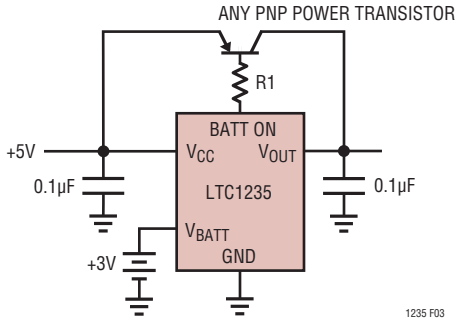


Figure 3. Using BATT ON to Drive External PNP Transistor

The LTC1235 is protected for safe area operation with short circuit limit. Output current is limited to approximately 200mA. If the device is overloaded for a long period of time, thermal shutdown turns the power switch off until the device cools down. The threshold temperature for thermal shutdown is approximately 155°C with about 10°C of hysteresis which prevents the device from oscillating in and out of shutdown.

The PNP switch was not chosen for the internal power switch because it injects unwanted current into the substrate. This current is collected by the V_{BATT} pin in competitive devices and adds to the charging current of the battery which can damage lithium batteries. LTC1235 uses a charge pumped NMOS power switch to eliminate unwanted charging current while achieving low dropout and low supply current. Since no current goes to the substrate, the current collected by V_{BATT} pin is strictly junction leakage.

Conditional Battery Backup

LTC1235 provides an unique feature to either allow V_{OUT} to be switched to V_{BATT} or to disable the CMOS RAM battery backup function when primary power is lost. Disabling the battery backup function is useful in conserving the backup battery's life when the SRAM doesn't need battery backup during long term storage of a computer system, or delivery of the computer system to the end user.

The BACKUP pin (Pin 8) is used to serve this feature on power-down. When V_{CC} is falling through the reset voltage threshold, the status of the BACKUP pin (logic low or logic high) is stored in the Memory Logic (see Block Diagram). If the stored status is logic high and V_{CC} fall to 50mV greater than V_{BATT}, a 125Ω PMOS switch, M2, connects the V_{BATT} input to V_{OUT} and the battery switchover comparator, C2, shuts off the NMOS power switch, M1. M2 is designed for very low dropout voltage (input-to-output differential). This feature is advantageous for low current applications such as battery backup in CMOS RAM and other low power CMOS circuitry. If the stored status is logic low and V_{CC} falls to 50mV greater than V_{BATT}, the Memory Logic keeps M2 off and C2 shuts off M1. V_{OUT} is in Battery Saving Mode (see Figure 4). The supply current in both mode is 1µA maximum.

On power-ups, C2 keeps M1 off before V_{CC} reaches 70mV higher than V_{BATT}. On the first power-up after the battery is replaced (with power off), the status stored in the Memory Logic is undetermined. V_{OUT} could be either in Battery Backup Mode or in Battery Saving Mode. When V_{CC} is 70mV greater than V_{BATT}, M1 connects V_{OUT} to V_{CC}. C2 has typically 20mV of hysteresis to prevent spurious switching when V_{CC} remains nearly equal to V_{BATT} and the status stored in the Memory Logic is high. The response time of C2 is approximately 20µs.

APPLICATIONS INFORMATION

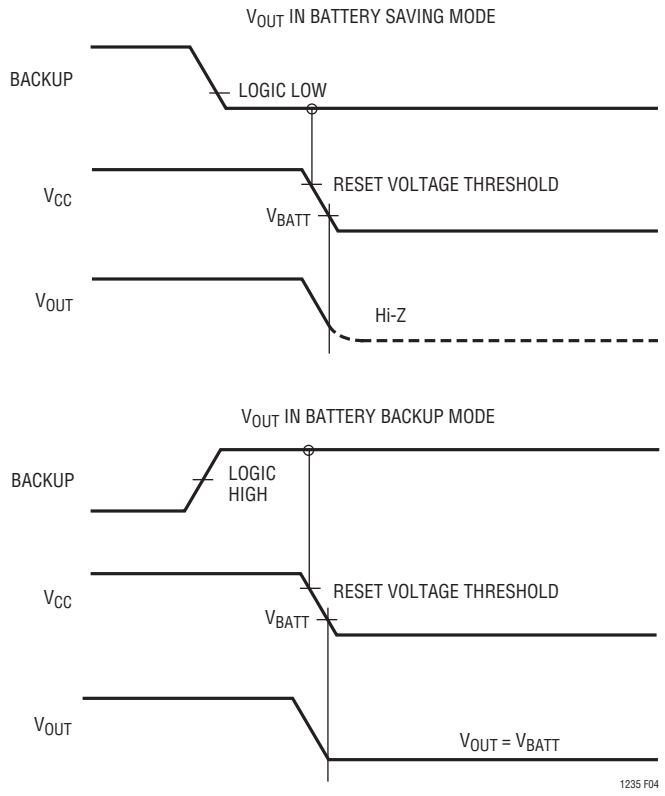


Figure 4. Conditional Battery Backup Operation

The operating voltage at the V_{BATT} pin ranges from 2.0V to 4.25V. High value capacitors, such as electrolytic or faradsize double layer capacitors, can be used for short term memory backup instead of a battery. For capacitor backup, see Typical Applications. The charging resistor for recharging rechargeable batteries should be connected to V_{OUT} through a diode since this eliminates the discharge path that exists when V_{CC} collapses and RAM is not backed up (Figure 5).

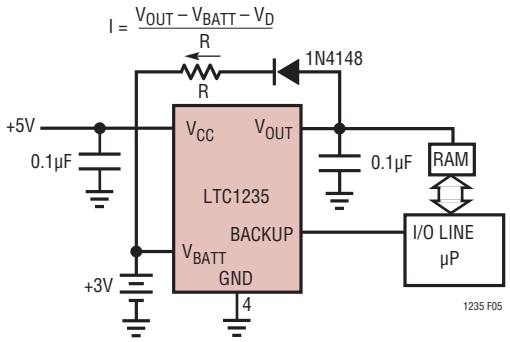


Figure 5. Charging External Battery Through V_{OUT}

Replacing the Backup Battery with Power On

When changing the backup battery with system power on, spurious resets can occur while battery is removed due to battery standby current. Although battery standby current is only a tiny leakage current, it can still charge up the stray capacitance on the V_{BATT} pin. The oscillation cycle is as follows: When V_{BATT} reaches within 50mV of V_{CC}, the LTC1235 switches to battery backup or battery saving mode. In either case, the battery supply current pulls V_{BATT} low and the device goes back to normal operation. The leakage current then charges up the V_{BATT} pin again and the cycle repeats.

If spurious resets during battery replacement pose no problems, then no action is required. Otherwise, two methods can be used to eliminate this problem. First, a capacitor from V_{BATT} to GND will allow time for battery replacement by slowing the charge rate. For example, the battery standby current is 1µA maximum over temperature and the external capacitor required to slow the charge rate is:

$$C_{EXT} \geq T_{REQ'D}\left(\frac{1\mu A}{V_{CC} \pm V_{BATT}}\right)$$

where $T_{REQ'D}$ is the maximum time required to replace the backup battery. With V_{CC} = 4.5V, V_{BATT} = 3V and $T_{REQ'D}$ = 3 sec, the value for external capacitor is 2µF. Second, a resistor from V_{BATT} to GND will hold the pin low while changing the battery. For example, the battery standby current is 1µA maximum over temperature and the external resistor required to hold V_{BATT} below V_{CC} is:

$$R \leq \frac{V_{CC} \pm 50mV}{1\mu A}$$

With V_{CC} = 4.5V, a 4.3M resistor will work. With a 3V battery, this resistor will draw only 0.7µA from the battery, which is negligible in most cases.

If the battery connections are made with long wires or PC traces, inductive spikes can be generated during battery replacement. Even if a resistor is used to prevent spurious resets as described above, these spikes can take the V_{BATT} pin below GND violating the LTC1235 absolute maximum ratings. A 0.1µF capacitor from V_{BATT} to GND is recommended to eliminate these potential spikes when battery replacement is made through long wires.

Table 1 shows the state of each pin during battery backup. If the backup battery is not used, connect V_{BATT} to GND and V_{OUT} to V_{CC}.

Table 1. Input and Output Status in Battery Backup Mode

SIGNAL	STATUS
V_{CC}	C2 monitors V_{CC} for active switchover.
BACKUP	BACKUP is ignored.
V_{OUT}	V_{OUT} is connected to V_{BATT} through an internal PMOS switch.
V_{BATT}	The supply current is 1µA maximum.
BATT ON	Logic high. The open circuit output voltage is equal to V_{OUT}.
PFI	Power Failure Input is ignored.
$\overline{PFO}$	Logic low
$\overline{PB\ RST}$	$\overline{PB\ RST}$ is ignored.
$\overline{RESET}$	Logic low
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low
WDI	Watchdog Input is ignored.
$\overline{WDO}$	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{CE}$ IN	$\overline{Chip\ Enable}$ Input is ignored.
$\overline{CE}$ OUT	Logic high. The open circuit output voltage is equal to V_{OUT}.

Memory Protection

The LTC1235 includes memory protection circuitry which ensures the integrity of the data in memory by preventing write operations when V_{CC} is at invalid level. Two pins, $\overline{CE}$ IN and $\overline{CE}$ OUT, control the $\overline{Chip\ Enable}$ or $\overline{Write}$ inputs of CMOS RAM. When V_{CC} is +5V, $\overline{CE}$ OUT follows $\overline{CE}$ IN with a typical propagation delay of 20ns. When V_{CC} falls below the reset voltage threshold or V_{BATT}, $\overline{CE}$ OUT is forced high, independent of $\overline{CE}$ IN. $\overline{CE}$ OUT is an alternative signal to drive the $\overline{CE}$, $\overline{CS}$, or Write input of battery-backed up CMOS RAM. $\overline{CE}$ OUT can also be used to drive the Store or $\overline{Write}$ input of an EEPROM, EAROM or NOVRAM to achieve similar protection. Figure 6 shows the timing diagram of $\overline{CE}$ IN and $\overline{CE}$ OUT.

$\overline{CE}$ IN can be derived from the microprocessor's address decoder output. Figure 7 shows a typical nonvolatile CMOS RAM application.

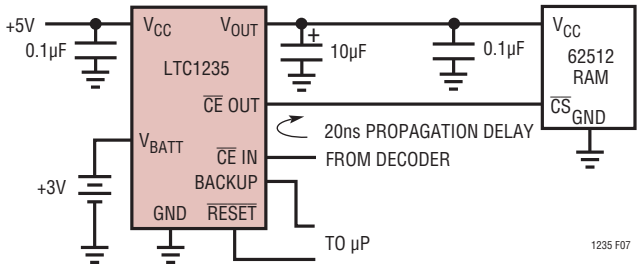


Figure 7. A Typical Nonvolatile CMOS RAM Application

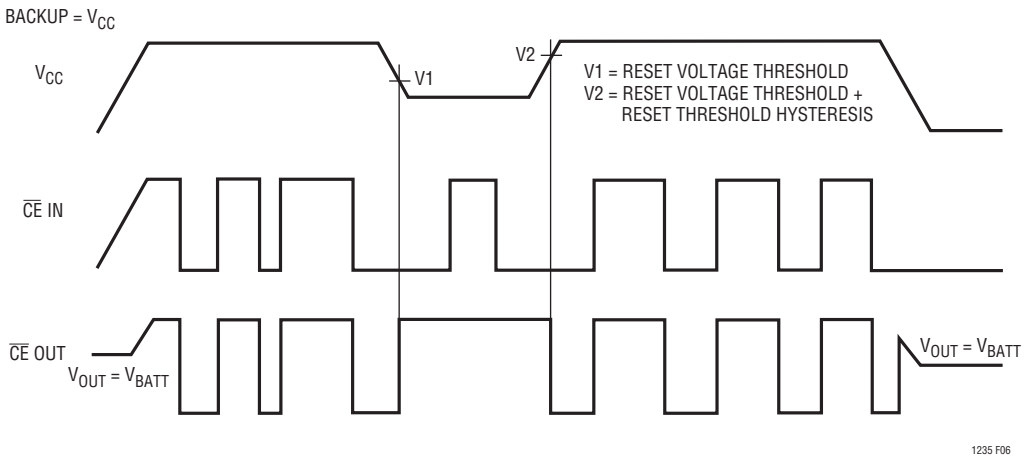


Figure 6. Timing Diagram for $\overline{CE}$ IN and $\overline{CE}$ OUT

APPLICATIONS INFORMATION

Power Fail Warning

The LTC1235 generates a Power Failure Output ($\overline{PFO}$) for early warning of failure in the microprocessor's power supply. This is accomplished by comparing the Power Failure Input (PFI) with an internal 1.3V reference. $\overline{PFO}$ goes low when the voltage at PFI pin is less than 1.3V. Typically PFI is driven by an external voltage divider (R1 and R2 in Figures 8 and 9) which senses either an unregulated DC input or a regulated 5V output. The voltage divider ratio can be chosen such that the voltage at PFI pin falls below 1.3V several milliseconds before the +5V supply falls below the maximum reset voltage threshold 4.75V. $\overline{PFO}$ is normally used to interrupt the microprocessor to execute shutdown procedure between $\overline{PFO}$ and $\overline{RESET}$ or RESET.

The power fail comparator, C3, does not have hysteresis. Hysteresis can be added however, by connecting a resistor between the $\overline{PFO}$ output and the noninverting PFI input pin as shown in Figures 8 and 9. The upper and lower trip points in the comparator are established as follows:

When $\overline{PFO}$ output is low, R3 sinks current from the summing junction at the PFI pin.

$$V_H = 1.3V\left(1+\frac{R1}{R2}+\frac{R1}{R3}\right)$$

When $\overline{PFO}$ output is high, the series combination of R3 and R4 source current into the PFI summing junction.

$$V_L = 1.3V\left(1+\frac{R1}{R2}\pm\frac{(5V\pm1.3V)R1}{1.3V(R3+R4)}\right)$$

$$\text{Assuming } R4 \ll R3, V_{HYST} = 5V\frac{R1}{R3}$$

Example 1: The circuit in Figure 8 demonstrates the use of the power fail comparator to monitor the unregulated power supply input. Assuming the rate of decay of the supply input V_{IN} is 100mV/ms and the total time to execute a shut-down procedure is 8ms. Also the noise of V_{IN} is 200mV. With these assumptions in mind, we can reasonably set V_L = 7.5V which 1.25V greater than the sum of maximum reset voltage threshold and the dropout voltage of LT1086-5 (4.75V + 1.5V) and V_{HYST} = 850mV.

$$V_{HYST} = 5V\frac{R1}{R3} = 850mV$$

$$R3 \approx 5.88\ R1$$

Choose R3 = 300k and R1 = 51k. Also select R4 = 10k which is much smaller than R3.

$$7.5V = 1.3V\left(1+\frac{51k}{R2}\pm\frac{(5V\pm1.3V)51k}{1.3V(310k)}\right)$$

R2 = 9.7k, Choose nearest 5% resistor 10k and recalculate V_L,

$$V_L = 1.3V\left(1+\frac{51k}{10k}\pm\frac{(5V\pm1.3V)51k}{1.3V(310k)}\right) = 7.32V$$

$$V_H = 1.3V\left(1+\frac{51k}{10k}+\frac{51k}{300k}\right) = 8.151V$$

$$\frac{(7.32V-6.25V)}{100mV/ms} = 10.7ms$$

V_{HYST} = 8.151V – 7.32V = 831mV

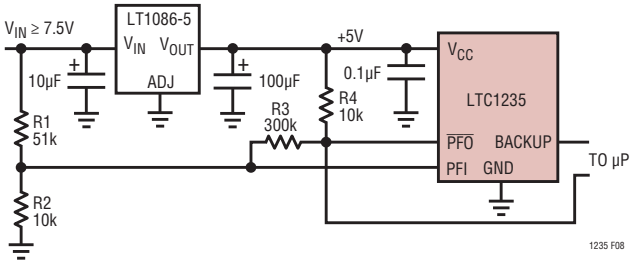


Figure 8. Monitoring *Unregulated* DC Supply with the LTC1235 Power Fail Comparator

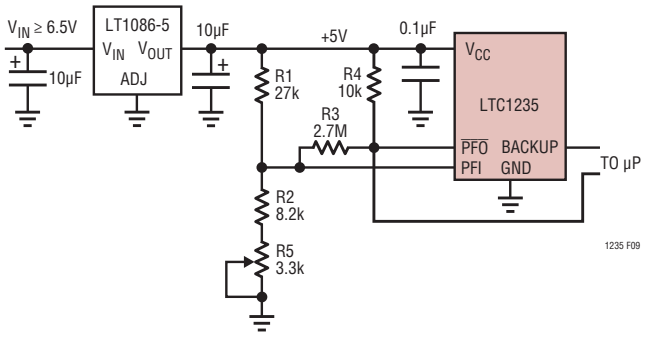


Figure 9. Monitoring *Regulated* DC Supply with the LTC1235 Power Fail Comparator

APPLICATIONS INFORMATION

The 10.7ms allows enough time to execute shut-down procedure for microprocessor and 831mV of hysteresis would prevent $\overline{PFO}$ from going low due to the noise of V_{IN}.

Example 2: The circuit in Figure 9 can be used to measure the regulated 5V supply to provide early warning of power failure. Because of variations in the PFI threshold, this circuit requires adjustment to ensure that the PFI comparator trips before the reset threshold is reached. Adjust R5 such that the $\overline{PFO}$ output goes low when the V_{CC} supply reaches the desired level (e.g., 4.85V).

Monitoring the Status of the Battery

C3 can also monitor the status of the memory backup battery (Figure 10). If desired, the $\overline{CE}$ OUT can be used to apply a test load to the battery. Since $\overline{CE}$ OUT is forced high in battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

Watchdog Timer

The LTC1235 provides a watchdog timer function to monitor the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the time-out period, the reset outputs are forced to active states for a minimum of 140ms. The watchdog time-out period is fixed at 1.0 second minimum on the LTC1235. This time-out period provides adequate time for many systems to service the watchdog timer immediately after a reset. Figure 11 shows the timing diagram of watchdog time-out period and reset active time. The watchdog time-out period is restarted as soon as the reset outputs are inactive. When either a high-to-low or low-to-high transition occurs at the WDI pin prior to time-out, the watchdog time is reset and begins to time out again. To ensure the watchdog time does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum time-out period. If the input to the WDI pin remains either high or low, reset pulses will be issued every 1.6 seconds typically. The watchdog timer can be deactivated by floating the WDI pin. The timer is also disabled when V_{CC} falls below the reset voltage threshold or V_{BATT}.

The Watchdog Output, $\overline{WDO}$, goes low if the watchdog timer is allowed to time out and remains low until set high by the next transition on the WDI pin. $\overline{WDO}$ is also set high when V_{CC} falls below the reset voltage threshold or V_{BATT}.

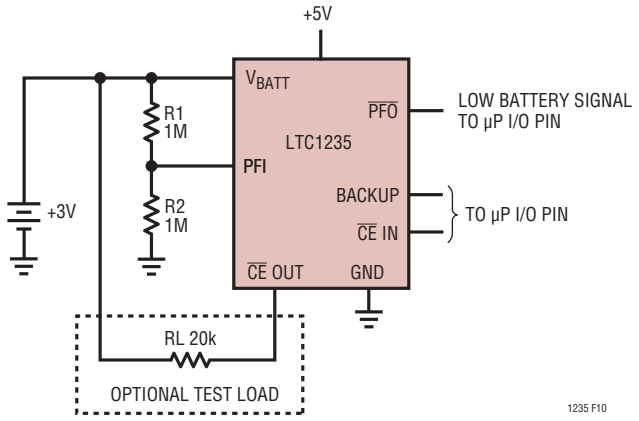


Figure 10. Backup Battery Monitor with Optional Test Load

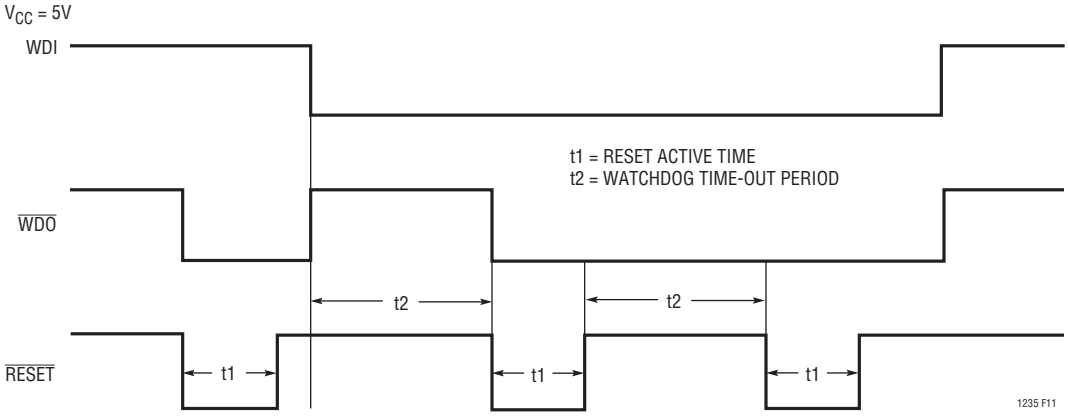
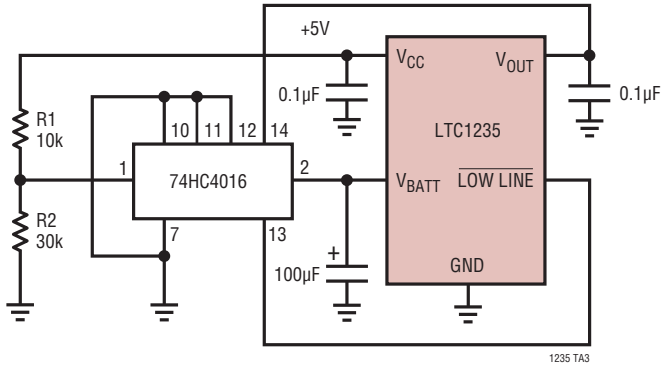


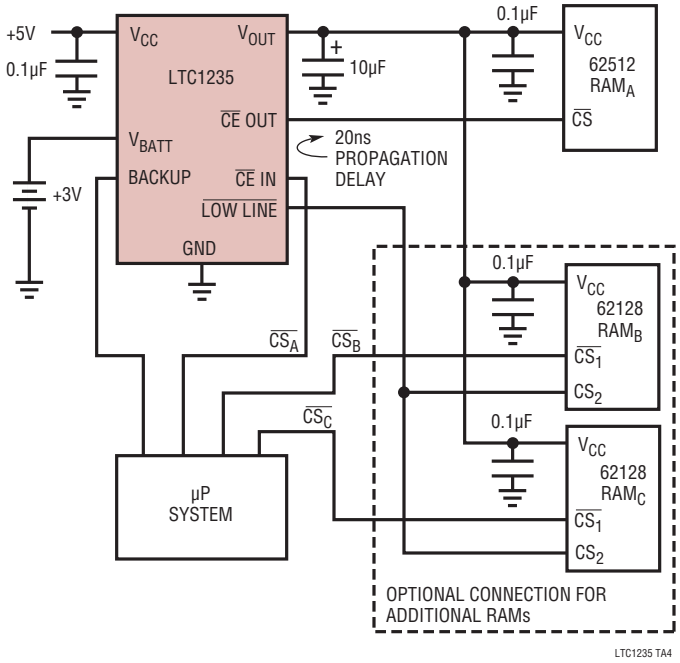
Figure 11. Watchdog Time-out Period and Reset Active Time

TYPICAL APPLICATIONS

Capacitor Backup with 74HC4016 Switch

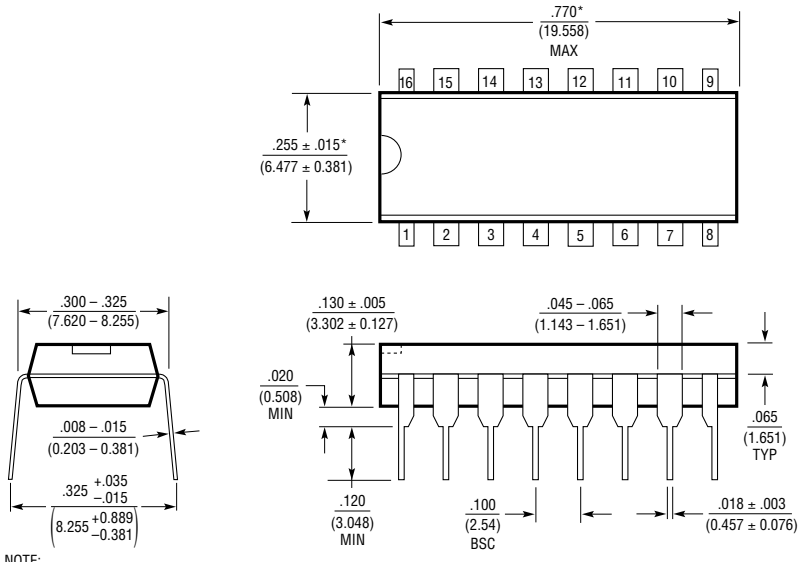


Write Protect for Additional RAMs



PACKAGE DESCRIPTION

N Package
16-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

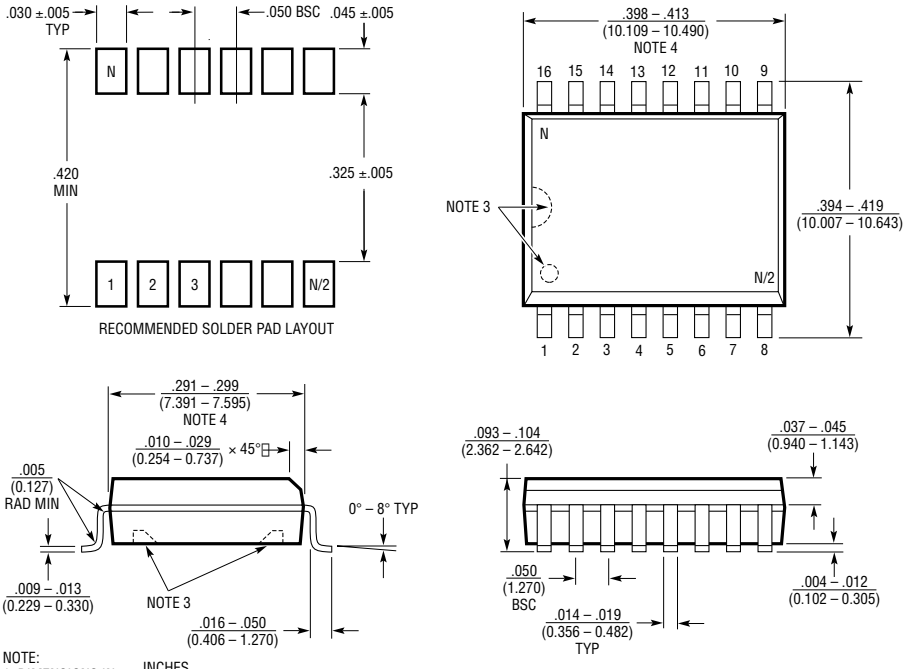


NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

N16 1002

SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S16 (WIDE) 0502

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC690	Single Channel Supervisor	UL recognized battery backup
LTC691	Single Channel Supervisor	UL recognized and conditional battery backup, RAM protect
LTC692	Single Channel Supervisor	UL recognized battery backup
LTC693	Single Channel Supervisor	UL recognized and conditional battery backup, RAM protect
LTC694	Single Channel Supervisor	UL recognized battery backup
LTC695	Single Channel Supervisor	UL recognized and conditional battery backup, RAM protect
LTC699	Single Channel Supervisor	Microprocessor Supervisory Circuit

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