Datasheet

AC/DC Converter IC

PWM Type DC/DC Converter IC Integrated Switching MOSFET

BM2P061FK-LBZ BM2P101FK-LBZ BM2P131FK-LBZ

General Description

This is the product guarantees long time support in industrial market.

This series IC is a PWM type DC/DC converter for AC/DC which provides an optimum system for various electrical product. It supports both isolated and non-isolated devices, enabling simpler design of various types of low power consumption electrical converters.

This series also has a built-in starter circuit that can withstand up to 800 V, which contributes to low power consumption. Since current mode control is utilized, current is restricted in each cycle and excellent performance is demonstrated in bandwidth and transient response. Switching frequency is fixed at 65 kHz, 100 kHz or 130 kHz. At light load, the switching frequency is reduced and high efficiency is achieved. A frequency hopping function is also built-in, which contributes to low EMI. In addition, this product has a built-in super junction MOSFET which has a withstand voltage of 800 V.

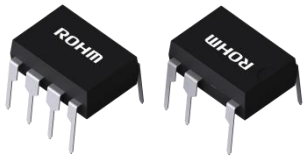
Features

- Long Time Support Product for Industrial Applications.
- Switching Frequency=65 kHz, 100 kHz, 130 kHz
- PWM Current Mode Control
- Built-in Frequency Hopping Function
- Burst Operation at Light Load
- Frequency Reduction Function
- Built-in 800 V Starter Circuit
- Built-in 800 V Super Junction MOSFET
- VCC Pin Under Voltage Protection
- VCC Pin Over Voltage Protection
- Over Current Limiter Function per Cycle
- Over Current Limiter with AC Voltage Correction
- Soft Start Function
- Brown IN/OUT Function
- ZT Pin OVP Function

Key Specifications

- Power Supply Voltage Operation Range:
  V_{CCA}(BM2P061FK-LBZ): 10.90 V to 30.00 V
  V_{CCA}(BM2P101FK-LBZ): 10.90 V to 30.00 V
  V_{CCB}(BM2P131FK-LBZ): 10.90 V to 26.00 V
  DRAIN: 800 V(Max)
- Normal Operating Current: 1.00 mA(Typ)
- Burst Operating Current: 0.30 mA(Typ)
- Switching Frequency:
  1A(BM2P061FK-LBZ): 65 kHz(Typ)
  1B(BM2P101FK-LBZ): 100 kHz(Typ)
  1C(BM2P131FK-LBZ): 130 kHz(Typ)
- Operating Temperature Range: -40 °C to +105 °C
- MOSFET ON Resistance: 1.60 Ω(Typ)

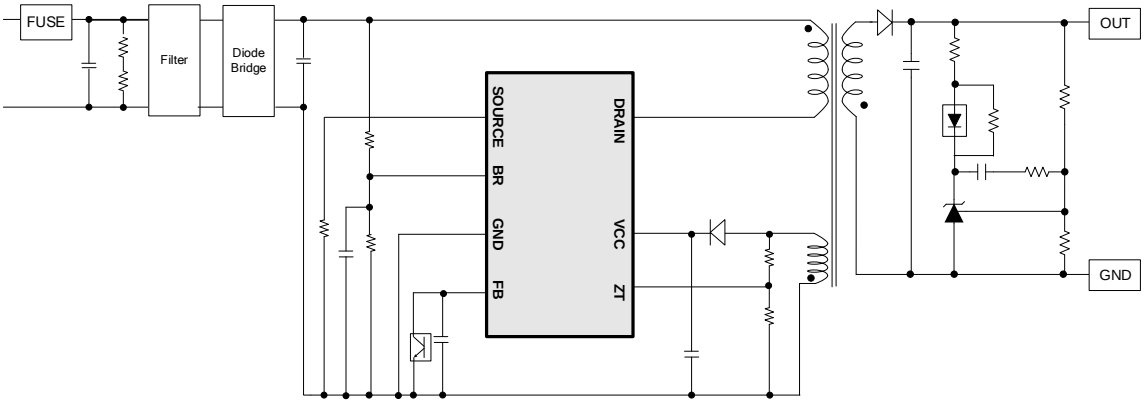
Package	W(Typ) x D(Typ) x H(Max)
DIP7AK:	9.27 mm x 6.35 mm x 8.63 mm pitch 2.54 mm



Applications

Industrial Equipment, Household Electrical Appliances, Adapters, etc.

Typical Application Circuit



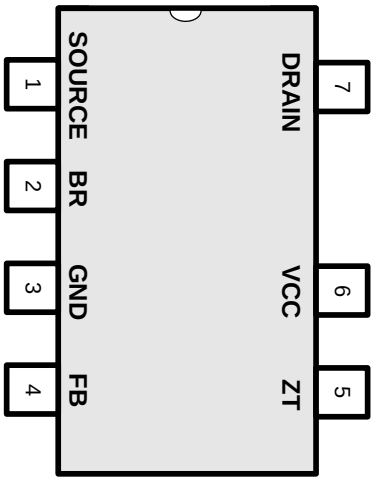
○Product structure: Silicon integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration

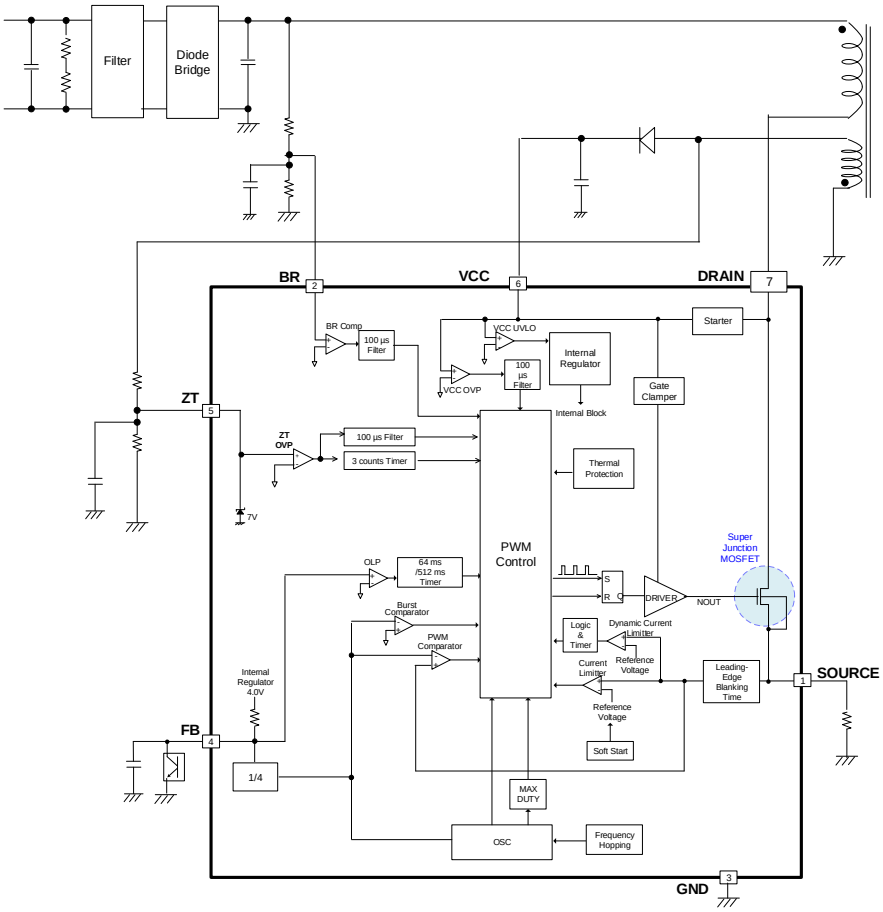
TOP VIEW



Pin Description

Pin No.	Pin Name	I/O	Function	ESD Diode	
				VCC	GND
1	SOURCE	I/O	MOSFET SOURCE pin	-	✓
2	BR	I	AC voltage detect pin	-	✓
3	GND	I/O	GND pin	✓	-
4	FB	I	Feedback signal input pin	-	✓
5	ZT	I	Auxiliary winding input pin	-	✓
6	VCC	I	Power supply input pin	-	✓
7	DRAIN	I/O	MOSFET DRAIN pin	-	✓

Block Diagram



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Description of Blocks

1. Starter Circuit (DRAIN: 7 pin)

This IC enables low standby electric power and high-speed startup because it has a built-in start circuit (800 V withstand voltage). The current consumption after startup is OFF current I_{START3} (Typ=10 µA).

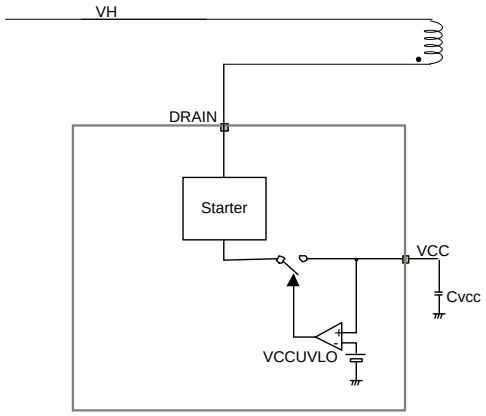


Figure 1. Start Circuit Block Diagram

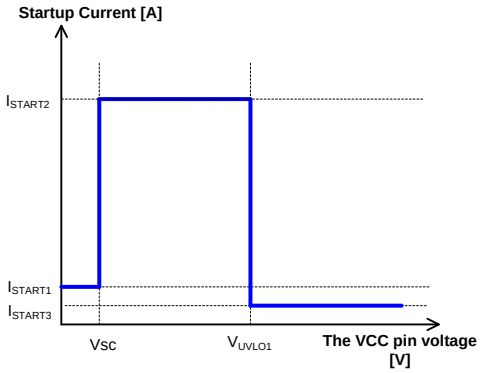


Figure 2. Startup Current vs the VCC Pin Voltage

2. Start Sequence (Soft Start Operation, Light Load Operation, Auto Restart Operation by Over Load Protection)

Start sequence is shown in Figure 3 and see the sections below for detailed descriptions.

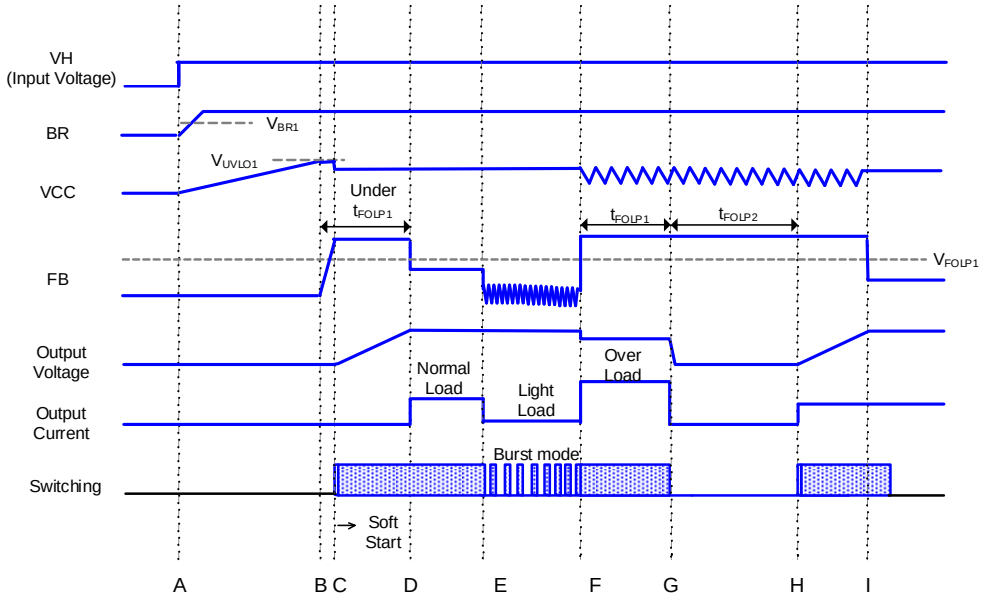


Figure 3. Start Sequences Timing Chart

A: The input voltage VH is applied to the IC. As VH voltage is applied, the BR pin voltage becomes higher than V_{BR1} (Typ=0.7 V).

B: When the VCC pin voltage exceeds V_{UVLO1} (Typ=15.5 V), the IC starts to operate. When the IC judges the other protection functions as normal condition, switching operation starts. Until the secondary output voltage becomes a constant value from startup, the VCC pin voltage drops by the VCC pin consumption current. When the VCC pin voltage becomes V_{CHG1} (Typ=10.7 V) or less, the VCC pin charge operation starts.

C: When switching operation starts, over current limit value is restricted to prevent any excessive rise in voltage or current by operating the soft start function. Output voltage will be set to rated voltage within the t_{FOLP1} (Typ=64 ms).

D: Once the output voltage is stable, the VCC pin voltage is also stable.

E: When the FB pin voltage becomes V_{BST1} (Typ=0.40 V) or less at light load, the IC starts burst operation to reduce the power consumption.

F: When the FB pin voltage becomes V_{FOLP1} (Typ=3.4 V) or more, overload protection function operates.

G: When the FB pin voltage stays V_{FOLP1} (Typ=3.4 V) or more for t_{FOLP1} (Typ=64 ms) or more, switching stops. When the FB pin voltage becomes V_{FOLP2} (Typ=3.2 V) or less, the IC's internal FB OLP timer is reset.

H: Stopping switching continues for t_{FOLP2} (Typ=512 ms), the IC starts switching.

I: Same as D.

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Description of Blocks – continued

3. VCC Pin Protection Function

This IC has the internal protection functions at the VCC pin.

1) Under voltage protection function: VCC UVLO (Under Voltage Lockout)
2) Over voltage protection function: VCC OVP (Over Voltage Protection)
3) VCC charge function

The VCC charge function charges the VCC pin from the high voltage line through the starter circuit at startup time and so on.

(1) VCC UVLO / VCC OVP Function

VCC UVLO function and VCC OVP function are auto recovery type protection function with voltage hysteresis. Switching is stopped by the VCC OVP function when the VCC pin voltage≥V_{OVP1A} (Typ=32.0 V) or the VCC pin voltage≥V_{OVP1B} (Typ=27.5 V), and restarts when the VCC pin voltage≤V_{OVP2A} (Typ=24.0 V) or the VCC pin voltage≤V_{OVP2B} (Typ=23.5 V).

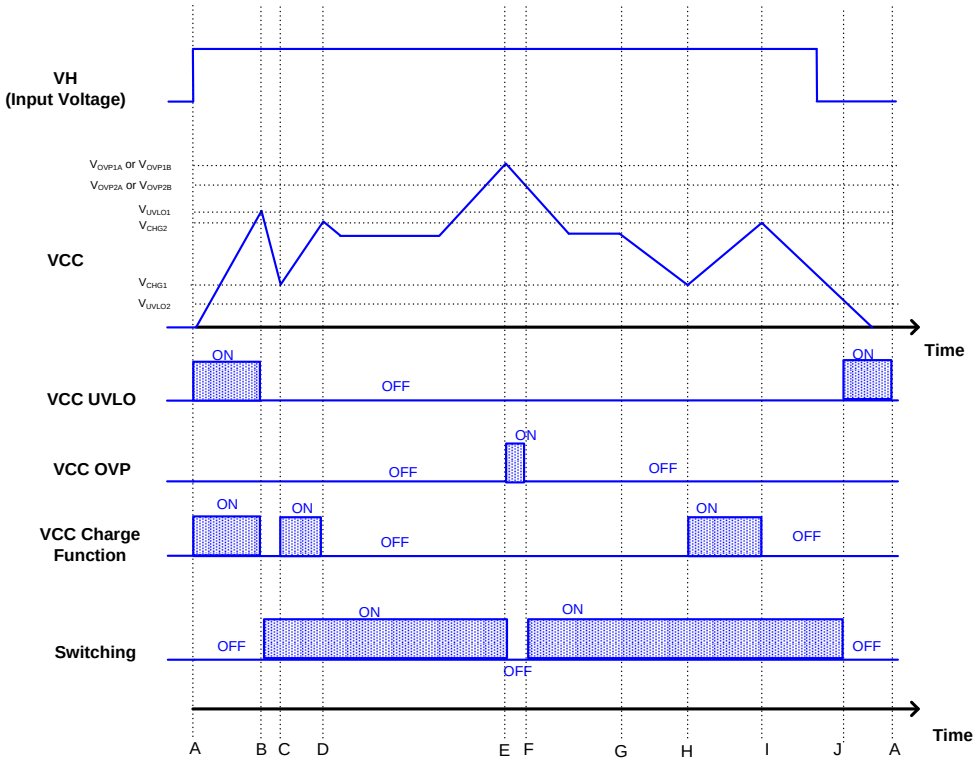


Figure 4. VCC UVLO / VCC OVP / VCC Charge Function Timing Chart

A: The VCC pin voltage starts to rises.
B: When the VCC pin voltage is V_{UVLO1} (Typ=15.5 V) or more, the VCC UVLO function is released and DC/DC operation starts.
C: When the VCC pin voltage is V_{CHG1} (Typ=10.7 V) or less, the VCC charge function operates and the VCC pin voltage rises.
D: When the VCC pin voltage is V_{CHG2} (Typ=15.0 V) or more, the VCC charge function stops.
E: When the status that the VCC pin voltage is V_{OVP1A} (Typ=32.0 V) or V_{OVP1B} (Typ=27.5 V) or more continues for t_{COMP1} (Typ=100 μs), switching is stopped by the VCC OVP function.
F: When the VCC pin voltage becomes V_{OVP2A} (Typ=24.0 V) or V_{OVP2B} (Typ=23.5 V) or less, switching operation restarts.
G: The VCC pin voltage drops.
H: Same as C.
I: Same as D.
J: When the input voltage VH drops and the VCC pin voltage becomes V_{UVLO2} (Typ=10.2 V) or less, switching operation is stopped by the VCC UVLO function.

(2) VCC Charge Function

The IC starts to operate when the VCC pin voltage becomes V_{UVLO1} (Typ=15.5 V) or more. After that, the VCC charge function operates when the VCC pin voltage becomes V_{CHG1} (Typ=10.7 V) or less. During this time, the VCC pin is charged from the DRAIN pin through the starter circuit. By this operation, failure at startup is prevented. Once the VCC charge function starts, it continues charge operation until the VCC pin voltage becomes V_{CHG2} (Typ=15.0 V) or more, after which the charge function stops.

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Description of Blocks – continued

4. DC/DC Driver (PWM Comparator, Frequency Hopping, Slope Compensate, OSC, Burst)

This IC operates by current mode PWM control. The internal oscillator sets the switching frequency at a fixed value when the FB pin voltage ≥ V_{DLT1} (Typ=1.25 V). It also has a built-in switching frequency hopping function.
Maximum duty cycle is fixed at 75 % (Typ) and minimum pulse width is fixed at 500 ns (Typ).
With current mode control, when the duty cycle exceeds 50 %, a sub harmonic oscillation may occur. As a countermeasure, the IC has built-in slope compensation function.
This IC also has a built-in burst mode operation and frequency reduction operation to achieve lower power consumption in light load.
The FB pin is pulled up by R_{FB} (Typ=30 kΩ) to an internal regulator. The FB pin voltage varies with secondary output voltage (secondary power). Burst mode operation and frequency reduction operation is determined by monitoring the FB pin voltage.

(1) Frequency Reduction Circuit

Figure 5A to Figure5C shows the FB pin voltage, switching frequency, and DC/DC operation modes.
mode 1: Burst voltage has hysteresis. Switching stops when the FB pin voltage ≤ V_{BST1} (Typ=0.4 V), and restarts when the FB pin voltage ≥ V_{BST2} (Typ=0.45 V).
mode 2: When the FB pin voltage ≤ V_{DLT2} (Typ=0.65 V), switching frequency is at f_{SW2} (Typ=25 kHz, 27 kHz or 35 kHz). At V_{DLT2} < the FB pin voltage ≤ V_{DLT1}, switching frequency changes within the range of f_{SW1} to f_{SW2}.
mode 3: Operates in fixed frequency f_{SW1} (Typ=65 kHz, 100 kHz or 130 kHz).
mode 4: If the IC detects over load status within a period of t_{FOLP1} (Typ=64 ms), it stops switching operation for t_{FOLP2} (Typ=512 ms).

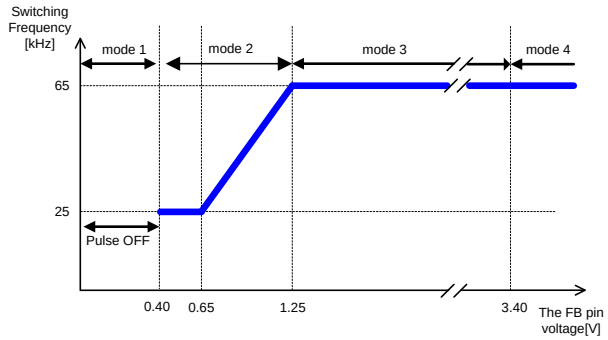


Figure 5A. Switching Frequency vs the FB Pin Voltage (BM2P061FK-LBZ)

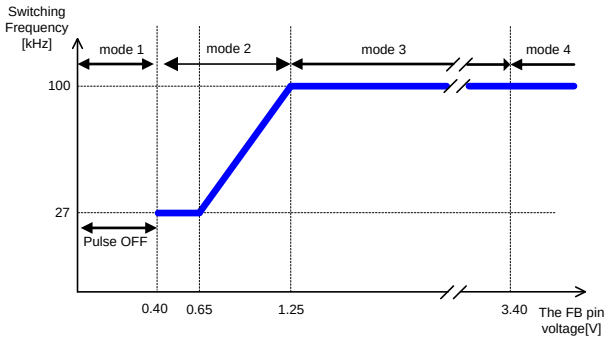


Figure 5B. Switching Frequency vs the FB Pin Voltage (BM2P101FK-LBZ)

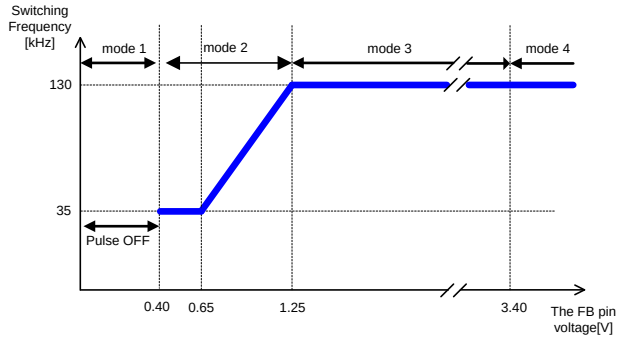


Figure 5C. Switching Frequency vs the FB Pin Voltage (BM2P131FK-LBZ)

(2) Frequency Hopping Function

Frequency hopping function achieves low EMI by changing the frequency at random. The pulse width changes in the range of ±6 % for base frequency.

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4. DC/DC Driver – continued

(3) Over Current Limiter

This IC has a built-in over current limiter per cycle. When the SOURCE pin voltage becomes V_{CSA} (Typ=0.4 V) or V_{CSB} (Typ=0.3 V) or more for 1 pulse, switching is turned off after passing internal delay time. The delay time varies in relation to the time by which the SOURCE pin voltage reaches V_{CSA} (Typ=0.4 V) or V_{CSB} (Typ=0.3 V). By this time, AC voltage correction function operates. The relations of the time until the SOURCE pin voltage reaches V_{CSA} (Typ=0.4 V) or V_{CSB} (Typ=0.3 V) and the additional delay time are shown in below.

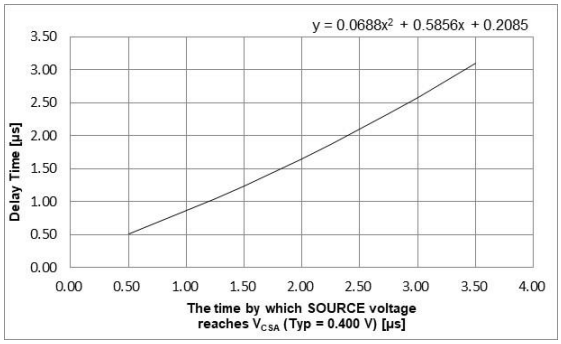


Figure 6A. Delay Time vs the Time by Which the SOURCE Pin Voltage Reaches V_{CSA} (Typ=0.4 V) (BM2P061FK-LBZ)

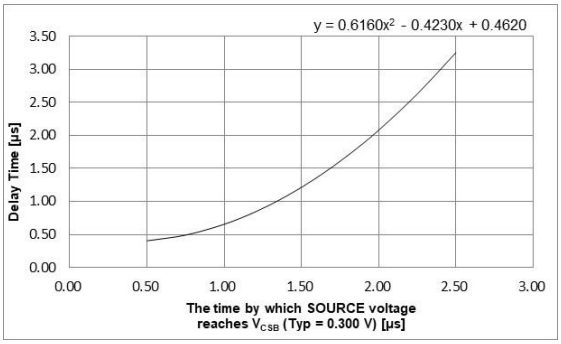


Figure 6B. Delay Time vs the Time by Which the SOURCE Pin Voltage Reaches V_{CSB} (Typ=0.3 V) (BM2P101FK-LBZ)

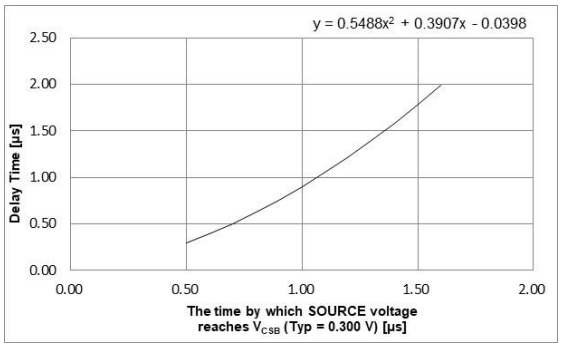


Figure 6C. Delay Time vs the Time by Which the SOURCE pin Voltage Reaches V_{CSB} (Typ=0.3 V) (BM2P131FK-LBZ)

Ip is calculated by the following formula.

$$Ip = \frac{Vin}{Lp} \times (t_{ON} + t_D + t_{DELAY}) \quad [A]$$

where:
Vin is the AC Input Voltage.
Lp is the Primary Inductance.
t_{ON} is the Time to V_{CSA} or V_{CSB}.
t_D is the Additional Delay Time introduced by the IC (Refer to Figure 6A to Figure 6C).
t_{DELAY} is the Delay Time peculiar to the IC (Typ=0.2 µs).

About the above Figure 6A to Figure 6C, design application considering that t_D operates in the range of ±20 % and t_{DELAY} operates in the range of ±0.1 µs. It is necessary to evaluate application in the end and adjust sense resistor and so on.

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4. DC/DC Driver – continued

(4) Dynamic Over Current Limiter

This IC has a built-in dynamic over current limiter circuit. When the SOURCE pin voltage becomes V_{DCS} (Typ=1.05 V) or more for two consecutive times, it stops switching operation for t_{DCS} (Typ=128 µs).

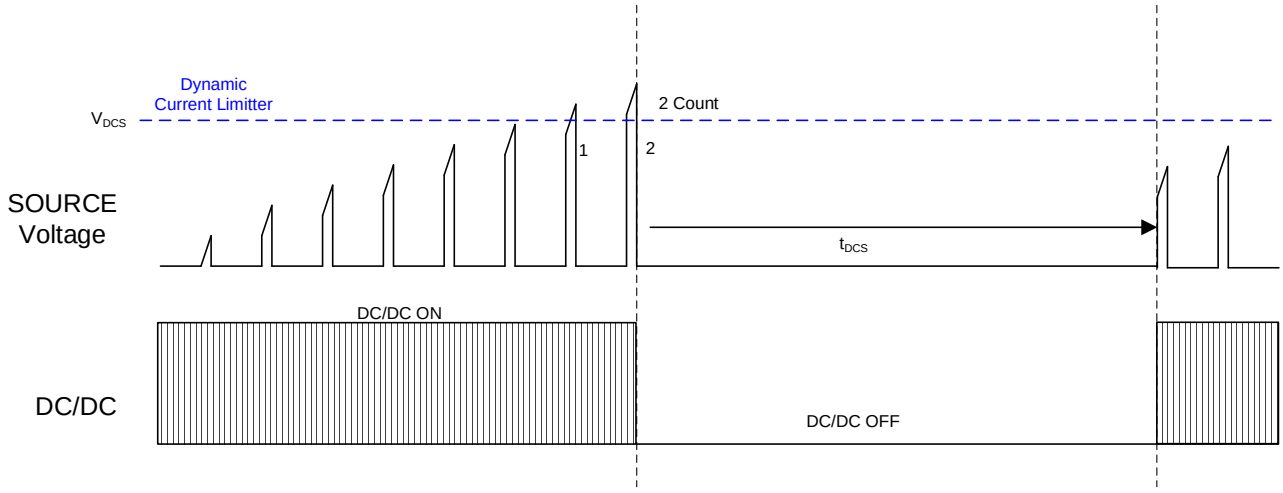


Figure 7. State Transition of Switching Frequency

(5) Soft Start Function

This function controls the over current limiter value in order to prevent any excessive rise in voltage or current upon startup. Figure 8 shows the details of soft start function. The IC implements soft start function by changing the over current limiter value with time.

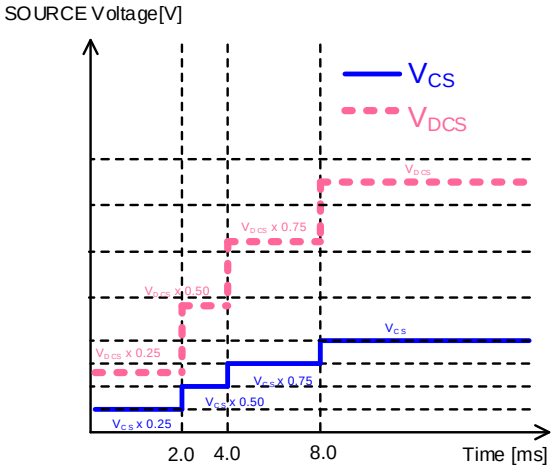


Figure 8. The SOURCE Pin Voltage vs Time

(6) L.E.B. Time

When MOSFET is turned ON, surge current occurs by capacitive elements and drive current. During this time, there is a probability of detection error in the over current limiter circuit due to a rise in the SOURCE pin voltage. To prevent it, there is a built-in L.E.B. function (Leading Edge Blanking function) to mask the SOURCE pin voltage for t_{LEB} (Typ=250 ns) after turn ON.

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Description of Blocks – continued

5. SOURCE Pin Short Protection

When the SOURCE pin is shorted to ground, the IC may overheat and get destroyed. To prevent destruction, it has a built-in short protection function. Switching is turned off in t_{CSSHT} (Typ=2.0 μs) ON width when the status that the SOURCE pin voltage is V_{CSSHT} (Typ=0.06 V) or less is detected by this function.

6. Output Over Load Protection Function (FB OLP Comparator)

Output over load protection function monitors the load condition and stops switching operation when over load condition is detected. The IC detects over load status at the FB pin voltage ≥ V_{FOLP1} (Typ=3.4 V) and releases FB OLP at the FB pin voltage ≤ V_{FOLP2} (Typ=3.2 V). As output voltage decreases during over load condition and this condition continues for t_{FOLP1} (Typ=64 ms), over load condition is detected and switching operation stops. FB OLP detection will be released after the auto-recovery period t_{FOLP2} (Typ=512 ms).

7. Input Voltage Protection Function (Brown IN/OUT)

This IC has a built-in UVLO function that monitors the input voltage through the BR pin. It prevents the IC from heating by over-current when the input voltage is low. When BR UVLO function is released, IC operates by soft start. The BR pin capacitor must be connected to prevent malfunction.

e.g. The case that BR UVLO is released when the input voltage is 130 Vac.

$$\frac{130V\times\sqrt{2}\times R_{BR2}}{R_{BR1}+R_{BR2}} = V_{BR1} \quad [V]$$

When R_{BR1} is set to 1.23 MΩ, R_{BR2} is calculated to 4.7 kΩ. Then, BR UVLO voltage is calculated as:

$$\frac{(R_{BR1}+R_{BR2})\times V_{BR2}}{R_{BR2}\times\sqrt{2}} = 71 \quad [Vac]$$

Therefore, the hysteresis is 59 Vac.

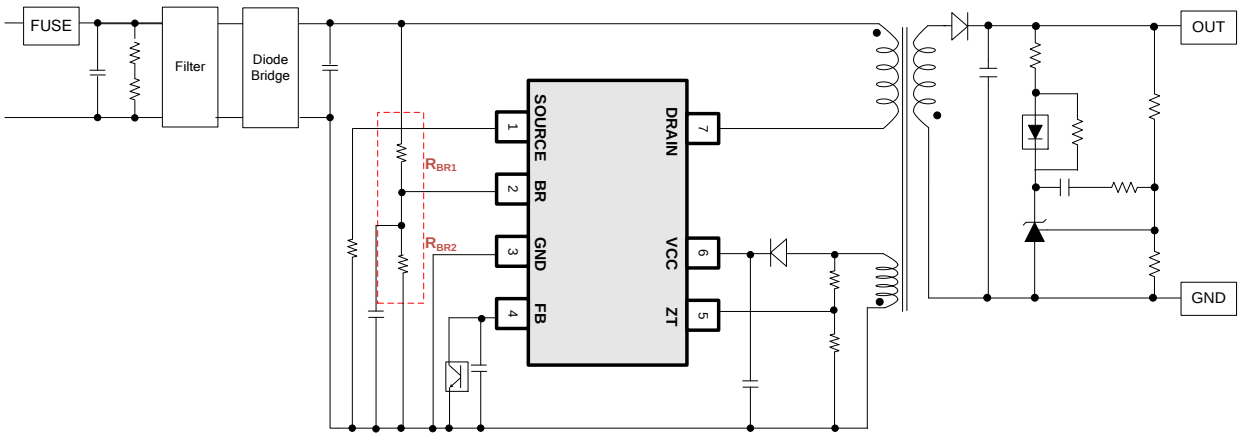


Figure 9. Brown IN/OUT Circuit Example.

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Description of Blocks – continued

8. ZT Pin Over Voltage Protection

ZT OVP has 2 protection functions (Pulse detection and DC detection), both operate by latch protection.

(1) Pulse Detection

After the ZT pin voltage becomes V_{ZTOVP} (Typ=3.5 V) or more for 3 consecutive switching times and continues for t_{ZTOVP} (Typ=100 µs), the IC detects ZT OVP.

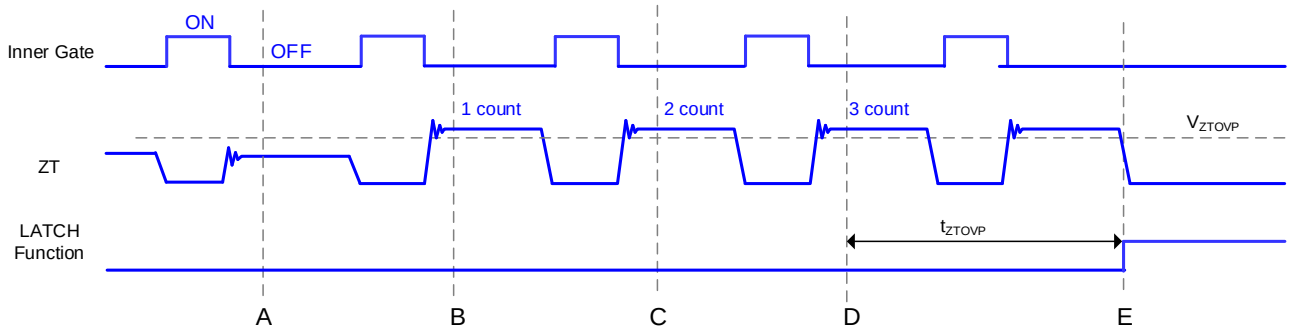


Figure 10. The ZT Pin Over Voltage Protection (Pulse Detection)

A: Normal operation because the ZT pin voltage < V_{ZTOVP} (Typ=3.5 V)
B: The ZT pin voltage ≥ V_{ZTOVP} (Typ=3.5 V) is detected.
C: The second of the ZT pin voltage ≥ V_{ZTOVP} (Typ=3.5 V) is detected.
D: The third of the ZT pin voltage ≥ V_{ZTOVP} (Typ=3.5 V) is detected. Then internal timer starts to operate because of detection of the three times continuation.
E: After t_{ZTOVP} (Typ=100 µs) from the three times detection, the IC stops by latch.

(2) DC Detection

When the ZT pin voltage ≥ V_{ZTOVP} (Typ=3.5 V) status continues for t_{ZTOVP} (Typ=100 µs), the IC detects ZT OVP.

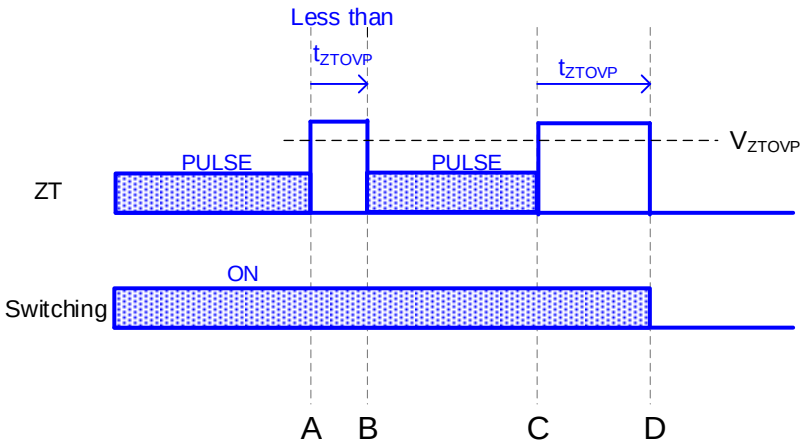


Figure 11. The ZT Pin Over Voltage Protection (DC Detection)

A: The ZT pin voltage ≥ V_{ZTOVP} (Typ=3.5 V)
B: Because the ZT pin voltage ≥ V_{ZTOVP} (Typ=3.5 V) status is less than t_{ZTOVP} (Typ=100 µs) period, DC/DC returns to normal operations.
C: The ZT pin voltage ≥ V_{ZTOVP} (Typ=3.5 V)
D: Because the ZT pin voltage ≥ V_{ZTOVP} (Typ=3.5 V) status continues for t_{ZTOVP} (Typ=100 µs), latching occurs and DC/DC is turned OFF.

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Description of Blocks – continued

9. ZT Trigger Mask Function

When switching is set ON / OFF, the superposition of noise may occur at the ZT pin. During this time, the detection function is turned OFF for the duration of t_{ZTMASK} (Typ=0.60 μs) to prevent the ZT pin part from false detection.

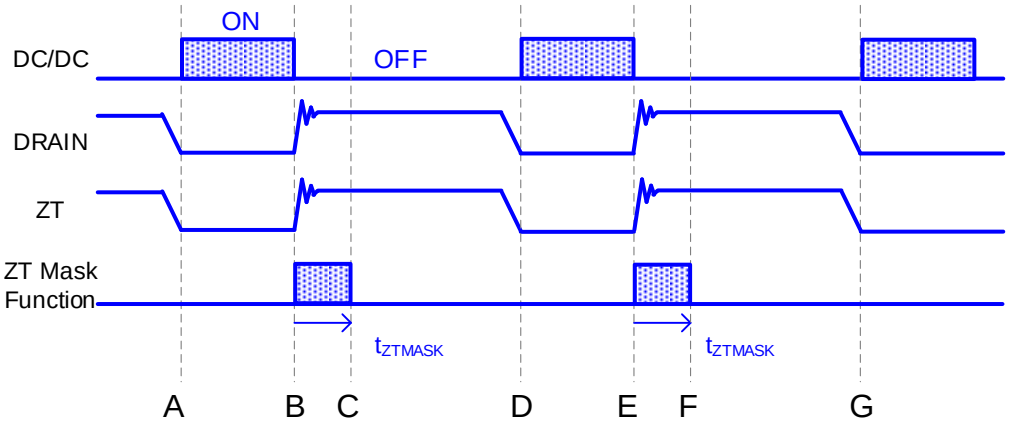


Figure 12. ZT Trigger Mask Function

A: DC/DC OFF → ON
B: DC/DC ON → OFF
C: Because noise occurs at the ZT pin, the ZT pin protection function is not operated for t_{ZTMASK} (Typ=0.60 μs).
D: Same as A.
E: Same as B
F: Same as C
G: Same as A

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Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Applied Voltage 1	V_{MAX1}	-0.3 to +800.0	V	DRAIN
Maximum Applied Voltage 2	V_{MAX2}	-0.3 to +35.0	V	VCC
Maximum Applied Voltage 3	V_{MAX3}	-0.3 to +6.5	V	BR, FB, SOURCE, ZT
DRAIN Current (DC)	I_{DD1}	3.0	A	
DRAIN Current (Pulse)	I_{DD2}	9.0	A	P_W=10 µs, Duty cycle=1 %
Power Dissipation	Pd	1.00	W	
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Reduce by 8.0 mW/°C when operating Ta=25 °C or more when mounted on 70 mm x 70 mm x 1.6 mm thick, glass epoxy on single-layer substrate.

Thermal Loss

The thermal design should set operation for the following conditions.

1. The ambient temperature Ta must be 105 °C or less.
2. The IC's loss must be within the power dissipation Pd.

The thermal reduction characteristics are as follows.
(PCB: 70 mm x 70 mm x 1.6 mm mounted on glass epoxy single layer substrate)

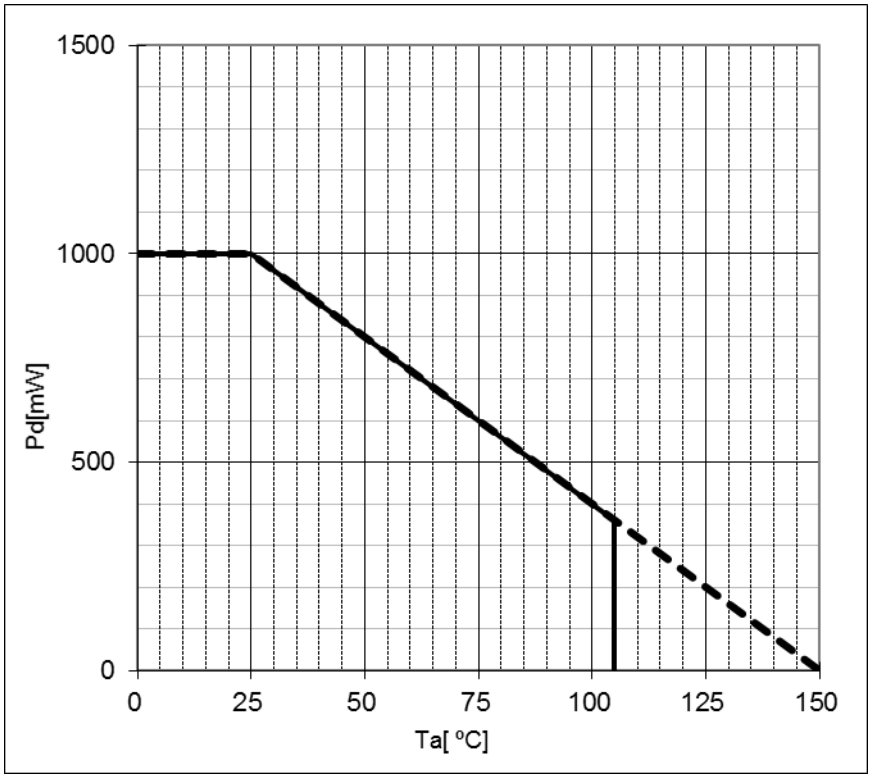


Figure 13. Thermal Reduction Characteristics

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Recommended Operating Condition

Parameter	Symbol	Specification			Unit	Conditions
		Min	Typ	Max		
Power Supply Voltage Range 1	V_{DRAIN}	-	-	800	V	DRAIN
Power Supply Voltage Range 2A	V_{CCA}	10.90	15.00	30.00	V	VCC *(Note 2)* BM2P061FK-LBZ, BM2P101FK-LBZ
Power Supply Voltage Range 2B	V_{CCB}	10.90	15.00	26.00	V	VCC *(Note 2)* BM2P131FK-LBZ
Operating Temperature	Topr	-40	+25	+105	°C	Surrounding Temperature

(Note 2) The VCC recharge function operates in the VCC pin voltage range of less than V_{CHG1} (Refer to P-4 [3-2] the VCC charge function)

Recommended External Component Condition

Parameter	Symbol	Recommended	Unit	Conditions
BR Pin Capacitor	C_{BR}	0.01 or more	μF	

Electrical Characteristics in MOSFET Part (Unless otherwise noted, Ta=25 °C, VCC=15 V)

Parameter	Symbol	Specifications			Unit	Conditions
		Min	Typ	Max		
DRAIN to SOURCE Voltage	V_{DDS}	800	-	-	V	I_D=1 mA, V_{GS}=0 V
DRAIN Leak Current	I_{DSS}	-	0	100	μA	V_{DS}=800 V, V_{GS}=0 V
ON Resistance	$R_{DS(ON)}$	-	1.60	2.15	Ω	I_D=1.5 A, V_{GS}=10 V

Electrical Characteristics in Starter Circuit Part (Unless otherwise noted, Ta=25 °C, VCC=15 V)

Parameter	Symbol	Specifications			Unit	Conditions
		Min	Typ	Max		
Start Current 1	I_{START1}	0.100	0.300	0.600	mA	VCC=0 V
Start Current 2	I_{START2}	3.00	5.50	8.50	mA	VCC=10 V
OFF Current	I_{START3}	-	10	20	μA	
Start Current Switching Voltage	V_{SC}	0.400	0.800	1.200	V	

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Electrical Characteristics in Control IC Part (Unless otherwise noted, Ta=25 °C, VCC=15 V)

Parameter	Symbol	Specifications			Unit	Conditions
		Min	Typ	Max		
[Circuit Current]						
Circuit Current (ON)1	I_{ON1}	-	1000	1800	μA	Pulse Operation, V_{FB}=2.0 V, DRAIN =OPEN
Circuit Current (ON)2	I_{ON2}	150	300	450	μA	Burst Operation, V_{FB}=0.3 V
[VCC Pin Protection Function]						
VCC UVLO Voltage 1	V_{UVLO1}	14.50	15.50	16.50	V	VCC rising
VCC UVLO Voltage 2	V_{UVLO2}	9.50	10.20	10.90	V	VCC falling
VCC UVLO Hysteresis	V_{UVLO3}	-	5.30	-	V	$V_{UVLO3}=V_{UVLO1}-V_{UVLO2}$
VCC OVP Voltage 1A	V_{OVP1A}	30.0	32.0	34.0	V	BM2P061FK-LBZ, BM2P101FK-LBZ
VCC OVP Voltage 1B	V_{OVP1B}	26.0	27.5	29.0		BM2P131FK-LBZ
VCC OVP Voltage 2A	V_{OVP2A}	-	24.0	-	V	BM2P061FK-LBZ, BM2P101FK-LBZ
VCC OVP Voltage 2B	V_{OVP2B}	-	23.5	-	V	BM2P131FK-LBZ
VCC OVP Hysteresis A	V_{OVP3A}	-	8.0	-	V	BM2P061FK-LBZ, BM2P101FK-LBZ
VCC OVP Hysteresis B	V_{OVP3B}	-	4.0	-	V	BM2P131FK-LBZ
VCC OVP Timer	t_{COMP1}	50	100	150	μs	
Latch Release VCC Voltage	V_{LATCH}	-	V_{UVLO2}-0.5	-	V	
VCC Charge Start Voltage	V_{CHG1}	9.70	10.70	11.70	V	
VCC Charge Stop Voltage	V_{CHG2}	14.00	15.00	16.00	V	
Over Temperature Protection 1 *(Note 3)*	T_{SD1}	150	175	200	°C	Control IC block's Tj rising
Over Temperature Protection 2 *(Note 3)*	T_{SD2}	-	100	-	°C	Control IC block's Tj falling
Over Temperature Protection Hysteresis	T_{SD3}	-	75	-	°C	
Over Temperature Protection Timer	t_{COMP2}	50	100	150	μs	
[PWM Type DC/DC Driver Block]						
Switching Frequency 1A	f_{SW1A}	61.5	65.0	68.5	kHz	V_{FB}=2.0 V (BM2P061FK-LBZ)
Switching Frequency 2A	f_{SW2A}	20	25	30	kHz	V_{FB}=0.5 V (BM2P061FK-LBZ)
Frequency Hopping Width 1A	f_{DEL1A}	-	4.0	-	kHz	V_{FB}=2.0 V (BM2P061FK-LBZ)
Switching Frequency 1B	f_{SW1B}	95.0	100.0	105.0	kHz	V_{FB}=2.0 V (BM2P101FK-LBZ)
Switching Frequency 2B	f_{SW2B}	20	27	34	kHz	V_{FB}=0.5 V (BM2P101FK-LBZ)
Frequency Hopping Width 1B	f_{DEL1B}	-	6.0	-	kHz	V_{FB}=2.0 V (BM2P101FK-LBZ)
Switching Frequency 1C	f_{SW1C}	122.0	130.0	138.0	kHz	V_{FB}=2.0 V (BM2P131FK-LBZ)
Switching Frequency 2C	f_{SW2C}	20	35	50	kHz	V_{FB}=0.5 V (BM2P131FK-LBZ)
Frequency Hopping Width 1C	f_{DEL1C}	-	8.0	-	kHz	V_{FB}=2.0 V (BM2P131FK-LBZ)
Minimum Pulse Width *(Note 4)*	t_{MIN}	-	500	-	ns	
Soft Start Time 1	t_{SS1}	1.20	2.00	2.80	ms	
Soft Start Time 2	t_{SS2}	2.40	4.00	5.60	ms	
Soft Start Time 3	t_{SS3}	4.80	8.00	11.20	ms	
Maximum Duty	D_{MAX}	68.0	75.0	82.0	%	
FB Pin Pull-up Resistor	R_{FB}	23	30	37	kΩ	
FB / CS Gain	Gain	-	4.00	-	V/V	
FB Burst Voltage 1	V_{BST1}	0.300	0.400	0.500	V	V_{FB} falling
FB Burst Voltage 2	V_{BST2}	0.350	0.450	0.550	V	V_{FB} rising
Frequency Reduction Start FB Voltage	V_{DLT1}	1.10	1.25	1.40	V	
Frequency Reduction Stop FB Voltage	V_{DLT2}	0.50	0.65	0.80	V	
FB OLP Voltage 1	V_{FOLP1}	3.20	3.40	3.60	V	OLP detect V_{FB} rising
FB OLP Voltage 2	V_{FOLP2}	3.00	3.20	3.40	V	OLP release V_{FB} falling
FB OLP ON Timer	t_{FOLP1}	40	64	88	ms	
FB OLP OFF Timer	t_{FOLP2}	358	512	666	ms	

(Note 3) Over temperature protection operates over Maximum Junction Temperature. Since, IC cannot guarantee for the operation over Maximum Junction Temperature, always operate at Maximum Junction Temperature or less.

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Electrical Characteristics in Control IC Part (Unless otherwise noted, Ta=25 °C, VCC=15 V) – continued

Parameter	Symbol	Specifications			Unit	Conditions
		Min	Typ	Max		
[PWM Type DC/DC Driver Block]						
Over Current Detection Voltage A	V_{CSA}	0.380	0.400	0.420	V	BM2P061FK-LBZ
Over Current Detection Voltage B	V_{CSB}	0.280	0.300	0.320	V	BM2P101FK-LBZ, BM2P131FK-LBZ
Dynamic Over Current Detection Voltage	V_{DCS}	0.950	1.050	1.150	V	
Dynamic Over Current Detection Timer	t_{DCS}	64	128	196	µs	
Leading Edge Blanking Time	t_{LEB}	-	250	-	ns	*(Note 4)*
SOURCE Pin Short Protection Voltage	V_{CSSHT}	0.030	0.060	0.090	V	
SOURCE Pin Short Protection Time	t_{CSSHT}	1.0	2.0	3.0	µs	
[BR Pin Function]						
BR Pin UVLO Detection Voltage 1	V_{BR1}	0.64	0.70	0.76	V	V_{BR} rising
BR Pin UVLO Detection Voltage 2	V_{BR2}	0.32	0.38	0.44	V	V_{BR} falling
BR Pin UVLO Hysteresis Voltage	V_{BR3}	-	0.32	-	V	$V_{BR3}=V_{BR1}-V_{BR2}$
BR Pin UVLO Detection Delay Time 1	t_{BR1}	50	100	150	µs	V_{BR} rising
BR Pin UVLO Detection Delay Time 2	t_{BR2}	64	128	196	ms	V_{BR} falling
[ZT Pin Function]						
ZT OVP Voltage	V_{ZTOVP}	3.250	3.500	3.750	V	
ZT OVP Timer	t_{ZTOVP}	50	100	150	µs	
ZT Trigger Mask Time	t_{ZTMASK}	-	0.60	-	µs	*(Note 4)*

(Note 4) Not 100 % tested.

Protection Circuit Operation Modes

The operation modes of the various protection functions of the IC are shown in Table 1.

Table 1. Protection Circuit Operation Modes

Function	VCC Pin Under Voltage Protection	VCC Pin Over Voltage Protection	Thermal Shutdown	FB pin Output Over Load Protection	SOURCE Short Protection	BR Pin Under Voltage Protection	ZT Pin Over Voltage Protection
Detection	$VCC<V_{UVLO2}$ (VCC falling)	$VCC>V_{OVP1A}$ or $VCC>V_{OVP1B}$ (VCC rising)	$Tj>T_{SD1}$ (Tj rising)	$V_{FB}>V_{FOLP1}$ (V_{FB} rising)	SOURCE< V_{CSSHT} (t_{CSSHT}=2.0 µs)	$V_{BR}<V_{BR2}$ (V_{BR} falling)	$V_{ZT}>V_{ZTOVP}$ (pulse)
Release	$VCC>V_{UVLO1}$ (VCC rising)	$VCC<V_{OVP2A}$ or $VCC<V_{OVP2B}$ (VCC falling)	$Tj<T_{SD2}$ (Tj falling)	$V_{FB}<V_{FOLP2}$ (V_{FB} falling)	Reset Pulse by Pulse	$V_{BR}>V_{BR1}$ (V_{BR} rising)	$V_{ZT}<V_{ZTOVP}$ (pulse)
Detection Timer	-	100 µs	100 µs	64 ms	-	128 ms	3 counts +100 µs
Release Timer	-	-	-	512 ms	-	100 µs	-
Mode	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery	Latch

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I/O Equivalence Circuit

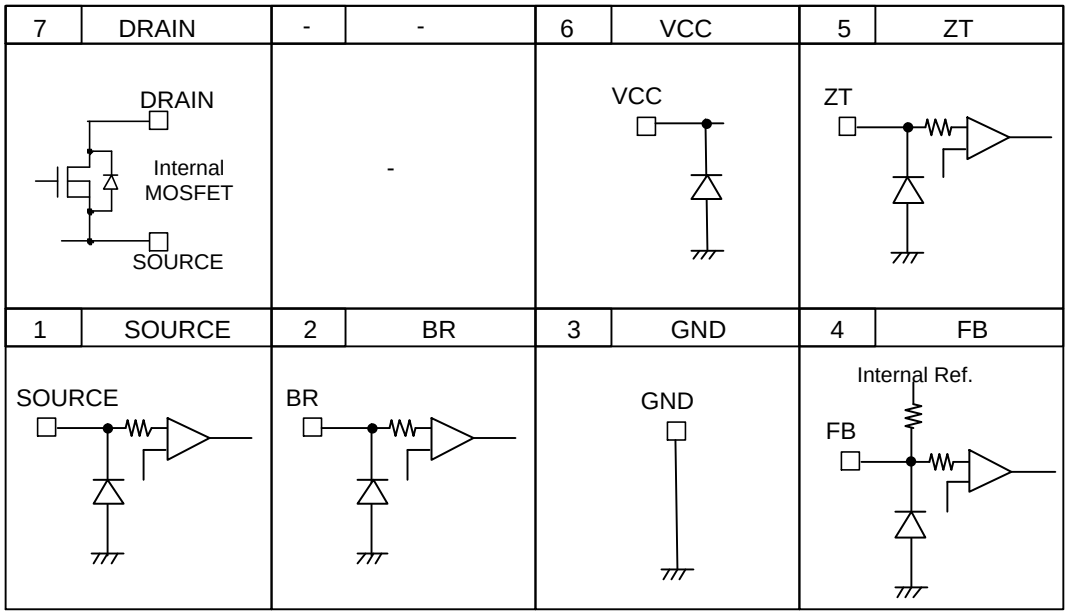


Figure 14. I/O Equivalence Circuits

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

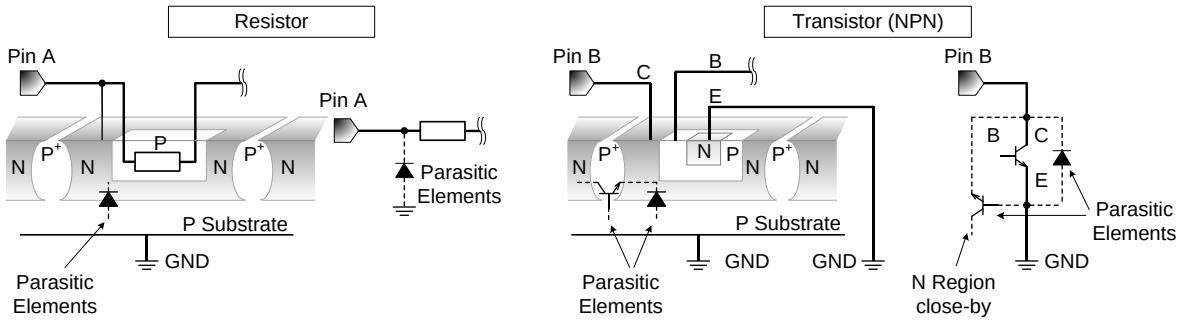


Figure 15. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information

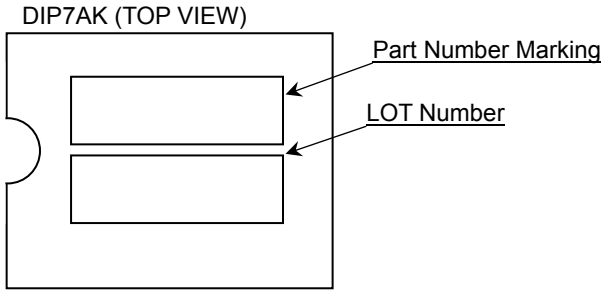
B M 2 P x x 1 F K - L B Z

- x x: 06: 65 kHz, 10: 100 kHz, 13: 130 kHz
- LBZ: Product Class, LB for Industrial Applications

Lineup

Product Number	Switching Frequency (kHz)	MOS FET $R_{DS(ON)}$ (Ω)	MOS FET Withstand Voltage (V)	Package	Orderable Part Number
BM2P061FK-LBZ	65	1.60	800	DIP7AK	BM2P061FK-LBZ
BM2P101FK-LBZ	100				BM2P101FK-LBZ
BM2P131FK-LBZ	130				BM2P131FK-LBZ

Making Diagram



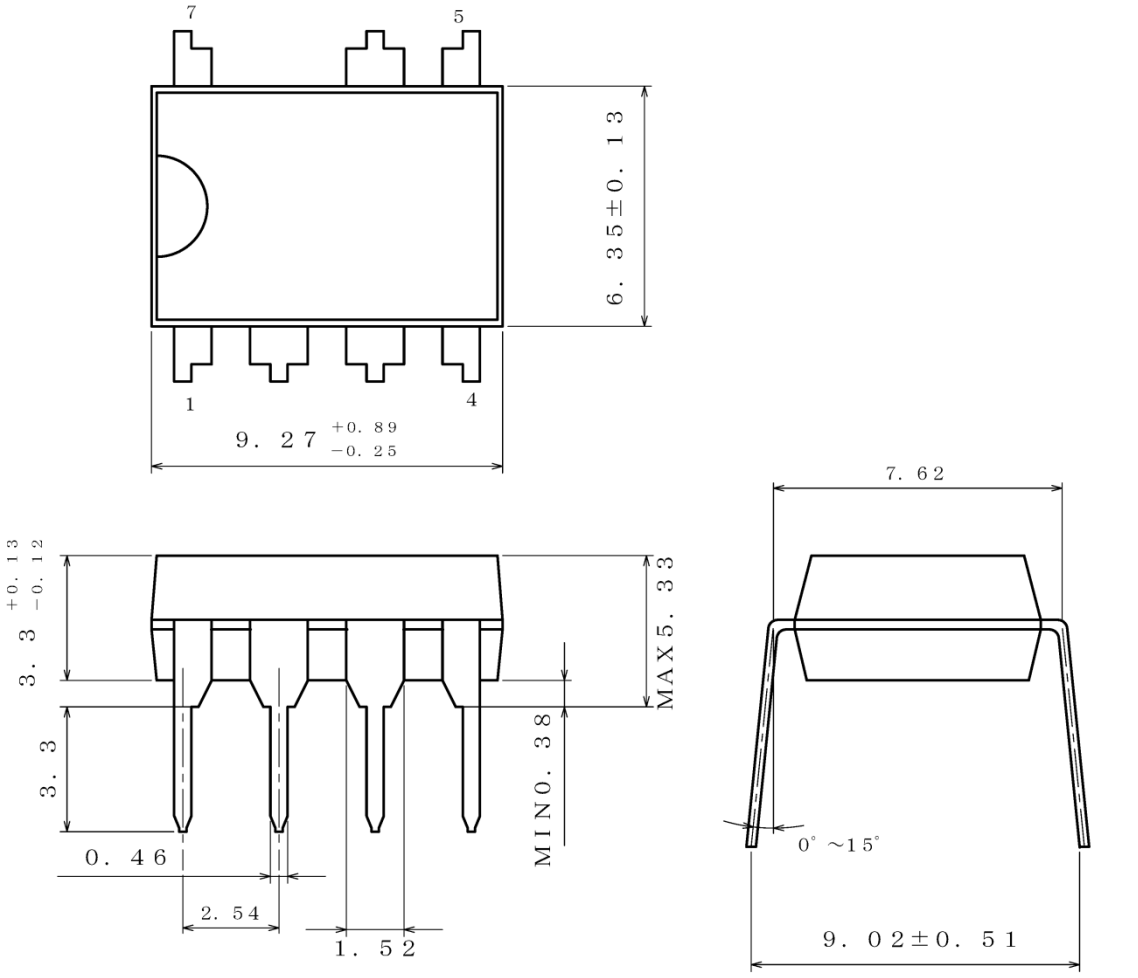
Product Number	Part Number Marking
BM2P061FK-LBZ	BM2P061FK
BM2P101FK-LBZ	BM2P101FK
BM2P131FK-LBZ	BM2P131FK

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Physical Dimension and Packing Information

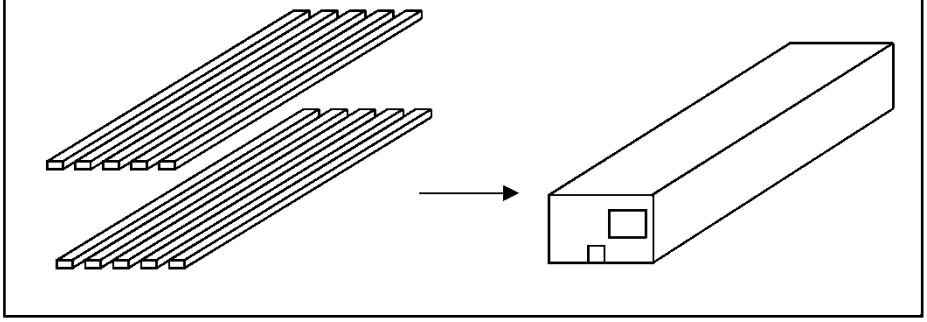
Package Name	DIP7AK



(UNIT:mm)
PKG:DIP7AK
Drawing No. EX001-0074

< Container Information >

Container	Tube
Quantity	2000pcs
Direction of feed	Packing orientation is same in tube



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Revision History

Date	Revision	Changes
09.Oct.2018	001	New Release
29.May.2019	002	Page12 Electrical Characteristics in MOSFET Part Ron(MAX) Add the division of product name
10.Feb.2021	003	Page6 Figure 6A, 6B, 6C are added to reference value for design and Figure 6B is updated formula

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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