Precision Angle Sensor IC
with On-Chip Linearization, SENT, SPI, and PWM Output

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC, for angular position, rotational speed, and direction measurement
  - □ Capable of sensing magnet rotational speeds targeting 12b effective resolution with 900 G field
  - □ Circular Vertical Hall (CVH) technology provides a single channel sensor system supporting operation across wide range of air gaps
- On-chip 32-segment linearization to improve angle accuracy
  - □ Reduces the impact of magnet to sensor misalignment
  - □ Reduces the impact of imperfect magnetization of target magnet
- Developed in accordance with ISO 26262 requirements for hardware product development for use in safety-critical applications
  - □ Single die version designed to meet ASIL B requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A33003 Safety Manual
  - □ Dual die version designed to meet ASIL D requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A33003 Safety Manual
- Programmable via Manchester encoding on the output line to reduce external wiring and enable in-application programming when in PWM or SENT mode

Continued on next page...

DESCRIPTION

The A33003 is a 360° angle sensor IC that provides contactless high-resolution angular position information based on magnetic circular vertical Hall (CVH) technology. It has a system-on-chip (SoC) architecture that includes: a CVH front end, digital signal processing to calculate the angular position information, and selectable output protocols (SPI, SENT, or PWM). It also includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles for flexible programming of calibration parameters. The A33003 is ideal for automotive applications requiring 0° to 360° angle measurements and high levels of redundancy, such as electronic power steering (EPS), transmission actuators, and steer-by-wire (SBW) systems.

The A33003 includes on-chip 32-segment linearization. This can be used to calibrate out errors due to misalignment between the magnet and the sensor or imperfect magnetization of the target magnet (which can present itself as a misalignment of the magnet to the sensor).

The A33003 supports customer integration into safety-critical applications.

The A33003 is available in a single or dual die 14-pin TSSOP package (suffix LU). The package is lead (Pb) free with 100% matte-tin leadframe plating. The 1 mm thin package reduces the minimum air gap between the CVH transducer and the target magnet.

PACKAGE:
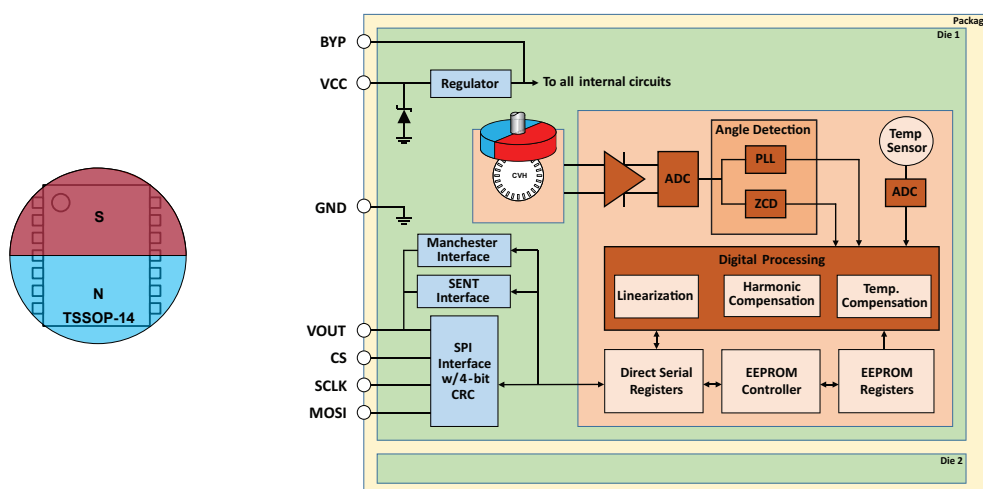
Not to scale
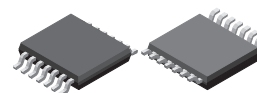
14-pin TSSOP
(Suffix LU)

Figure 1: A33003 Magnetic Circuit and IC Diagram

FEATURES AND BENEFITS (continued)

- Digital output format selectable between SPI, SENT, or PWM
- SENT output is SAEJ2716 JAN2010 compliant with Allegro proprietary enhancements
  □ Customer-programmable SENT tick times ranging from 0.5 to 7.9 μs
- On-chip EEPROM for storing factory and customer calibration parameters
  □ Integrated charge pump allows in-application programming without any requirement for high voltages to be supplied to the device during programming
  □ Single-bit error correction, dual-bit error detection error correction control (ECC)
- Supports operation in harsh conditions, required for automotive and industrial applications
  □ Operating temperature range from –40°C to 150°C
  □ Operating supply voltage range from 4.5 to 5.5 V, absolute maximum of 28 V
- Loss of power is indicated by reset flag
- 10 MHz SPI for low latency angle and diagnostic information;

enables multiple independent ICs to be connected to the same bus
  □ 4-bit CRC
- Multiple programming / configuration formats supported
  □ The system can be completely controlled and programmed over SPI or Manchester protocol, including EEPROM writes
  □ For system with limited pins available, writing and reading can be performed over VOUT pin
  □ 1 mm thin surface mount TSSOP package to minimize air gap from target magnet to the CVH transducer for improved field strength

SELECTION GUIDE

Part Number	Hot Trim Temperature	Interface Voltage [1]	System Die	Package	Packing
A33003LLUATR	150°C	3.3 V	Single	14-pin TSSOP	4000 pieces per 13-inch reel
A33003LLUATR-125	125°C	3.3 V			
A33003LUBTR-DD	150°C	3.3 V	Dual		
A33003LUBTR-DD-125	125°C	3.3 V			

[1] Contact Allegro MicroSystems for 5.0 V interface availability.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles, respecting T_J(max)	28	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	–18	V
VOUT Pin	V_{OUT}		18	V
All other Pins Forward Voltage	V_{IN}		5.5	V
All Other Pins Reverse Voltage	V_R		0.5	V
Operating Ambient Temperature	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LU-14 package; measured on JEDEC JESD51-7 2s2p board	82	°C/W

Table of Contents

PINOUT DIAGRAMS AND TERMINAL LIST TABLES

Pinout Diagram

LU 14-Pin TSSOP, Single Die

SCLK	1	○	14	GND
MOSI/SA1	2		13	GND
CS/SA0	3		12	GND
VOUT	4		11	GND
GND	5		10	GND
BYP	6		9	GND
VCC	7		8	GND
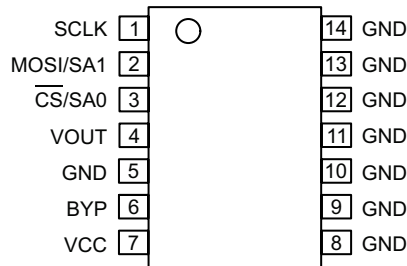
Terminal List Table, Single Die

Pin Number	Pin Name	Function
1	SCLK	SPI: Clock input terminal.
2	MOSI/SA1	SPI: Master-Out Slave-In. Manchester/SENT: Sets bit 1 of address field. Tie to BYP for a logic 1, GND for a logic 0.
3	CS/SA0	SPI Chip Select terminal, active low input. Manchester/SENT: Sets bit 0 of address field. Tie to BYP for a logic 1, GND for a logic 0.
4	VOUT	SPI: Master In / Slave Out, push-pull. SENT/PWM: Input / Output, open drain. Manchester: Input / Output, push-pull.
5, 8-14	GND	Device ground terminal. All GND pins should be connected together.
6	BYP	External bypass capacitor terminal for internal regulator.
7	VCC	Power supply.

Pinout Diagram

LU 14-Pin TSSOP, Dual Die

SCLK_1	1	○	14	VCC_2
MOSI/SA1_1	2		13	BYP_2
CS/SA0_1	3		12	GND_2
VOUT_1	4		11	VOUT_2
GND_1	5		10	CS/SA0_2
BYP_1	6		9	MOSI/SA1_2
VCC_1	7		8	SCLK_2
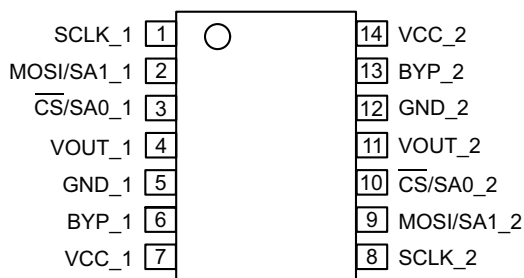
Terminal List Table, Dual Die

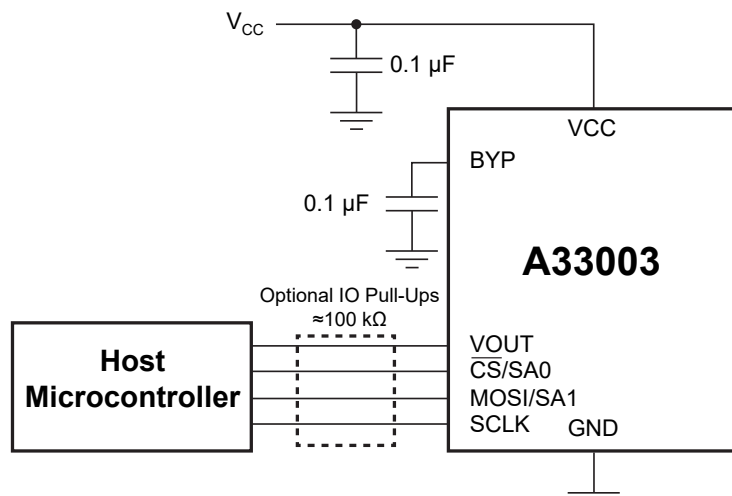| Pin Number	Pin Name	Function
1	SCLK_1	SPI: Clock input terminal. (Die 1)
2	MOSI/SA1_1	SPI: Master-Out Slave-In. Manchester/SENT: Sets bit 1 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 1)
3	CS/SA0_1	SPI Chip Select terminal, active low input. Manchester/SENT: Sets bit 0 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 1)
4	VOUT_1	SPI: Master In / Slave Out, push-pull. SENT/PWM: Input / Output, open drain. Manchester: Input / Output, push-pull. (Die 1)
5	GND_1	Device ground terminal. (Die 1)
6	BYP_1	External bypass capacitor terminal for internal regulator. (Die 1)
7	VCC_1	Power supply. (Die 1)
8	SCLK_2	SPI: Clock input terminal. (Die 2)
9	MOSI/SA1_2	SPI: Master-Out Slave-In. Manchester/SENT: Sets bit 1 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 2)
10	CS/SA0_2	SPI Chip Select terminal, active low input. Manchester/SENT: Sets bit 0 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 2)
11	VOUT_2	SPI: Master In / Slave Out, push-pull. SENT/PWM: Input / Output, open drain. Manchester: Input / Output, push-pull. (Die 2)
12	GND_2	Device ground terminal. (Die 2)
13	BYP_2	External bypass capacitor terminal for internal regulator. (Die 2)
14	VCC_2	Power supply. (Die 2)

Figure 2: A33003 Typical Setup

* V_S should match IO voltage level (3.3 V or 5.0 V).
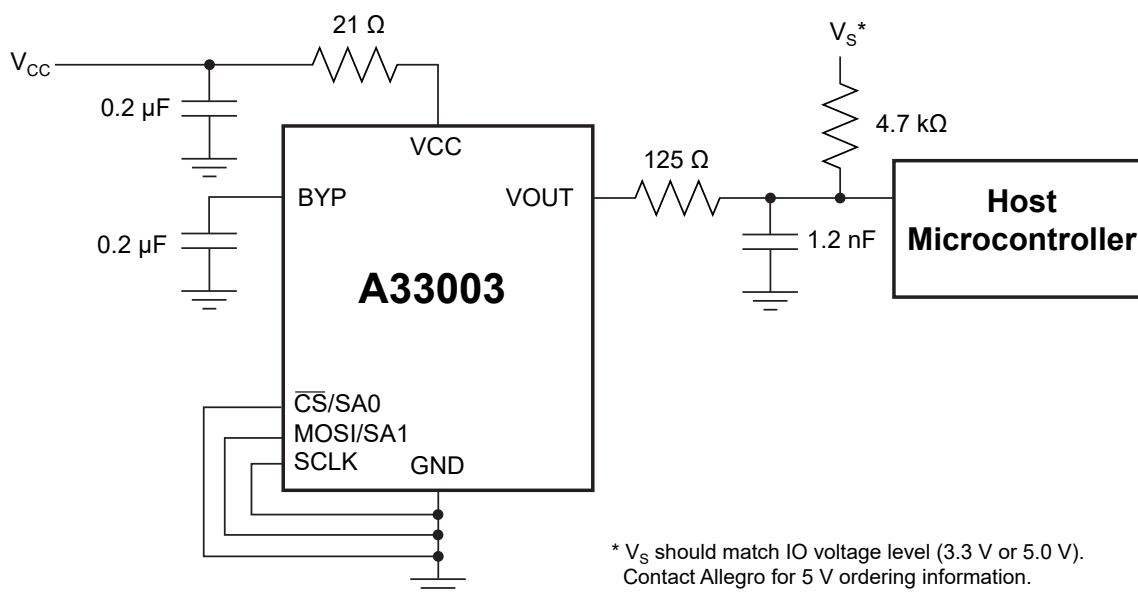Contact Allegro for 5 V ordering information.

Figure 3: A33003 Reference Design for Stringent EMC Requirements

OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	Customer supply	4.5	–	5.5	V
Supply Current	I_{CC}	Each die	11	13	16	mA
Undervoltage Flag Threshold	V_{UVD}	dV/dt = 1 V/ms, A33003 sampling enabled	4.5	–	4.7	V
Supply Zener Clamp Voltage	V_{ZSUP}	$I_{CC} = I_{CC(max)}$ + 3 mA, T_A = 25°C	26.5	–	–	V
Reverse Battery Current	I_{RCC}	V_{RCC} = –18 V, T_A = 25°C	–	–	–5	mA
Power-On Time [2]	t_{PO}	Power-on diagnostics disabled	–	15	–	ms
Bypass Pin Output Voltage [3]	V_{BYP}	T_A = 25°C, C_{BYP} = 0.1 µF, 3.3 V interface	2.93	3.3	3.63	V
		T_A = 25°C, C_{BYP} = 0.1 µF, 5.0 V interface, V_{CC} = 5 V	4	–	5.5	V
Digital Oscillator Frequency	f_{OSC}	Main digital oscillator	28	32	36	MHz
SPI INTERFACE SPECIFICATIONS (for 3.3 V interface)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{HL}	VOUT pins, C_L = 20 pF	2.93	3.3	3.63	V
SPI Output Low Voltage	V_{OL}	VOUT pins, C_L = 20 pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS (for 5.0 V interface) (*Contact Allegro for 5 V SPI ordering information*)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{HL}	VOUT pins, C_L = 20 pF	4	5	–	V
SPI Output Low Voltage	V_{OL}	VOUT pins, C_L = 20 pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency [4]	f_{SCLK}	VOUT pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle [4]	D_{fSCLK}	SPI_{CLKDC}	40	-	60	%
SPI Frame Rate [4]	t_{SPI}	Assuming a 16-bit SPI packet	5.8	–	588	kHz
Chip Select to First SCLK Edge [4]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [4]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [4]	t_{DAV}	Data output valid after SCLK falling edge	–	–	50	ns
MOSI Setup Time [4]	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time [4]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time [4]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [4]	C_L	Loading on digital output (VOUT) pin	–	–	20	pF

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
MANCHESTER INTERFACE SPECIFICATIONS							
Bit Rate		Defined by the input message bit rate sent from the external controller		4	–	40	kbps
Bit Time	t_{BIT}	Data bit pulse width at 4 kbps		243	250	257	µs
		Data bit pulse width at 100 kbps		9.5	10	10.5	µs
Bit Time Error	err_{TBIT}	Deviation in t_{BIT} during one command frame		–11	–	11	%
Read Delay	t_{START_READ}	Delay from the trailing edge of a Read command frame to the leading edge of the Read Acknowledge frame		$2 \times t_{BIT}$	–	–	µs
Bit Time Delay	t_b			–	2	–	t_{BIT}
Access Code Timeout	t_{msgRX}			–	–	300	µs
Interrupt Pulse Hold Time	t_{HOLD}	SSENT – Short	F_AUX	56	–	70	ticks
		SSENT – Long	F_AUX	216	–	264	ticks
		ASENT	F_AUX	56	–	70	ticks
		SENT	Aux. Interrupt Pulse	30	–	–	ticks
		TSENT	Aux. Interrupt Pulse	30	–	–	ticks
		PWM	Aux. Interrupt Pulse	2× PWM period [5]	–	–	µs
Deglitch Gate Time	t_{GATE}			1.0	–	–	µs
INPUT SIGNAL VOLTAGE							
Manchester Code High Voltage	$V_{MAN(H)}$	Applied to PWM/MISO/SENT line		2.8	–	V_{CC}	V
Manchester Code Low Voltage	$V_{MAN(L)}$	Applied to PWM/MISO/SENT line		0.0	–	1.2	V
OUTPUT SIGNAL VOLTAGE							
Manchester Code High Voltage	$V_{MAN(H)}$	Minimum R_{PULLUP} = 5 kΩ		$0.9 \times V_S$	–	–	V
		Maximum R_{PULLUP} = 50 kΩ		$0.7 \times V_S$	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	5 kΩ < R_{PULLUP} < 50 kΩ		–	–	0.1	V

Continued on the next page…

OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency [4]	f_{PWM}	PWM Frequency Min Setting, T_A in specification	–	98	–	Hz
		PWM Programmable Options	–	128	–	codes
		PWM Frequency Max Setting, T_A in specification	–	3.125	–	kHz
PWM Output Low Clamp	$D_{PWM(min)}$	Corresponding to digital angle of 0x000	–	5	–	%
PWM Output High Clamp	$D_{PWM(max)}$	Corresponding to digital angle of 0xFFF	–	95	–	%
PWM Output Resolution	RES_{PWM}		–	12	–	bit
PWM Output Saturation Voltage	$V_{SAT\_LOW(PWM)}$	Output current = –1 mA, V_{CC} = 5 V, output FET on	–	–	0.25	V
PWM Current Limit	$I_{LIMIT(PWM)}$	Output FET on, T_A = 25°C	20	36	45	mA
PWM Output Impedance [4]	$R_{ON(PWM)}$	PWM driver impedance when pulling to logic low; T_A = 25°C	40	–	250	Ω
SENT SPECIFICATIONS [4]						
SENT Tick Time	t_{TICK}	All SENT Modes [6]	0.5	–	7.9375	µs
SENT Tick Time Tolerance	TOL_{tTICK}	All SENT Modes	–15	–	15	%
SENT Output Trigger Thresholds	$V_{SENTtrig(L)}$	V_{OUT} falling, 3.3 V digital	–	–	1.2	V
	$V_{SENTtrig(H)}$	V_{OUT} rising, 3.3 V digital	2.8	–	–	V
SENT Output Saturation Voltage	$V_{SAT(LOW)}$	Output current = –4.7 mA, V_{CC} = 5 V, output FET on	–	–	0.45	V
SENT Output Current Limit	I_{LIMIT}	Output FET on, T_A = 25°C	20	36	45	mA
SENT Output Load Resistance	$R_{L(PULLUP)}$	Output current ≥ –10 mA	1.2	–	–	kΩ
Trigger Delay Time [7]	t_{dSENT}	From end of trigger pulse to beginning of SENT message frame (TSENT and Shared SENT)	7	–	–	ticks
SENT Output Impedance [4]	$R_{ON(SENT)}$	SENT driver impedance when pulled to logic low; T_A = 25°C	40	–	250	Ω
BUILT-IN SELF TEST						
Logic BIST Time	t_{LBIST}	Configurable to run on power-up or on user request	–	30	–	ms
Circular Vertical Hall Self-Test Time	t_{CVHST}	Configurable to run on power-up or on user request	–	52	–	ms

Continued on the next page…

OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MAGNETIC CHARACTERISTICS						
Magnetic Field	B	Range of input field	–	–	900	G [1]
ANGLE CHARACTERISTICS						
Output [8]	RES_{ANGLE}	Both 12 and 15 bit angle values are available via SPI	–	12/15	–	bit
Angle Refresh Rate [9]	t_{ANG}	No averaging	–	2.0	–	µs
Response Time [4]	$t_{RESPONSE}$	Angular latency	–	17	–	µs
Effective Resolution [12]		B = 300 G [1], T_A = 25°C	–	12.5	–	bits

[1] 1 G (gauss) = 0.1 mT (millitesla). Recommended minimum field is 300 G.
[2] During the power-on phase, the A33003 SPI transactions will be valid within ≈ 300 µs of power on (with no self-tests). Angle reading requires full t_{PO} to stabilize.
[3] The output voltage specification is to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents to be expected during normal operation.
[4] Parameter is not guaranteed at final test. Determined by design.
[5] The minimum hold time for the Auxiliary interrupt, when the output is set for PWM, is double the PWM period. If the PWM frequency increases as a result of a diagnostic condition, the hold time is double the new PWM period at the diagnosis frequency.
[6] Tick times under 0.5 µs are available, but not guaranteed.
[7] The synchronization pulse delay is a minimum of 7 ticks but can be extended to cover Slot Marking in SSENT.
[8] RES_{ANGLE} represents the number of bits of data available for reading from the die registers.
[9] The rate at which a new angle reading will be ready.
[10] Error and noise values are with no further signal processing. Angle Noise can be reduced with internal filtering and slower Angle Refresh Rate value.
[11] This value represents 3-sigma or three times the standard deviation of the measured samples.
[12] Effective Resolution is calculated using the formula below:

$$Effective\ Resolution = log_2(360) - log_2\left(\frac{1}{n} \times \sum_{i=1}^{n}\sigma_i\right)$$

where σ is the Standard Deviation based on thirty measurements taken at each of the 32 angular positions, I = 11.25, 22.5, … 360.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ALLEGRO
microsystems

A33003LLUATR and A33003LLUBTR-DD PERFORMANCE CHARACTERISTICS:
Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions [1]	Min.	Typ.	Max.	Unit
Angle Error	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0	−1.2	±0.4	1.2	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0	−1.5	±0.5	1.5	degrees
Temperature Drift	$ANGLE_{DRIFT}$	T_A = 150°C, B = 300 G	−1.75	–	1.75	degrees
		T_A = −40°C, B = 300 G	–	±1	–	degrees
Angle Noise [2][3]	N_{ANG}	T_A = 25°C, B = 300 G, no internal filtering, target rpm = 0, 3 sigma noise	–	±0.19	–	degrees
		T_A = 150°C, no internal filtering, B = 300 G, target rpm = 0, 3 sigma noise	–	±0.25	–	degrees
Angle Drift Over Lifetime [4]	$Angle_{Drift\_Life}$	B = 300 G, average maximum drift observed following AEC-Q100 qualification testing	–	0.34	–	degrees

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Error and noise values are with no further signal processing. Angle Noise can be reduced with internal filtering and slower Angle Refresh Rate value.
[3] This value represents 3-sigma or three times the standard deviation of the measured samples.
[4] Maximum drift seen during AEC-Q100 testing was 1.076 degrees.

A33003LLUATR-125 and A33003LLUBTR-DD-125 PERFORMANCE CHARACTERISTICS:
Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions [1]	Min.	Typ.	Max.	Unit
Angle Error	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0	−1.2	±0.4	1.2	degrees
		T_A = 125°C, ideal magnet alignment, B = 300 G, target rpm = 0	−1.5	±0.5	1.5	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0	–	±1	–	degrees
Temperature Drift	$ANGLE_{DRIFT}$	T_A = 125°C, B = 300 G	−1.75	–	1.75	degrees
		T_A = 150°C, B = 300 G	–	±1	–	degrees
		T_A = −40°C, B = 300 G	–	±1	–	degrees
Angle Noise [2][3]	N_{ANG}	T_A = 25°C, B = 300 G, no internal filtering, target rpm = 0, 3 sigma noise	–	±0.19	–	degrees
		T_A = 125°C, no internal filtering, B = 300 G, target rpm = 0, 3 sigma noise	–	±0.25	–	degrees
		T_A = 150°C, no internal filtering, B = 300 G, target rpm = 0, 3 sigma noise	–	±0.25	–	degrees
Angle Drift Over Lifetime [4]	$Angle_{Drift\_Life}$	B = 300 G, average maximum drift observed following AEC-Q100 qualification testing	–	0.34	–	degrees

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Error and noise values are with no further signal processing. Angle Noise can be reduced with internal filtering and slower Angle Refresh Rate value.
[3] This value represents 3-sigma or three times the standard deviation of the measured samples.
[4] Maximum drift seen during AEC-Q100 testing was 1.076 degrees.

TYPICAL PERFORMANCE CHARACTERISTICS
The figures below show performance data from 30 samples of A33003LUBTR-DD devices.

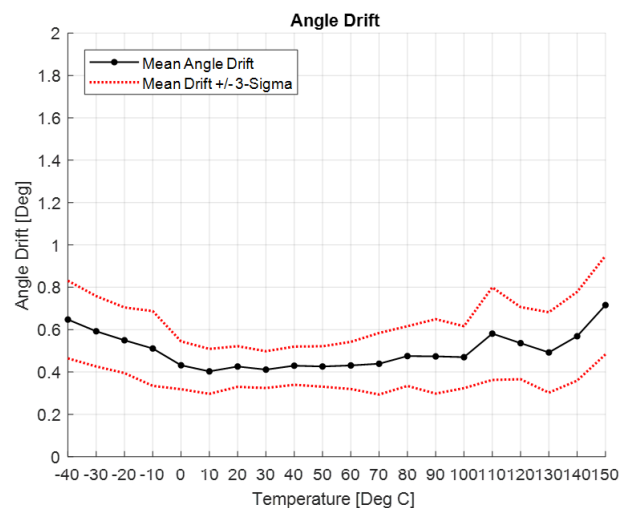**Figure 4: Peak Angle Error over Temperature (300 G)**

Figure 5: Maximum Absolute Drift Over Temperature (300 G)
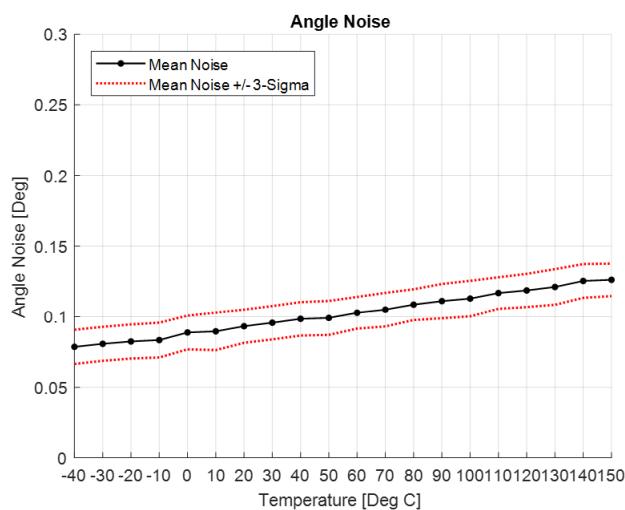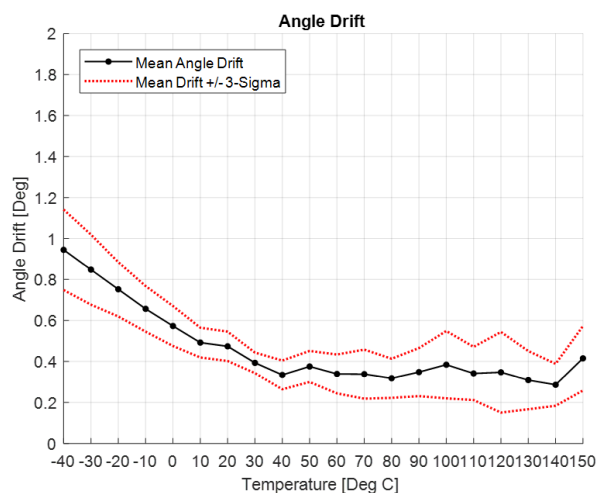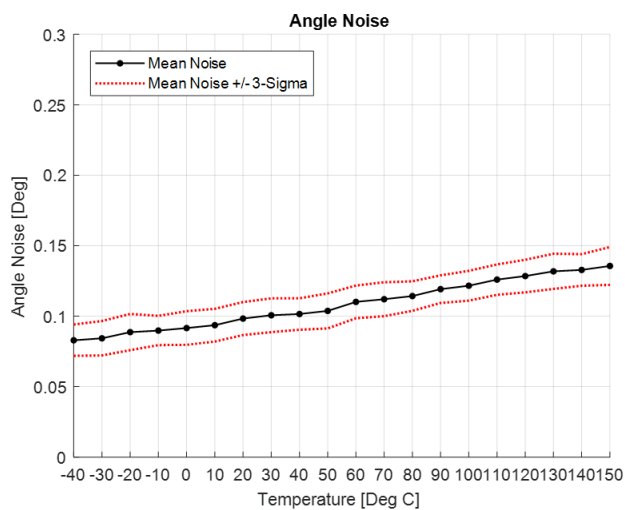

Figure 6: Noise Performance over Temperatures (3-Sigma, 300 G)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)
The figures below show performance data from 30 samples of A33003LUBTR-DD-125 devices.

Figure 7: Peak Angle Error over Temperature (300 G)

Figure 8: Maximum Absolute Drift Over Temperature (300 G)

Figure 9: Noise Performance over Temperatures (3-Sigma, 300 G)

FUNCTIONAL DESCRIPTION

Overview

The A33003 is a rotary position Hall-sensor-based device in a surface-mount package, providing solid-state consistency and reliability, and supporting a wide variety of automotive applications. The Hall-sensor-based device measures the direction of the magnetic field vector through 360° in the x-y plane (parallel to the branded face of the device) and computes an angle measurement based on the actual physical reading, as well as any internal parameters that have been set by the user. The output is used by the host microcontroller to provide a single channel of target data.

This device is an advanced, programmable system-on-chip (SoC). The integrated circuit includes a circular vertical Hall (CVH) analog front end, a high-speed sampling A-to-D converter, digital filtering, and digital signal processing.

Advanced offset, gain, and linearization adjustment options are available in the A33003. These options can be configured in onboard EEPROM, providing a wide range of sensing solutions in the same device.

Angle Measurement

The A33003 is capable of tracking magnet position at high speed. Performance up to 12,000 rpm has been verified by testing. Operation up to 30,000 rpm has been verified via design simulation. The A33003 has a typical output refresh rate of 2 µs.

Readout in SPI is possible with 12-bit resolution, with error flags included in the same word, or in 15-bit resolution without included error flags. Reading out the angle requires a minimum of 16 SPI clock cycles. A 20-bit SPI packet with 4 bits of CRC is also supported.

PWM output is always resolved to a 12-bit angle value.

When using SENT output, a 12-bit or 16-bit angle packet may be selected via the DATA_MODE field in EEPROM.

The sensor readout is processed and linearized in various steps. These are detailed in Figure 12.

System Level Timing

Internal registers are updated with a new angle value every t_{ANG}. Due to signal path delay, the angle is $t_{RESPONSE}$ old at each update. In other words, $t_{RESPONSE}$ is the delay from time of magnet sampling until generation of a processed angle value. SPI, which is asynchronously clocked, results in a varying latency depending on sampling frequency and SCLK speed. The values which are presented to the user are latched to the output registers on the first SCLK edge of the SPI output frame. This means that if the SPI clock is 10 MHz, the data will be clocked out after 1.6 µs. As the data was sampled in at the first clock edge at an age of maximum $t_{RESPONSE}$, its age after the SPI transaction has finished will be between 1.6 and $1.6 + t_{RESPONSE}$ µs.

Similar to SPI, when using the PWM output, the output packet is not synchronized with the internal update rate of the sensor. The angle is latched at the beginning of the carrier frequency period (effectively at the rising edge of the PWM output). Because of this, the age of the angle value, once read by the system micro-controller, may be up to $t_{response} + 1/f_{PWM}$.

The point within the SENT packet at which the angle value is latched varies with SENT configurations, although in all configurations, the SENT transmission time is the dominant contributor to delay. See the SENT section within this datasheet for a detailed description.

Power-Up

Upon applying power to the A33003, the device automatically runs through an initialization routine. The purpose of this initialization is to ensure that the device comes up in the same predictable operating condition every power cycle. This initialization routine takes time to complete, which is referred to as Power-On Time, t_{PO}. If diagnostics are enabled at Power-On, additional time is required for the device to complete the programmed tests. Regardless of the state of the device before a power cycle, the device will re-power with EEPROM shadow bits copied from the EEPROM, and serial registers in their default states. For example, on every power-up, the device will power with the "zero_offset" that was stored in the EEPROM. The extended write access field "write_adr" will be set back to its default value of zero.

PWM Output

The A33003 provides a pulse-width-modulated open-drain output, with the duty cycle (DC) proportional to measured angle. The PWM duty cycle is clamped at 5% and 95% for diagnostics purposes. A 5% DC corresponds to 0°; a 95% DC corresponds to 360°.
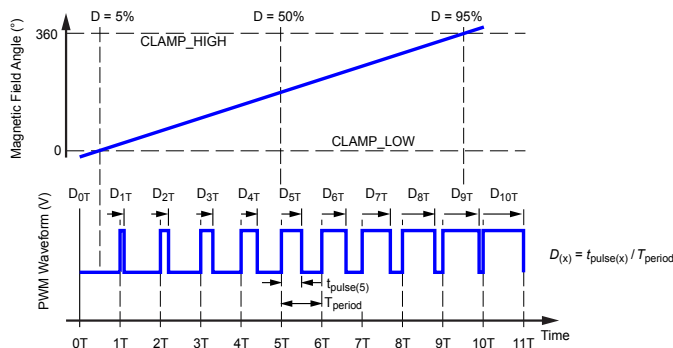

Figure 10: PWM Mode Outputs a Duty-Cycle Proportional To Sensed Angle

Within each cycle, the output is high for the first 5% and low for the last 5% of each period. The middle 90% of the period is a linear interpolation of the angle as sampled the start of the PWM period.
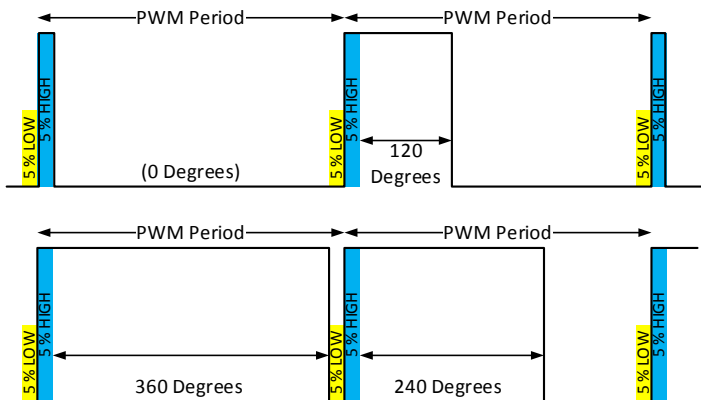

Figure 11: Pulse-Width Modulation (PWM) Examples

The angle is represented in 12-bit resolution and can never reach 360°. The maximum duty cycle high period is:

$$\text{DutyCycleMax} (\%) = (4095 / 4096) \times 90 + 5 .$$

PWM CARRIER FREQUENCY

The PWM carrier frequency is controlled via two EEPROM fields, both of which are found in the PWS row.

- PWM_FREQ
- PWM_BAND

Together these two fields allow 128 different PWM carrier frequencies to be selected.

Table 1: PWM Carrier Frequencies in Hz

		PWM_BAND							
		0	1	2	3	4	5	6	7
PWM_FREQ	0	3125	2778	2273	1667	1087	641	352	185
	1	3101	2740	2222	1613	1042	610	333	175
	2	3077	2703	2174	1563	1000	581	316	166
	3	3053	2667	2128	1515	962	556	301	157
	4	3030	2632	2083	1471	926	532	287	150
	5	3008	2597	2041	1429	893	510	275	143
	6	2985	2564	2000	1389	862	490	263	137
	7	2963	2532	1961	1351	833	472	253	131
	8	2941	2500	1923	1316	806	455	243	126
	9	2920	2469	1887	1282	781	439	234	121
	10	2899	2439	1852	1250	758	424	225	116
	11	2878	2410	1818	1220	735	410	217	112
	12	2857	2381	1786	1190	714	397	210	108
	13	2837	2353	1754	1163	694	385	203	105
	14	2817	2326	1724	1136	676	373	197	101
	15	2797	2299	1695	1111	658	362	191	98

ERROR REPORTING IN PWM

The PWM output can be configured to change state if certain errors occur. There are three options:

- No error reporting

- Tristate the PWM

- Halve the carrier frequency and represent the error via different duty cycles

Two EEPROM bits, "PEO" and "PES" control how errors are reported in PWM mode, both of which are in the PWS address row of EEPROM:

Table 2: PWM Error Output Enable Option (PEO)

Code	Description
0	PWM does not respond to errors.
1	PWM output responds to errors as selected with the PES field.

Table 3: PWM Error Select (PES)

Code	Description
0	PWM tristates on an error.
1	PWM carrier frequency halved and highest priority error output on PWM as selected duty cycle.

The error priority and corresponding duty cycle are shown in Table 4 below, with the high priority error dictating the PWM duty cycle.

Each error is individually enabled for PWM reporting, so that only events of interest interrupt the device output. These enable bits may be found within the PWE (0x18) EEPROM row.

Table 4: PWM Error Duty Cycle and Priority

| Error	Priority	Duty Cycle %	Description / Persistence
WDE	1 (highest)	5	Watchdog error. Permanent.
EUE	2	10.625	EEPROM uncorrectable error.
STF	3	16.25	Self-test failure. Permanent.
PLK	4	21.875	PLL not locked. Persists until PLL locks.
ZIE	5	27.5	Zero-crossing integrity error. Persists until goes away.
AVG	6	33.125	Angle averaging error. Outputs once then clears.
UV	7	38.75	Undervoltage (UVA and/or UVCC dependent on serial error masks). Persists until no unmasked undervoltage.
MSL	8	44.375	Persists until field strength higher than low threshold.
ESE	9	50	EEPROM correctable error. Outputs once then clears.
SAT	10	55.625	Persists until no saturation warnings.
MSH	11	61.25	Persists until field strength lower than high threshold.
TR	12	66.875	Persists until temperature within range.
TOV	13	72.5	Persists until cleared via the serial CTRL register.
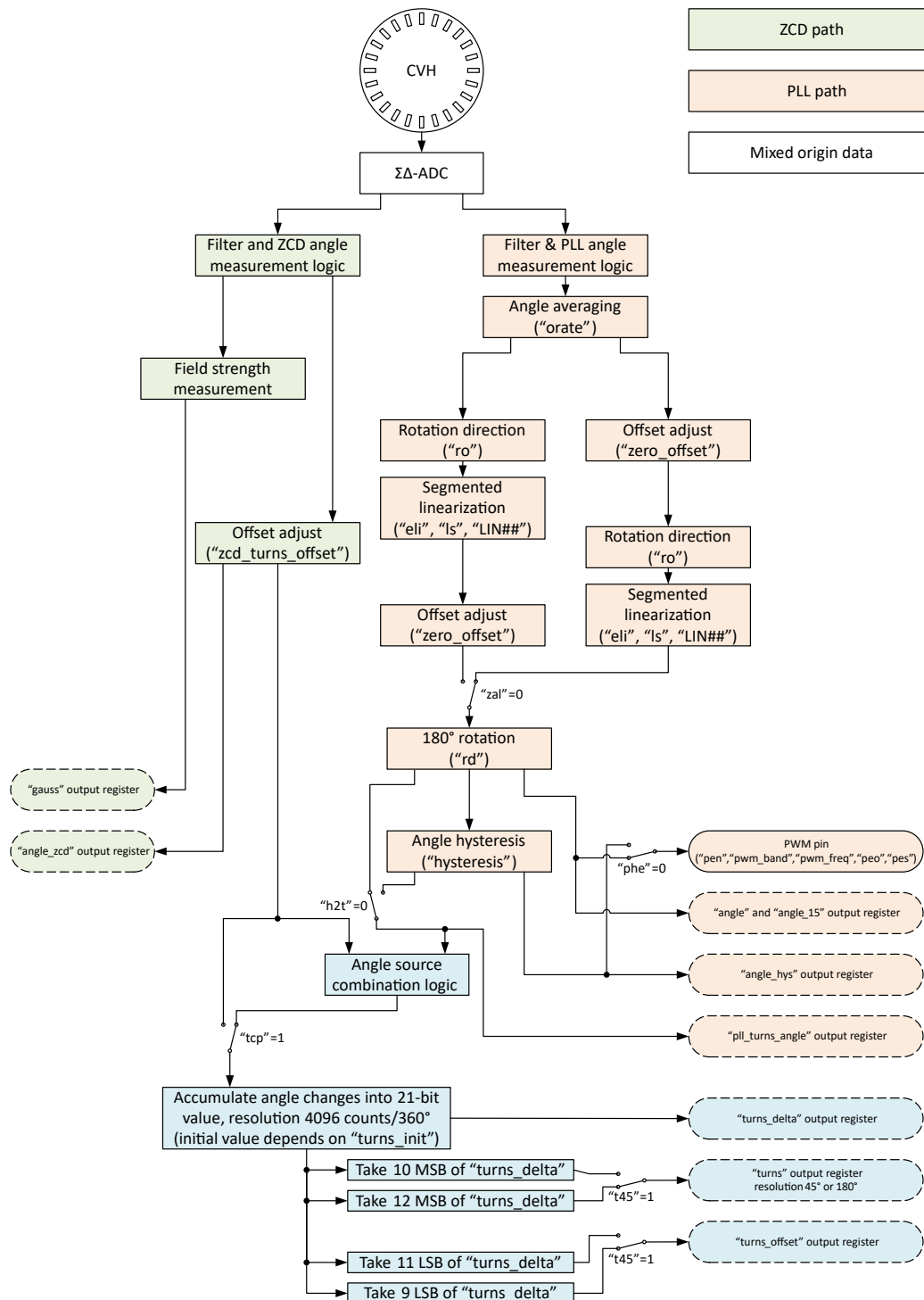
Figure 12: Angle Measurement – Sensor Readout Steps

Linearization

The A33003 contains linearization functionality. Linearization allows for conversion of the initially sensor-measured magnetic field data into customer-desired linear output. This can be used to correct minor imperfections in the encoder signal, or to allow motor commutation in side-shaft measurement setups.

Linearization converts the electrical angles (the angle as measured by the sensor front end) into mechanical angles (the actual angle of the encoder signal).

To use the linearization feature, it is most convenient to use the Allegro A33003 Samples Programmer Graphical User Interface (GUI). It allows the user to measure points along the mechanical rotation, calculate all parameters that need to be written into the sensor, and writes these values into the sensor. To use this function, the user must be able to read and control the mechanical angle.

The sensor performs linearization by taking the measured electrical angles and, depending on the angle measured, subtracting a linearization coefficient stored in EEPROM. There are 32 of these linearization coefficients in the EEPROM. The angle value at a sensor angle reading of 0.00, 11.25, 22.50, … 348.75 electrical degrees will be modified by the values in EEPROM fields LIN0, LIN1, LIN2, … LIN31. The EEPROM LIN values are subtracted from the electrical sensor angles, as shown in Table 5.

The LIN fields are 12-bit signed values. Each LIN coefficient has a range of –2048…+2047 LSB that corresponds to a correction of the electrical angle by +22.50…–22.49 degrees (EEPROM field "ls" = 0) or by +45.00…–44.98 degrees (EEPROM field "ls" = 1). When the electrical angle is between two of the linearization points, the sensor calculates the appropriate correction value for this angle by linear interpolation between the two coefficients next to the value. For example, if the sensor measures an angle of 5.625°, the output will be 5.625 – (LIN0 + LIN1) / 2.

Figure 13 is shown as an example of a nonlinear curve that is corrected by the sensor. In this example, the values of LIN0 through LIN4 are positive numbers, while LIN5 and LIN6 are negative numbers. The straight line interpolation between LIN points typically gives rise to some residual error, as the device is fitting a line to a non-linear error profile. Figure 14 shows an example of this.

The output delay of the A33003 is not affected by enabling or disabling linearization. If linearization is disabled, the EEPROM LIN fields can be used for other customer purposes.

Table 5: Linearization Coefficients

| Electrical angle (°) measured by sensor	Correction value Written in EEPROM	Output angle Visible on sensor output
0.00	LIN0	Output = 0.00 - LIN0
11.25	LIN1	Output = 11.25 - LIN1
22.50	LIN2	Output = 22.50 - LIN2
33.75	LIN3	Output = 33.75 - LIN3
45.00	LIN4	Output = 45.00 - LIN4
56.25	LIN5	Output = 56.25 - LIN5
67.50	LIN6	Output = 67.50 - LIN6
78.75	LIN7	Output = 78.75 - LIN7
90.00	LIN8	Output = 90.00 - LIN8
101.25	LIN9	Output = 101.25 - LIN9
112.50	LIN10	Output = 112.50 - LIN10
123.75	LIN11	Output = 123.75 - LIN11
135.00	LIN12	Output = 135.00 - LIN12
146.25	LIN13	Output = 146.25 - LIN13
157.50	LIN14	Output = 157.50 - LIN14
168.75	LIN15	Output = 168.75 - LIN15
180.00	LIN16	Output = 180.00 - LIN16
191.25	LIN17	Output = 191.25 - LIN17
202.50	LIN18	Output = 202.50 - LIN18
213.75	LIN19	Output = 213.75 - LIN19
225.00	LIN20	Output = 225.00 - LIN20
236.25	LIN21	Output = 236.25 - LIN21
247.50	LIN22	Output = 247.50 - LIN22
258.75	LIN23	Output = 258.75 - LIN23
270.00	LIN24	Output = 270.00 - LIN24
281.25	LIN25	Output = 281.25 - LIN25
292.50	LIN26	Output = 292.50 - LIN26
303.75	LIN27	Output = 303.75 - LIN27
315.00	LIN28	Output = 315.00 - LIN28
326.25	LIN29	Output = 326.25 - LIN29
337.50	LIN30	Output = 337.50 - LIN30
348.75	LIN31	Output = 348.75 - LIN31
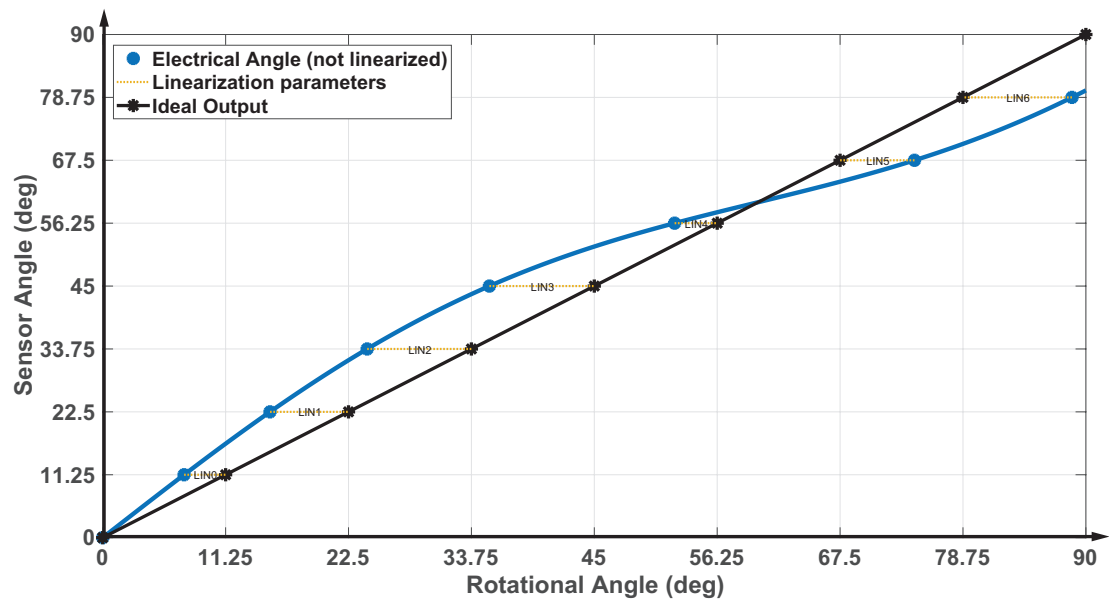
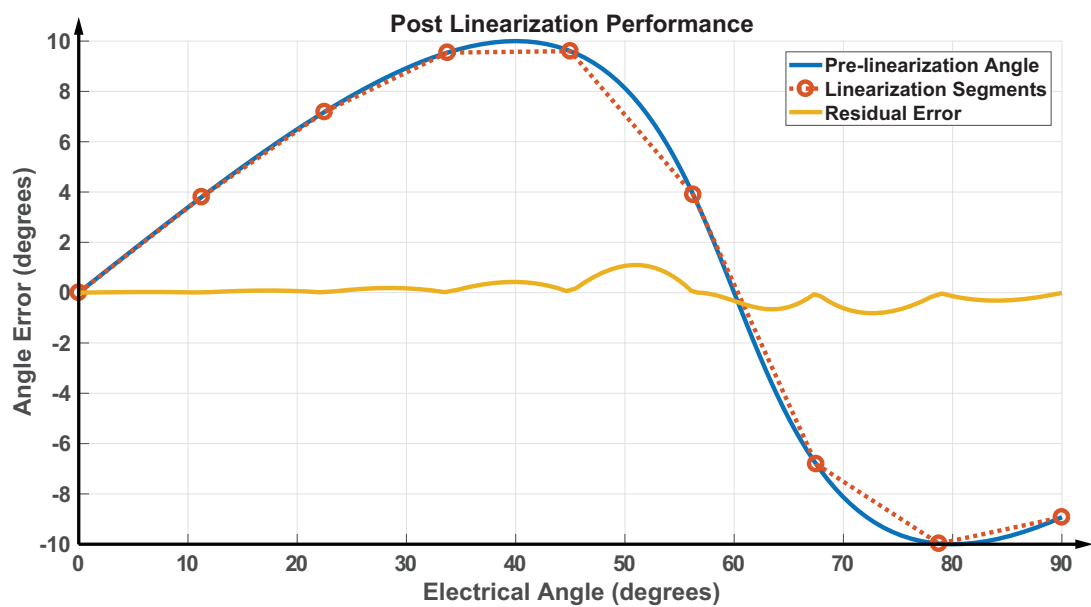**Figure 13: Linearization Example**

Figure 14: Post Linearization Error

Angle Hysteresis

Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. In the A33003, the hysteresis field (ANG.hysteresis) defines the width of an angle window at 14-bit resolution. Mathematically, the width of this window is:

$$ANG.hysteresis \times (360 / 16384) \text{ degrees} \qquad ,$$

giving a range of 0 to 1.384 degrees.

On the SPI or Manchester interface, the hysteresis-compensated angle can be read via an alternate register (HANG.angle_hys) at 12-bit resolution.

The effect of the hysteresis is shown in Figure 15. The current angle position as measured by the sensor is at the "head" of the hysteresis window. As long as the sensor (electrical) angle advances in the same direction of rotation, the output angle will be the sensor angle, minimizing latency. If the sensor angle reverses direction, the output angle is held static until the sensor angle exits the hysteresis window in either direction. If the exit is in the opposite direction of rotation where the "head" was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. The current direction of rotation, or "head" for the purposes of hysteresis, is viewable via the STA.rot bit, where 0 is increasing angle direction and 1 is in decreasing angle direction.

This behavior has the following consequences:

1. If the hysteresis window is greater than the output resolution, the output angle will skip consecutive resolution steps.

2. If there is jitter due to noise or mechanical vibration, especially at a static angle position or very slow rotation, the angle will tend to bias to one side of the window, depending on the direction of rotation as the angular velocity approaches zero (i.e., towards the current "head") rather than to the average position of the jitter.
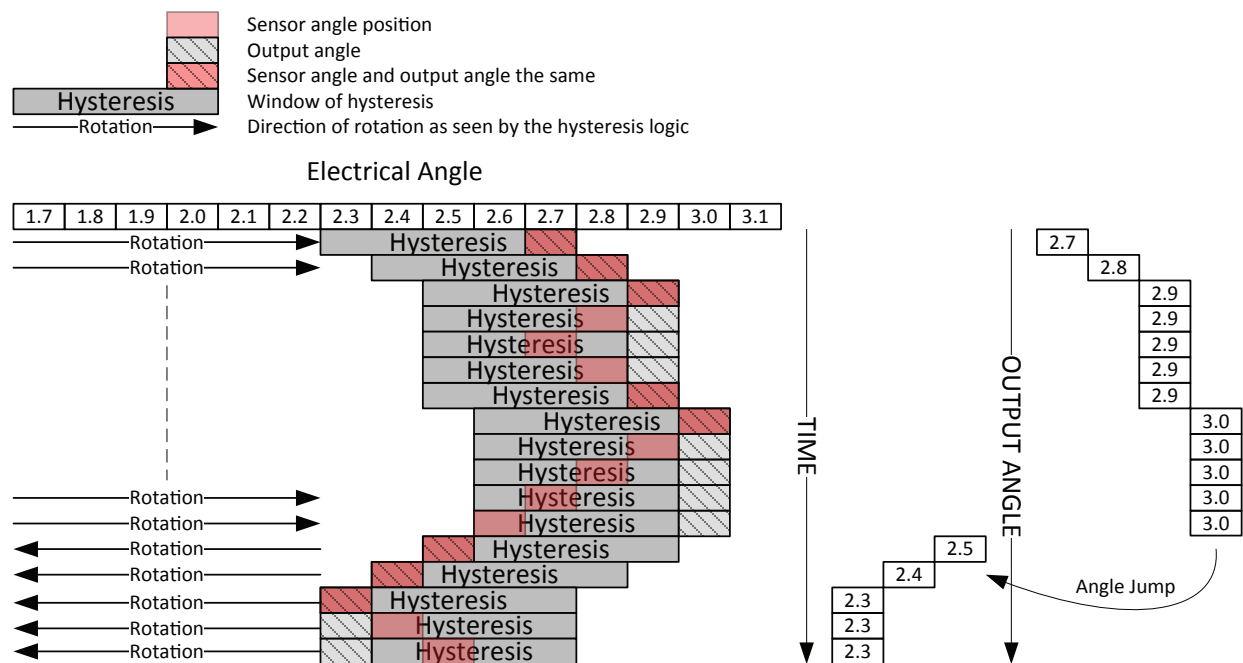

Figure 15: Effect of Hysteresis

Note: The rotation direction resets to 0, or increasing angle direction. At power-up or after LBIST, the hysteresis window will always be behind the initial angle position, so if hysteresis is enabled a decreasing angle direction of rotation will not register until the hysteresis window is past.

Turns Counting

Certain automotive angle sensing applications involve the magnetic target rotating multiple times. Thus, tracking the turns of the measured magnet becomes more important than knowing the specific angle at which the target sits. Examples of such applications include:

• Seat-belt passive safety systems

• EPS motor position

This implementation can also be used to measure exact angle in cases where the rotation is geared-up such that a slight angle rotation of the interested device results in multiple rotations of a target magnet which the sensor is measuring. For this reason, the A33003 includes a circuit that counts the rotational turns of a magnet. This feature also includes the ability to start up with a preset value, allowing the turns counter to persist through power-off periods, when combined with adequate system-level control. Traditionally, recovering the turns counter value was achieved by a combination of relatively complex mechanical and electrical components. The A33003 can help reduce system-level complexity and eliminate many system components by performing both the absolute angle measurement and the tracking of turns.

It is possible to use the ZCD signal path as the turns counter source. This is done by setting the tcp field in EEPROM to 0.

To read the total position of the magnetic encoder (angle in 12-bit resolution, as well as additional revolutions in 9 bits, sign-extended to 12 bits), a serial register turns_delta is provided. This 24-bit word accumulates the total changes in angle. The initial value of the register (zero, current angle, or current angle with turns_count zeroed) can be controlled using the EEPROM field turns_init, as detailed in Figure 17.

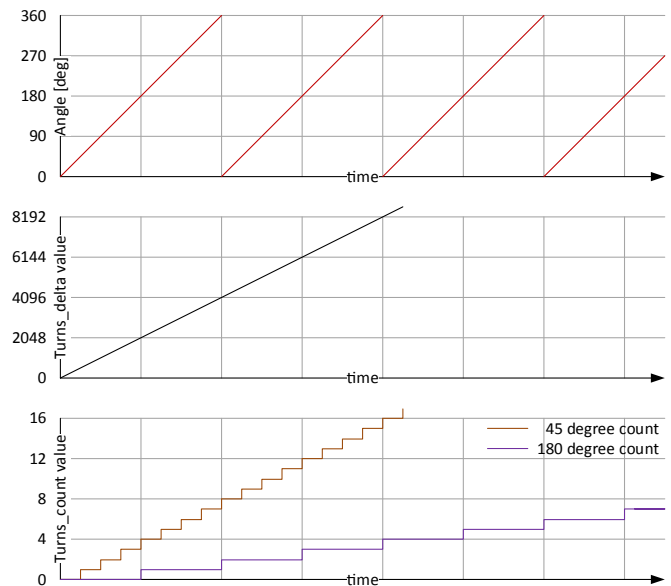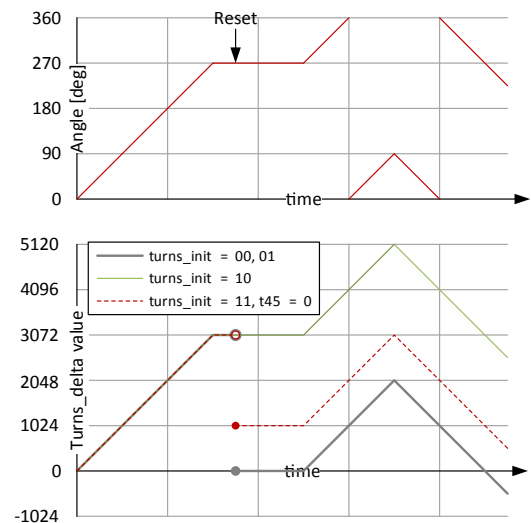**Figure 16: Turn Counting**

Figure 17: EEPROM field turns_init

Turns Counting Behavior on Power-Up

Turns tracking as measured by the IC is derived from the turns_delta register. This is a 21-bit register that tracks absolute angle across multiple magnetic rotations by tracking the change in angle from a reference position. The actual "turns" register (address 0x2C) is simply the upper bits from the turns_delta value. When configured in 180° turns mode (T45 set to '0'), the upper 10 bits are used; if in 45° mode (T45 set to '1'), the upper 12 bits are used to indicate the "turns". The A33003 is capable of tracking up to –512/+511 turns in 180° mode and –2048/+2047 in 45° mode.

turns_delta register																				
20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

11	10	9	8	7	6	5	4	3	2	1	0
SE	SE	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Turns register with T45 = '0'
SE = sign extended

turns_delta register																				
20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

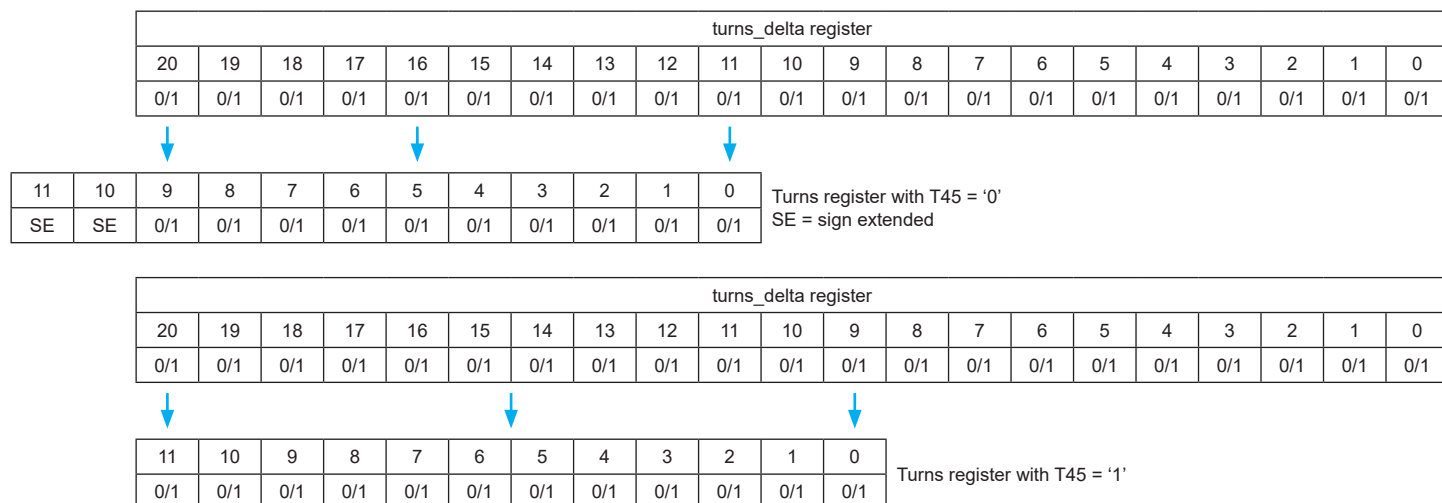| 11	10	9	8	7	6	5	4	3	2	1	0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Turns register with T45 = '1'

Figure 18: Turns Register

The reference position from which the turns_delta is measured will impact the initial turns count value. The turns_init field has the following options controlling this:

Table 6: turns_init (EEPROM 0x1D bits 19:18)

turns_init	Description
00	Turns counter will be zeroed on power-up. Turns are tracked relative to the angle observed on power-up. turns_delta = 0 at power-up.
01	
10	Turns counter will be set relative to the sensor's defined 0 position, which may be a non-zero number. turns_delta will be set to the angle observed on power-up.
11	Turns counter value initialized to zero, but increments on the 0/180 or 45 boundaries as observed by the IC (set via the T45 field). turns_delta register will be initialized with an offset based on the T45 register.

Figure 17 illustrates how the turns_init field controls the starting turns count value. In Figure 17, the angle is constantly increasing, up to 270°, after which a sensor rest occurs.

For a turns_init value of 00_2 or 01_2, the turns_delta register measures the change in position relative to the observed angle on power-up. As such, the turn's value is initialized to '0' on sensor reset.

With turns_init set to 10_2, the turns_delta value represents the difference in position relative to the sensor's defined 0° position; put more simply, the turns_delta is initialized to the angle observed on power-up. As shown in Figure 17, once the reset occurs, the turn_delta register is loaded with 3072 codes, which is 270° in 12-bit resolution. Depending on the T45 setting, this will be reflected as a turn value of 1 (in 180° mode) or 6 (in 45° mode).

When the turns_init field is set to 11_2, the turns count is initialized to 0, and the increment/decrement points for turns counting are fixed to either the 0/180° or the 0/45/90/135/180/225/270/315 boundaries, based on the T45 field. The turns_delta register will be loaded with the angular distance between two adjacent boundaries (0/180° or a multiple of 45°). For example, in Figure 17, the T45 bit is set to 0, enabling 180° mode. The turn's value in this case is 0. The angle on power-up is 270°, which is 50% between 180° and 360°; to reflect this, the turns_delta register is loaded with 1024 codes indicating it is halfway between one turn (one turn being 180° in 12-bit resolution, or 2048 codes).

Setting the Turns Count Value

There are two ways to modify the value of the turns counter.

- Using the turns counter reset function
- By writing the turns_delta value to register EWD and loading it into turns_delta

INVOKING A TURNS COUNTER RESET

Resetting the turns counter is a command invoked using the "special" field of the register CTRL.

CHANGING OR RESTORING TURNS_DELTA VALUE

It is possible to load a desired value into the turns counter register. This may be useful if a certain externally stored value should be set again following a power loss. The turns counter register itself cannot be written directly. Instead, the writing action is an indirect one using the following steps:

1. Writing should only be done when the system is stable, as indicated by the STA.aok bit field.
2. Write the desired 21-bit value of turns_delta into the serial registers EWDH and EWDL in little-endian format. Example:
   A. The user wants to set the turns_delta to value 10441.32° (29 rotations and 1.32° current angle), so they must write $(10441.32 / 360) \times 4096 = 118799 = 0x01D00F$.

B. Write the lower 16 bits into register EWDL and the higher 5 bits into EWDH, with leading zeroes to make the 16-bit value to write. This results in writing 0x0001 to EWDH (0x04:0x05) and 0xD00F to EWDL (0x06:0x07).

3. Write the value 0x03 to the field "special" and write 0x46 to the field "initiate_special".

4. The sensor behavior to process the setting will depend on the setting of the turns_init EEPROM field:

A. When turns_init = 00_2 or 01_2, the value will be copied to turns_delta, and subsequent angle changes will be accumulated on top of this value. Using this is not recommended for scenarios in which one wants to restore a saved value, as small offset changes / noise errors will accumulate every time such a write is performed.

B. When turns_init = 10_2 or 11_2, the value will be compared to the currently sensed angle. The turns_delta field will 'snap' to the closest value matching the sensed angle. Errors in position of <180° will be removed this way. This method is recommended for scenarios when one wants to restore a saved turns count value, but the measured angle may have changed slightly in the meantime.

ALLEGRO microsystems

DEVICE PROGRAMMING INTERFACE

The A33003 can be programmed in two ways:

- Using the *SPI interface* for input and output

- Using a *Manchester protocol* on the VOUT pin.

The A33003 features an internal charge pump and does not require high-voltage pulses to write EEPROM.

All setting fields and all data fields of the sensor can be read and written using both protocols. Locking the EEPROM from changes will lock EEPROM write access from both protocols.

A separate setting to completely disable the Manchester interface is available in the PWS.dm field of the EEPROM. Using this setting will cause the sensor to ignore any commands entered using Manchester protocol. The SPI interface will not be disabled by disabling the Manchester interface.

For details regarding the programming procedures, contact your Allegro representative.

SWITCHING BETWEEN THE DIFFERENT OUTPUT PROTOCOLS

The A33003 supports four output protocols (SPI, Manchester, SENT, PWM), all of which overlap with the same pin. Below is the hierarchy of precedence for control of the MISO pin.

- SPI, when set with SPO bit within the serial register.

- Manchester communication (when Auxiliary Interrupt Pulse is sent).

- PWM, when set via the PWS.PEN bit in EEPROM.

- SENT, when enabled via the SENT_MODE field in EEPROM.

- Manchester, when neither PWM or SENT is enabled; SPI, when Manchester is disabled.

When the SPO bit is set, the SPI interface will immediately override all other output protocols—this includes Manchester. If this bit is set via the Manchester interface, the device will end the Manchester interface, and stop responding to Manchester communication until SPO is cleared.

INTERFACE STRUCTURE

The primary serial interface registers are used for direct writes and reads by the host controller for frequently required information. All forms of communication operate through these registers, whether it be via SPI or Manchester. These registers also provide a data and address location for accessing extended memory locations under control of the onboard processor.

EEPROM writing requires additional procedures. For more information, see the EEPROM Description and Programming section.

Contact your Allegro representative for additional information.

SPI Interface

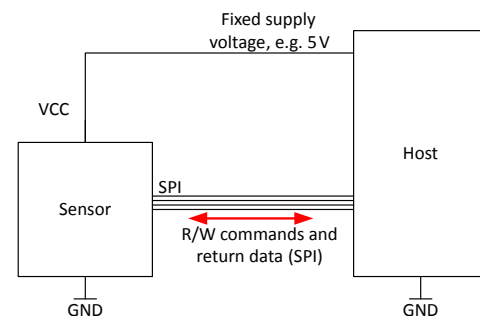The setup for programming using the SPI interface is given in Figure 19.

Figure 19: SPI Interface Programming Setup

SPI INTERFACE TIMING

The SPI interface operates in pure Slave mode, with the Master controlling the SCLK, MOSI, and CS lines. The Master can maximize data throughput, up to $f_{SCLK(max)}$ of 10 MHz. The figures below show the timing for Read and Write cycles.
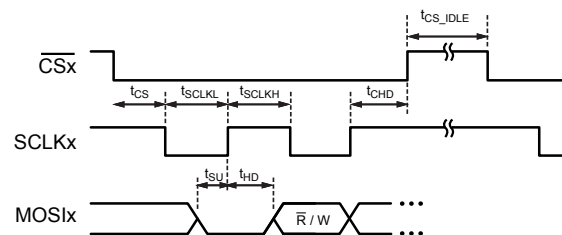

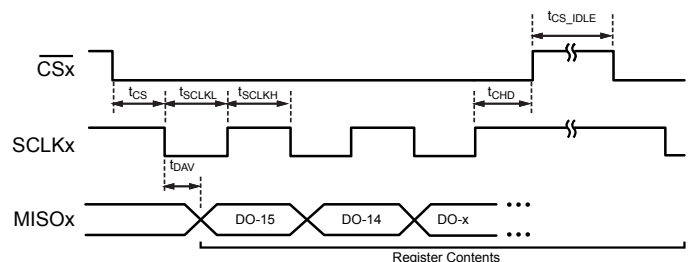**Figure 20: A33003 SPI Interface Timings Input**

Figure 21: A33003 SPI Interface Timings Output

SPI MESSAGE FRAME SIZE

The SPI interface requires either 16, 17, or 20-bit packet lengths. The extended 20-bit SPI packet allows 4-bit CRC to accompany every data packet. The 17-bit packet is only allowed when the EEPROM/Shadow bit S17 is set to '1'.

The purpose of the 17-bit SPI option is to allow a delayed reading of the MISO line on the host side. Some hosts allow data to be sampled from the slave on the falling edge of SCLK. This is typically done in the case of long interface delays caused by large line capacitances or very long cables. Due to the sampling on the falling edge, an additional 17th clock is required for the 16 bits of information.

If more or less clock pulses than expected are detected by the sensor during a SPI transaction, the interface warning WARN.IER will set. This would be anything other than 16 or 20 when S17 = '0', or anything other than 17 when S17 = '1'.
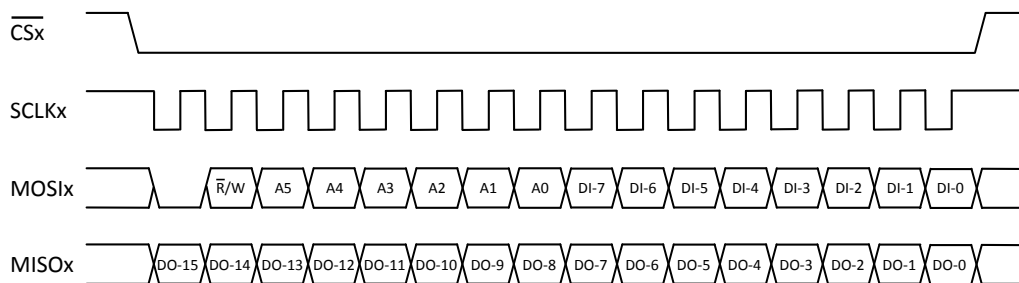
Figure 22: Sixteen Bit SPI Transaction
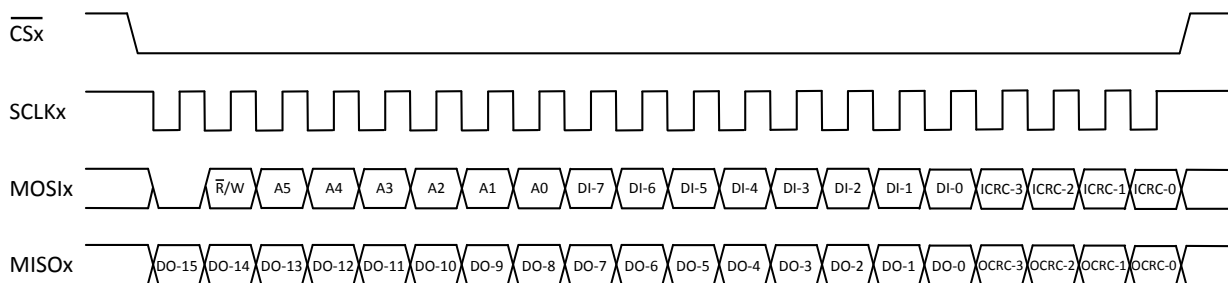
Figure 23: Twenty Bit SPI Transaction

SPI OUTPUT VOLTAGE LEVELS

The A33003 can operate in either 3.3 or 5 V SPI mode. Contact Allegro MicroSystems for more information.

WRITE CYCLE OVERVIEW

Write cycles consist of a 1-bit low, a 1-bit $\overline{R}/W$ asserted high, 6 address bits (corresponding to the primary serial register), 8 data bits, and 4 optional CRC bits. To write a full 16-bit serial register, two Write commands are required (even and odd byte addresses). MOSI bits are clocked in on the rising edge of the Master-generated SCLK signal. The complete SPI packet is latched on the rising edge of the Master-generated ($\overline{CS}$) signal.

The simultaneous MISO signal output represents the contents of the corresponding die SPI read packet, including 16 data bits and 4 optional CRC bits—automatically included if a 17th SCLK edge is detected. The data bits correspond to the register contents selected during the previous read command. In the event when the previous command was a Write, the device will by default output the angle register (0x20). If no previous command was sent, i.e., first SPI packet after POR, then the data sent by the device is indeterminate.
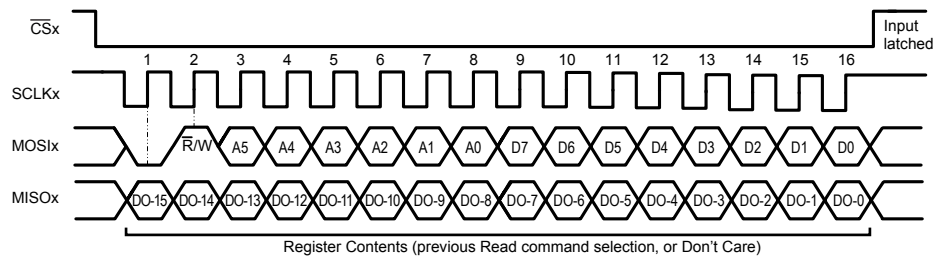

Figure 24: SPI Write Example

READ CYCLE OVERVIEW

Read cycles have two stages: a Read command to select a serial register address, followed by another Read command to transmit the data from the selected register. Both commands consist of a 1-bit low, a 1-bit $\overline{R}$/W asserted low, 6 address bits identifying the target register, and 8 data bits (all zeroes because no data is being written).

In the first stage, as with the Write command, Read command MOSI bits are clocked-in on the rising edge of the Master generated SCLK signal and data latched on the rising edge of the ($\overline{CS}$) signal. During the first Read stage, the simultaneous MISO signal output is the content of the SPI read data from the previous Read command.

In the second stage, the Read command continues on the next

falling edge of the Master-generated ($\overline{CS}$) signal. The MISO bits are the contents of the register selected during the first stage, read 16 bits at a time. The MISO bits transmit on the falling edge of the SCLK signal, such that the Master can sample them on the SCLK rising edges.

Because a SPI Read can transmit 16 data bits at one time, the primary serial registers are built from one even and one odd byte, the entire 16-bit contents of one serial register may be transmitted with one SPI frame. This is accomplished by providing an even serial address value. If an odd value address is sent, only the contents of the single byte will be returned, with the eight most significant bits within the SPI packet set to zero.

Example: To read all 16 bits of the Error register (0x24:0x25), a SPI read request with the address bits set to 0x24 should be sent. If only the 8 LSBs are desired, the address 0x25 should be used.
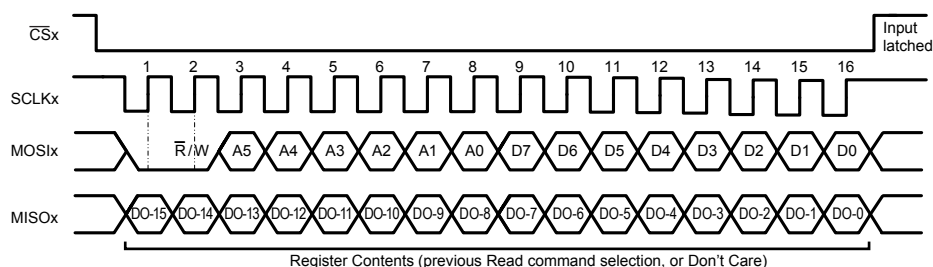

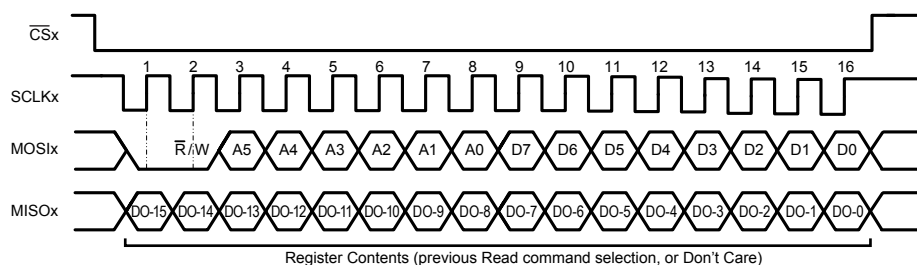**Figure 25: SPI Read Example, Register Selection**

Figure 26: SPI Read Example, Data Output
From Selected Register

CRC

If the user wants to check the data coming from the sensor, it is possible to use 20-bit SPI frames. Without additional setting required, a 4-bit CRC is automatically generated and placed on the MISO line if more than 16 bits are read from the sensor.

The four additional CRC bits on the MOSI line coming from the host are ignored by the sensor, unless the "PWI.sc" bit is set within EEPROM (0x1B, bit 0). When the incoming CRC check is enabled, an incoming SPI packet with an incorrect CRC will be discarded, and the CRC error flag set in serial register "warn.crc".

The CRC is based on the polynomial $x^4 + x + 1$ with the linear feedback shift register preset to all 1s. The 16-bit packet is shifted through from bit 15 (MSB) to bit 0 (LSB). The CRC logic is shown in Figure 27. Data are fed into the CRC logic with MSB first. Output is sent as C3-C2-C1-C0.
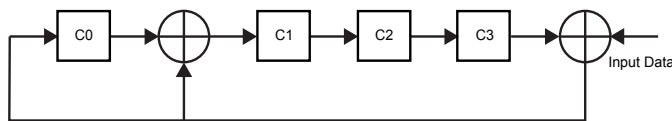

Figure 27: SPI CRC

The CRC output by the sensor on the MISO pin will always be correct. The CRC from the host on the MOSI pin must be correct if the CRC enable bit PWI.sc in the EEPROM was set.

Note: If the ERD (extended read data) register is read before the "ERCS.ERD" bit indicates a read has completed, there is a possibility of a CRC error, as the data could change during the read. Do not read the ERD register until it is known to be stable based on the done bit indication or waiting sufficient time.

The CRC can be calculated with the following C code:

```
/*
* CalculateCRC
*
* Take the 16-bit input and generate a 4-bit CRC
* Polynomial = x^4 + x + 1
* LFSR preset to all 1's
*/
uint8_t CalculateCRC(uint16_t input)
{
    bool CRC0 = true;
    bool CRC1 = true;
    bool CRC2 = true;
    bool CRC3 = true;
    int  i;
    bool DoInvert;
    uint16_t mask = 0x8000;

    for (i = 0; i < 16; ++i)
    {
        DoInvert = ((input & mask) != 0) ^ CRC3;
        CRC3 = CRC2;
        CRC2 = CRC1;
        CRC1 = CRC0 ^ DoInvert;
        CRC0 = DoInvert;
        mask >>= 1;
    }

    return (CRC3 ? 8U : 0U) + (CRC2 ? 4U : 0U) + (CRC1 ? 2U
: 0U) + (CRC0 ? 1U : 0U);
}
```

Manchester Serial Interface

The A33003 incorporates a serial interface shared with the standard output line (VOUT). (Note: The A33003 may be programmed via SPI, with additional wiring connections). This interface allows an external controller to read and write registers in the A33003 EEPROM and volatile memory without the need for the host controller to control V_{CC} or even share the same V_{CC} line. The device uses a point-to-point communication protocol, based on Manchester encoding per G.E. Thomas (a rising edge indicates a '0' and a falling edge indicates a '1'), with address and data transmitted MSB first. The addressable Manchester code implementation uses the logic states of the SA0/SA1 pins to set address values for each die. In this way, individual communication with up to four A33003 die is possible per line.

To prevent any undesired programming of the A33003, the serial interface can be disabled by setting the Disable Manchester bit (PWS.DM EEPROM address 0x1B bit 3) to a '1'. With this bit set, the A33003 will ignore any Manchester input commands.
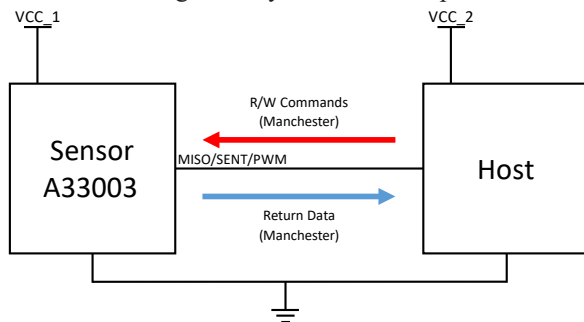

Figure 28: Manchester Interface Programming Setup

ENTERING MANCHESTER COMMUNICATION MODE

Provided the Disable Manchester bit is not set in EEPROM, there are two ways to begin Manchester communication:

1. If PWM, SENT, and SPO are disabled, and Manchester is the active communication protocol, then only the Manchester entry code on the VOUT pin is required to begin Manchester communication.

2. If PWM or SENT protocols are enabled, the Manchester Auxiliary Interrupt Pulse or F_AUX pulses must be used, followed by the Manchester entry code. Once this has been completed, Manchester communication is enabled. If no entry code is received after an Auxiliary Interrupt Pulse or F_AUX pulse for t_{msgRX}, the Manchester interface will timeout, and the device will return to its previous operating state. (Note: If MEPE bit is set to '0', then the Auxiliary Interrupt Pulse and F_AUX pulses are disabled. Because of this, Manchester communication is not possible when PWM or SENT are active.)

Once the Manchester Communication Mode is entered, the VOUT pin will cease to provide angle data, interrupting any data transmission in progress. After this, the Manchester interface will only respond to two specific codes: the Access and Exit codes. If the Access code is sent, the Manchester interface is now fully active and will respond to all commands. If the Exit code is sent, the Manchester interface will close all access and the previous protocol will resume control of the pin PWM or SENT as determined by EEPROM. Both the Access and Exit code must be written to address 0x3F (address field of all 1's).

MANCHESTER AUXILIARY INTERRUPT PULSE FOR PWM OUTPUT MODE

To initialize communication using the Manchester Auxiliary command when the A33003 is configured with PWM output, the auxiliary interrupt pulse can be applied at any time. The auxiliary pulse must have a minimum width of t_{HOLD}, after which the pulse is released for t_{GATE} plus the rise time to allow the line to pull high and the device to register a rising edge. After this, the controller must pull low for t_{GATE} before beginning to send the Manchester Access Code. The device must recognize the first rising edge of the Manchester access code before t_{msgRX} after the hold time or the device will timeout, aborting Manchester initialization and returning to PWM functionality. The Manchester Auxiliary command for PWM output is shown Figure 29.
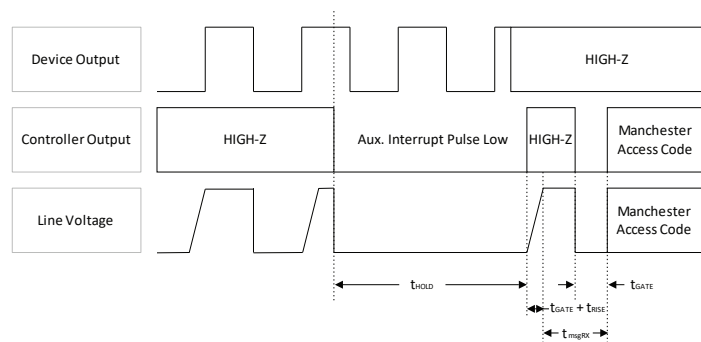

Figure 29: Auxiliary Interrupt Pulse Waveform

MANCHESTER AUXILIARY COMMAND FOR SENT AND TSENT OUTPUT MODE

To initialize communication using the Manchester Auxiliary command when the A33003 is configured with SENT or TSENT output, the auxiliary interrupt pulse can begin at any time between the start of the Sync pulse and the end of the last data nibble pulse. The pulse must have a minimum width of t_{HOLD}, after which the pulse must be released for t_{GATE} plus the rise time to allow the line to pull high, followed by a low period of t_{GATE} before sending the Manchester access code. Again, if the first rising edge of the Manchester access code is not seen before t_{msgRX}, the device will timeout, Manchester initialization is aborted, and the device will return to normal functionality. The Manchester Auxiliary command for SENT and TSENT output is shown Figure 30.
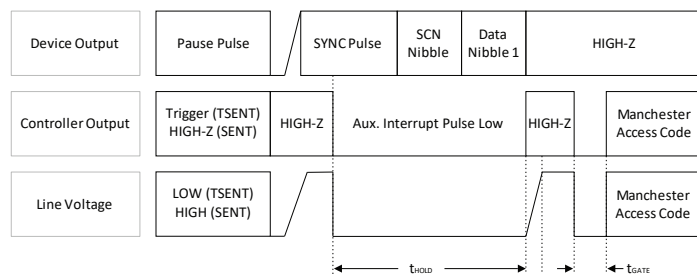

Figure 30: Interrupt waveform for SENT and TSENT output

OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Access Code Timeout	t_{msgRX}			–	–	300	µs
Interrupt Pulse Hold Time	t_{HOLD}	SSENT – Short	F_AUX	50	–	83	ticks
		SSENT – Long	F_AUX	196	–	297	ticks
		ASENT	F_AUX	50	–	80	ticks
		SENT	Aux. Interrupt Pulse	30	–	–	ticks
		TSENT	Aux. Interrupt Pulse	30	–	–	ticks
		PWM	Aux. Interrupt Pulse	2× PWM period [5]	–	–	µs
Deglitch Gate Time	t_{GATE}			1.0	–	–	µs

[5] The minimum hold time for the Auxiliary interrupt, when the output is set for PWM, is double the PWM period. If the PWM frequency increases as a result of a diagnostic condition, the hold time is double the new PWM period at the diagnosis frequency.

Manchester Message Structure

The general format of a command message frame is shown in Figure 31. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary.
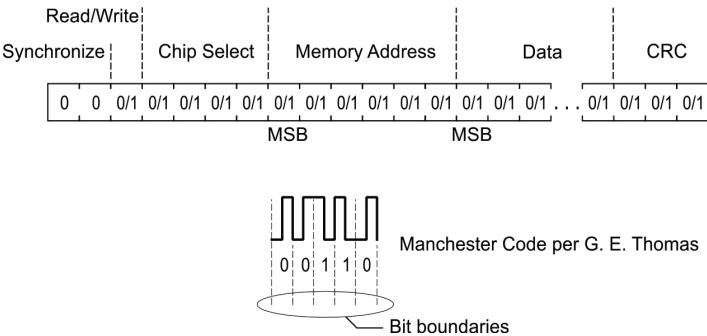

Figure 31: General Format for Serial Interface Commands

A brief description of each bit is provided in Table 7.

Table 7: Manchester Command General Format

Bits	Parameter Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
4	Chip Select	0/1	Used to select a set of target chips/die, based on ID value.
6	Address	0/1	[Read/Write] Serial address
16	Data	0/1	Requested serial register contents (Write operation only)
3	CRC	0/1	Incorrect value indicates errors

When the A33003 is operating in I²C Mode (ISEL pin set to a logic low), the Die ID value is determined by the state of the SA0 and SA1 pins.

Table 8: Pin Values

SA1	SA0	ID Value
0	0	ID0
0	1	ID1
1	0	ID2
1	1	ID3

Using the 4 bits of the Chip Select field, die can be selected via their ID value, allowing up to four die to be individually addressed and providing for different group addressing schemes. If Chip Select is all zeros or the A33003 is operating in SPI mode (ISEL pin set to a logic high), no ID comparison will be made, allowing all A1335s to be addressed at once.

Example: If Chip Select = 1010, all die with ID3 or ID1 will be selected.

Note: If the sharing a SENT line with multiple chips/dies, reading must be done one die at a time.

Table 9: Chip Select

Chip Select			
ID3	ID2	ID1	ID0

MANCHESTER AUXILIARY COMMAND FOR SSENT AND ASENT OUTPUT MODE

To initialize communication using the Manchester Auxiliary command when the A33003 is configured with SSENT or ASENT output, the auxiliary function pulse, F_AUX, is applied as the frame request pulse. The auxiliary pulse must have a minimum width of t_{HOLD}. After the pulse is released, the output line is required to go HIGH-Z for t_{GATE} plus the rise time. The controller must then pull the output line low for t_{GATE} before sending the Manchester access code. If the first rising edge of the access code is not recognized before t_{msgRX}, a timeout will occur, the Manchester initialization is aborted, and the output will return to normal functionality.
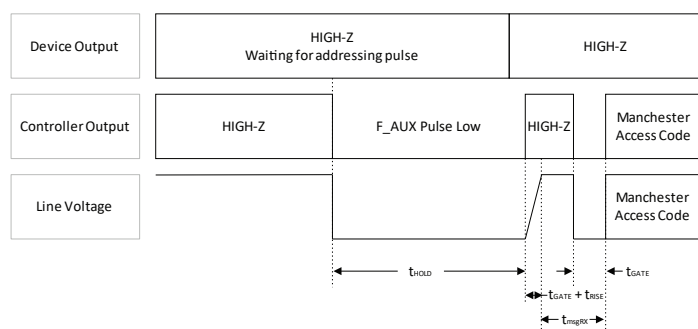
Figure 32: Interrupt waveform for SSENT and ASENT output

ACCESS CODES

Once the device is set up to recognize Manchester communication, there are two special Manchester codes used to activate or deactivate the serial interface:

1. Manchester Access Code: This code, (equivalent to performing a write to register: 0x3F with data: 0x62D2) must be sent to fully begin Manchester communication. Once this is performed, the Manchester interface will respond to all available Manchester commands.

2. Manchester Exit Code: This code, (equivalent to writing to register: 0x3F with data: 0x0000) when sent, will exit Manchester communication, and return the device to its previous state.

Once the Manchester Communication Mode is exited, the output pin will return to outputting angle data (provided no flag is asserted). This output data is taken directly from the transmission in progress. It is recommended to disregard the first angle reading when exiting Manchester communication, and wait for the start of the next PWM duty cycle or SENT packet as applicable.

TRANSACTION TYPES

The A33003 will never initiate communication, and recognizes four transactions: write access, write to EEPROM, write to volatile, and read. Only the read transaction will prompt the A33003 to respond with data. When responding to a read command, the A33003 will not check for line contention; it is the responsibility of the controller to release the line in time and be ready to read the data sent by the A33003.

After a read command is received, there is a delay time between when the last bit of the command is sent to the device and when the device begins to respond on the line. This delay is divided between two times.

- The first (t_d) is the delay between the last bit of the read command and when the devices begins to pull the line low in preparation to send data.

- The second delay (t_b) is the delay between the time when the device pulls the line low to when it begins outputting the data. While the output is fully readable as long as the controller releases control before $t_d + t_b$, it is recommended to release the line before t_d.
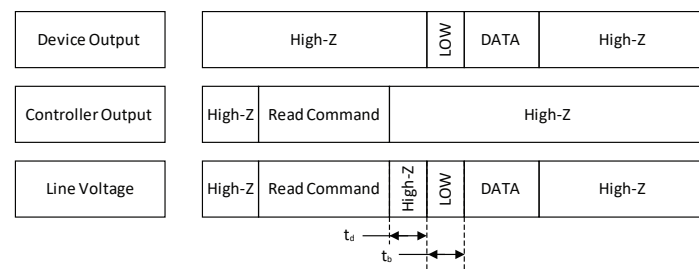

Figure 33: Transaction Types

READING DATA USING MANCHESTER ENCODING

A Read command with the desired register number is sent from the controller to the A33003. The device responds with a Read Response frame using the Manchester protocol.

In addition to the contents of the requested memory location, a Return Status field is included with every Read Response. This field provides the ID used to communicate with the part and any errors which may have occurred during the transaction. These bits are:

- **ID** – ID (SA1, SA0) unless BC = 1 (ID will be 00)
- **BC** – Broadcast; ID field was zero
- **AE** – Abort Error; edge detection failure after sync detect
- **OR**– Overrun Error; a new Manchester command has been received before the previous request could be completed
- **CS** – Checksum error; a prior command had a checksum error

Table 10: Return Status Bits

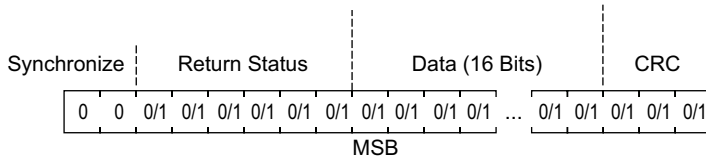| Return Status Bits (6 bits)					
5	4	3	2	1	0
ID		BC	AE	OR	CS

Figure 34: Manchester Read Response

The following command messages can be exchanged between the device and the external controller:

- Manchester Access Code
- Manchester Exit Code
- Read
- Read Response
- Write

For EEPROM address information, refer to the EEPROM Structure section. For serial address locations, refer to the serial register map.

ERROR CHECKING

The serial Manchester interface uses a cyclic redundancy check (CRC) for data bit error checking (synchronization bits are ignored during the check).

The CRC algorithm is based on the polynomial

$$g(x) = x^3 + x + 1 \ ,$$

and the calculation is represented graphically in Figure 35.

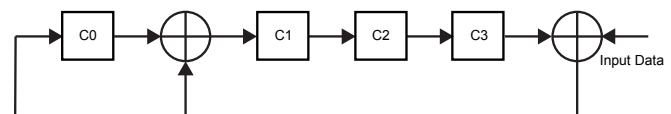The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111.

Figure 35: Manchester CRC Calculation

Table 11: Manchester Access Code

Function	Transmits the Access Code to the A33003. Enters Serial Communication mode with the desired output protocol.
Syntax	Sent by the external controller on the A33003 output pin.
Related Commands	Related command: Serial Exit Code
Pulse Sequence	

Options	Access Codes:
	  Manchester Access Code = 0x62D2
	    Selects Manchester output on the PWM pin.

Examples	The Manchester Access Code operates as a broadcast pulse, meaning the Target ID field is inconsequential. For example, if two A33003s configured with ID0 and ID2 respectively are sharing a common SENT line, a Manchester Access Code with a Target ID Value of 0x1 results in both sensors entering Manchester Serial Communication mode.

Table 12: Manchester Exit Code

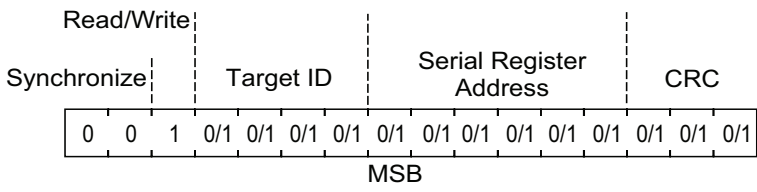| Function	Returns the A33003 to normal operation.
Syntax	Sent by the external controller on the A33003 output pin. Manchester Exit Code = Any value other than 0x62d2
Related Commands	Manchester Access Codes
Pulse Sequence	
Options	None
Examples	Similiar to the Manchester Access code, the Manchester Exit code acts as a broadcast pulse. To exit the serial communication mode, the Exit Code can be any value besides the Access Code (such as 0x0000).

Table 13: Manchester Read

Function	Determines the serial address within the A33003, from which the next Read Response will transmit data. The A33003 must first receive a Manchester Access Code before responding to a Read command.
Syntax	Sent by the external controller on the A33003 output pin.
Related Commands	Read Response
Pulse Sequence	Read Response with Manchester output.
Options	None
Examples	

Table 14: Manchester Read Response
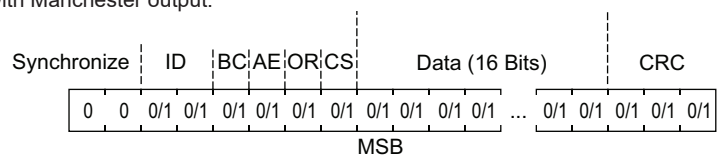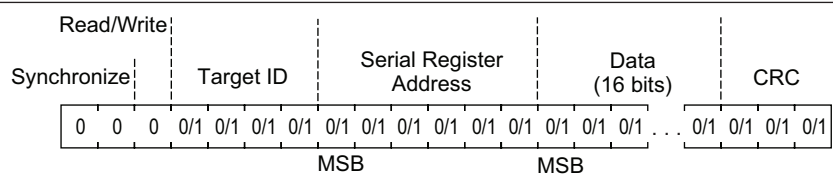
Function	Transmits to the external controller data retrieved from the A33003 serial register in response to the most recent Read command.
Syntax	Sent by the A33003 on the output pin. Sent after a Read command.
Related Commands	Read
Pulse Sequence	Read Response with Manchester output.
Options	Read from an Even address returns Even byte [15:8] and Odd byte [7:0]. Read from an Odd address returns Odd byte [7:0] only. Data bits [15:8] will be zeroes.
Examples	–

Table 15: Manchester Write

Function	Transmits to the A33003 data prepared by the external controller.
Syntax	Sent by the external controller on the A33003 output pin.
Related Commands	
Pulse Sequence	
Options	Data is written to Address and Address+1 if Even address (16-bit write). If Odd address, only 8 bits are written (LSB of 16-bit data field).
Examples	

EEPROM AND SHADOW MEMORY USAGE

The device uses EEPROM to permanently store configuration parameters for operation. EEPROM is user-programmable and permanently stores operation parameter values or customer information. The operation parameters are downloaded to shadow (volatile) memory at power-up. Shadow fields are initially loaded from corresponding fields in EEPROM, but can be overwritten, either by performing an extended write to the shadow addresses, or by reprogramming the corresponding EEPROM fields and power cycling the IC. Use of shadow memory is substantially faster than accessing EEPROM. In situations where many parameter need to be tested quickly, shadow memory is recommended for trying parameter values before permanently programming them into EEPROM. The shadow memory registers have the same format as the EEPROM and are accessed at extended addresses 0x40 higher than the equivalent EEPROM address. Unused bits in the EEPROM do not exist in the related shadow register, and will return 0 when read. Shadow registers do not contain the ECC bits. All EEPROM and shadow locations may be read without unlocking. The mapping of bits from register addresses in EEPROM to their corresponding register addresses in shadow is shown in the EEPROM table (See "EEPROM table" section).

Extended access is provided to additional memory space via the direct registers. This access includes the EEPROM, shadow registers, and registers for additional status and diagnostics. All extended registers are up to 32 bits wide.
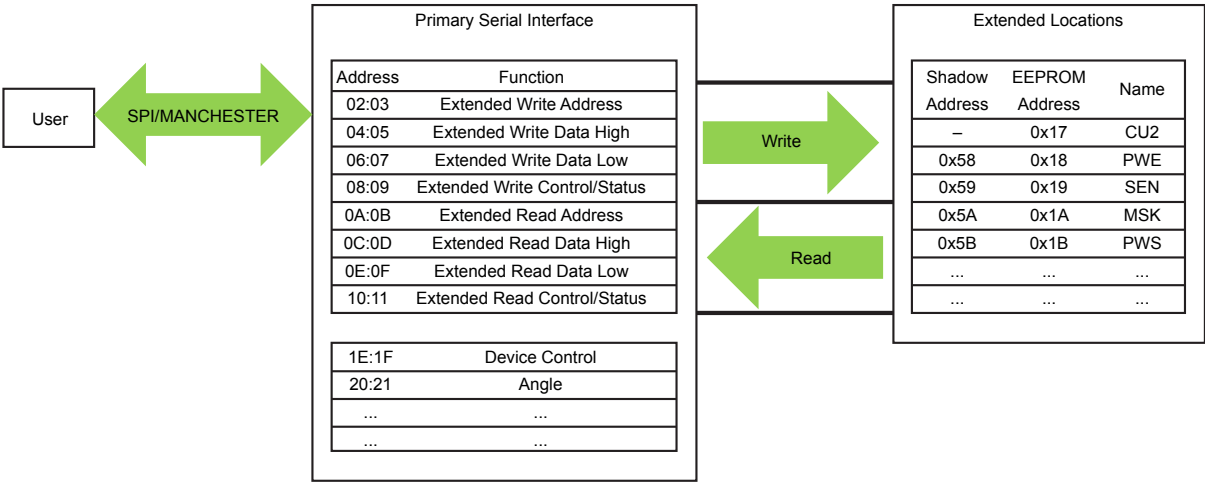
Figure 36: Serial Interface to Extended Memory (EEPROM and Shadow)

Enabling EEPROM Access

To enable EEPROM write access after power-on-reset, a unlock code needs to be written to the serial register "keycode". This involves five write commands, which should be executed after each other:

Write 0x00 to register 0x3C[15:8]

Write 0x27 to register 0x3C[15:8]

Write 0x81 to register 0x3C[15:8]

Write 0x1F to register 0x3C[15:8]

Write 0x77 to register 0x3C[15:8]

This needs to be done once after power-on reset if the customer intends to write to the EEPROM.

Writing to serial registers and reading from serial registers does not require anything special after power-on.

Reading all EEPROM cells is always possible.

Device must be unlocked when performing EEPROM margin checking.

EEPROM Write Lock

It is possible to protect the EEPROM against accidental writes.

- Setting the EEPROM field "lock" to value 0xC ('1100' binary) will block any writes to the EEPROM, so that permanent changes are not possible anymore. Temporary changes to the setting are still possible by writing to the shadow memory, but these changes are lost after a power cycle.
  This lock is permanent and cannot be reversed. Reading of the settings is still possible.

Setting the EEPROM field "lock" to value 0x3 ('0011' binary) will lock EEPROM writes AND shadow memory writes. This means none of the sensor settings can be changed anymore. This lock is permanent and cannot be reversed. Reading of the settings is still possible.

Read Transaction from EEPROM (or Shadow Memory)

Invoking an extended read access is a three-step process:

1. Load the ERA register (using SPI or Manchester direct access) with the target extended address. ERA is the 8-bit extended address that determines which extended memory address will be accessed.

2. Invoke the extended access by writing the direct ERCS register EXR bit with '1'. The ERA address is then read and the data is loaded into the ERD registers.

3. Read the ERD registers (using SPI or Manchester direct access) to get the extended data. This will take multiple packets to obtain all 32 bits.

EEPROM read accesses may take up to 2 µs to complete. The RDN bit in the ERCS register can be polled to determine if the read access is complete before reading the data. Shadow and AUX register reads complete in one system clock cycle after synchronization. Do not attempt to read the ERD registers if the read access is potentially in process, as it could change during the serial access and the data will be inconsistent. It is also possible that a SPI CRC error will be detected if the data changes during the serial read via the SPI interface.

For example, to read location 0x1F in the EEPROM:

*   Write 0x1F to lower 8 bits of ERA (0x1F to ERA+1, Address 0x0B)
*   Write 0x80 to ERCS
*   Read ERCS+1 until bit 0 (RDN) is set (or wait enough time)
*   Read ERD (upper 16 bits of read data)
*   Read ERD+2 (lower 16 bits of read data)

For example, to read location 0x1F in the EEPROM:

- Write 0x1F to lower 8 bits of "era" (0x1F to "era+1", Address 0x0B)

| 0x4B | 0x1F |

- Write 0x80 to "ercs"

| 0x4C | 0x80 |
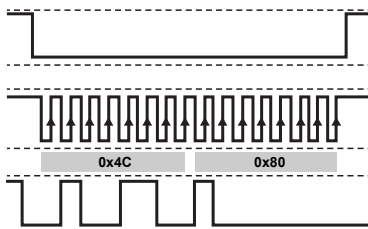
- Read "ercs"+1 until bit 0 ("rdn") is set, or wait enough time.

In the example, register 0x0C is read, so that the last bit of the second output byte contains the "rdn" bit.

| 0x0C | 0x00 | 0x00 | 0x00 |
| 0x52 | 0x7B | 0x00 | 0x01 |
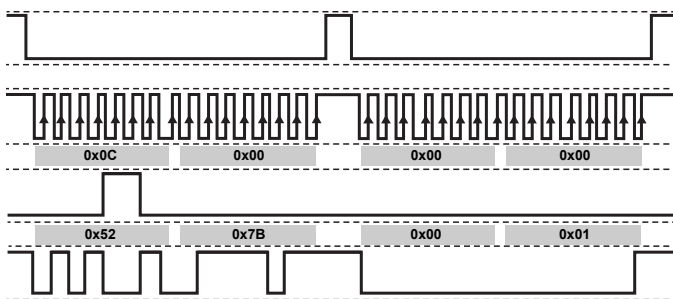
- Read "erdh" (upper 16 bits of read data)
- Read "erdl" (lower 16 bits of read data)

In the example below, the result for the data at address 0x1F is 0x58A45678. In this value,

    □ Bit [31:26] are the EEPROM CRC

    □ Bit [25:24] are unused and zero

    □ Bit [23:0] are the EEPROM values that can be used. These are the 24 bits containing the information 0xA45678 that was written in the EEPROM write example.

| 0x0E | 0x00 | 0x00 | 0x00 | 0x10 | 0x00 | 0x00 | 0x00 |
| 0x00 | 0x00 | 0x58 | 0xA4 | 0x00 | 0x00 | 0x56 | 0x78 |
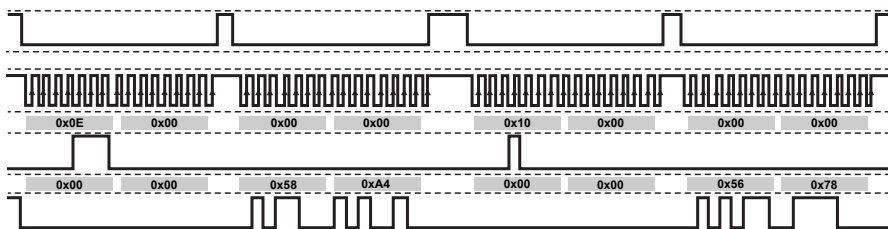
Note that it would have been possible to pipeline transactions in this example, i.e. send a new command while reading return data from the old command. This way the transaction could have been performed in 5 SPI frames instead of 8.

ALLEGRO microsystems

Write Transaction to EEPROM (or Shadow Memory)

Invoking an extended write access is a three-step process:

1. Load the EWA register (using SPI or Manchester direct access) with the target extended address.

2. Load the EWD registers (using SPI or Manchester direct access) with the data to be written to the target. This will take four SPI writes or two Manchester packets to load all 32 bits of data.

3. Invoke the extended access by writing the direct EWCS register EXW bit with '1'.

The EWA address is then written with the 32-bit EWD data.

The WDN bit in the EWCS register can be polled to determine when the write completes. This is only necessary for EEPROM writes, which can take up to 24 ms to complete. Shadow and AUX register writes complete immediately in one system clock cycle after synchronization.

For example, to write location 0x1F in the EEPROM with 0x00A45678:

- Write 0x1F to lower 8 bits of EWA register (0x1F to EWA+1 Address 0x03)

- Write 0x00A45678 to EWD (0x00 to EWD, 0xA4 to EWD+1, 0x56 to EWD+2, 0x78 to EWD+3)

- Write 0x80 to EWCS

- Read EWCS+1 until bit 0 (WDN) is set (or wait enough time)

If an access violation occurs (address not unlocked), the transaction will be terminated and the corresponding RDN or WDN bit set, and the XEE warning bit will assert. The XEE bit in the ERR register will also set if the EEPROM write aborts.

For example, to write location 0x1F in the EEPROM with 0x00A45678:

• Write 0x1F to lower 8 bits of EWA register (0x1F to EWA+1 Address 0x03)
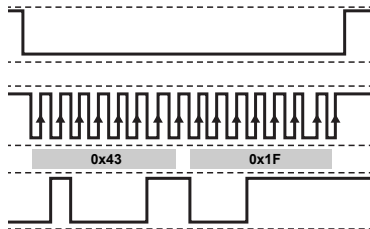
• Write 0x00A45678 to EWD (0x00 to EWD, 0xA4 to EWD+1, 0x56 to EWD+2, 0x78 to EWD+3)
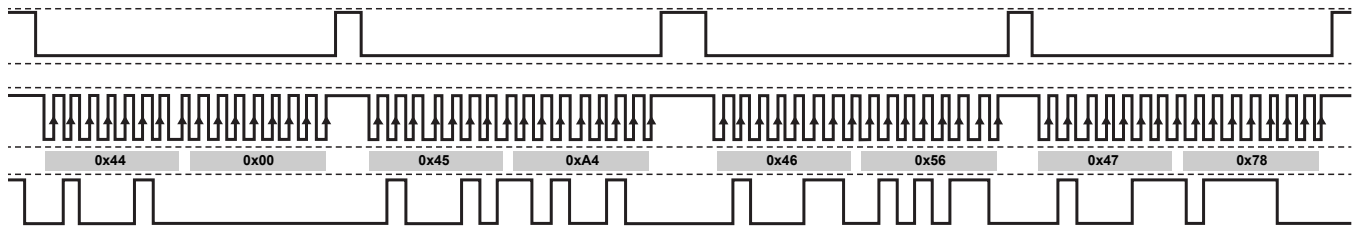


• Write 0x80 to EWCS
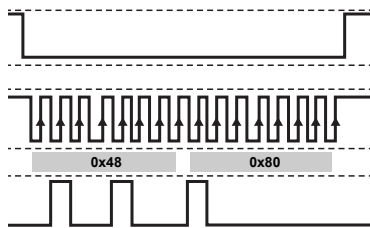
• Read EWCS+1 until bit 0 ("wdn") is set, or wait enough time.

In the example, register 0x08 is read, so that the second output byte is from register 0x09, and we wait for bit 0 to become '1', which happens in the last read.
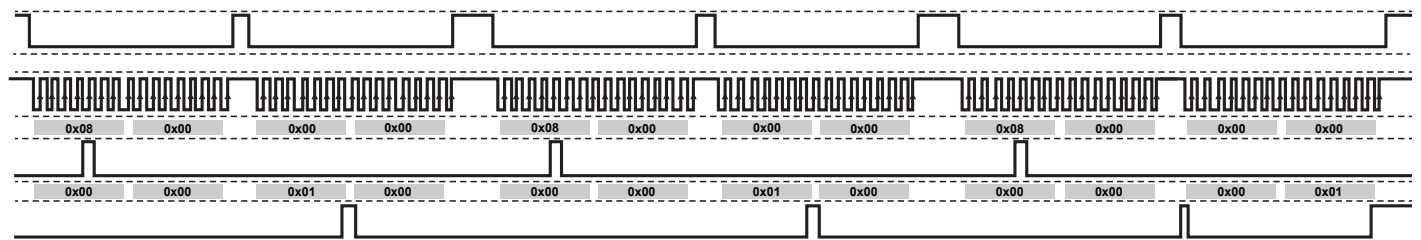
If an access violation occurs (address not unlocked), the transaction will be terminated and the corresponding "rdn" or "wdn" bit set, and the "xee" warning bit will assert. The "xee" bit in the "err" register will also set if the EEPROM write aborts.

Shadow Memory Read and Write Transactions

Shadow memory Read and Write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM extended address, one must address to the Shadow Extended addresses, which are located at an offset of 0x40 above the EEPROM. Refer to the EEPROM table for all addresses.

SERIAL INTERFACE TABLE

Table 16: Primary Serial Interface Registers Bits Map

Address* (0x00)	Register Symbol	Read/ Write	Addressed Byte (MSB)								Addressed Byte + 1 (LSB)								LSB Address
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x00	nop	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x01
0x02	ewa	RW	0	0	0	0	0	0	0	0	write_adr								0x03
0x04	ewdh	RW	write_data_hi																0x05
0x06	ewdl	RW	write_data_lo																0x07
0x08	ewcs	WO/RO	exw	0	0	0	0	0	0	wip	0	0	0	0	0	0	0	wdn	0x09
0x0A	era	RW	0	0	0	0	0	0	0	0	read_adr								0x0B
0x0C	ercs	WO/RO	exr	0	0	0	0	0	0	rip	0	0	0	0	0	0	0	rdn	0x0D
0x0E	erdh	RO	read_data_hi																0x0F
0x10	erdl	RO	read_data_lo																0x11
0x12 0x14 0x16 0x18 0x1A 0x1C	Unused	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x13 0x15 0x17 0x19 0x1B 0x1D
0x1E	ctrl	RW/WO	special				spo	cls	clw	cle	initiate_special								0x1F
0x20	ang	RO	0	ef	uv	p	angle												0x21
0x22	sta	RO	1	0	0	0	eptr	0	dieid		rot	0	sdn	bdn	lbr	cstr	bip	aok	0x23
0x24	err	RO	1	0	1	0	war	stf	avg	0	plk	zie	eue	ofe	uvd	uva	msl	rst	0x25
0x26	warn	RO	1	0	1	1	ier	crc	sen	0	xee	tr	ese	sat	tcw	bsy	msh	tov	0x27
0x28	tsen	RO	1	1	1	1	temperature												0x29
0x2A	sfield	RO	1	1	1	0	gauss												0x2B
0x2C	turns	RO	1	1	tsrc	p	turns												0x2D
0x2E	toff	RO	1	lat	0	p	0	turns_offset											0x2F
0x30	hang	RO	0	ef	uv	p	angle_hys												0x31
0x32	ang15	RO	0	angle_15															0x33
0x34	zang	RO	0	ef	uv	p	angle_zcd												0x35
0x36	td_high	RO	0	ef	tsrc	p	turns_delta[23:12]												0x37
0x38	td_low	RO	0	ef	lat	p	turns_delta[11:0]												0x39
0x3A	ptang	RO	0	ef	uv	p	pll_turns_angle												0x3B
0x3C	ikey	WO/RO	keycode								0	0	0	0	0	0	0	cul	0x3D
0x3E	Unused	RO	Unused																0x3F

*Addresses that span multiple bytes are addressed by the most significant byte.

PRIMARY SERIAL INTERFACE REGISTERS REFERENCE

Location 0x02:0x03 ("ewa")

ewa.write_adr

The field "write_adr" is a bit field located at address 0x02[7:0]. This bit field is part of the location "ewa".

8-bit address for extended writes. Writes require unlock.

    0x00-0x1F: EEPROM (takes about 24 ms)
    0x40-0x5F: Shadow

Location 0x04:0x05 ("ewdh")

ewdh.write_data_hi

The field "write_data_hi" is a bit field located at address 0x04[15:0]. This bit field is part of the location "ewdh".

Upper 16 bits of data for an extended write operation.

Location 0x06:0x07 ("ewdl")

ewdl.write_data_lo

The field "write_data_lo" is a bit field located at address 0x06[15:0]. This bit field is part of the location "ewdl".

Lower 16 bits of data for an extended write operation.

Location 0x08:0x09 ("ewcs")

ewcs.wdn

The field "wdn" is a bit located at address 0x08[0]. This bit is part of the location "ewcs".

Write done when wdn = '1'; wdn clears when exw is set to '1'.

ewcs.wip

The field "wip" is a bit located at address 0x08[8]. This bit is part of the location "ewcs".

Write in progress when '1'.

ewcs.exw

The field "exw" is a bit located at address 0x08[15]. This bit is part of the location "ewcs".

Initiate extended write by writing with '1'. Sets "wip" and clears "wdn". Write-only, always reads back 0.

Location 0x0A:0x0B ("era")

era.read_adr

The field "read_adr" is a bit field located at address 0x0A[7:0]. This bit field is part of the location "era".

8-bit address for extended reads.

    0x00-0x1F: EEPROM (takes about 2 μs)
    0x40-0x5F: Shadow

NOTE: After LBIST or a reload of EEPROM values, this value of read_adr will be changed.

Location 0x0C:0x0D ("ercs")

ercs.rdn

The field "rdn" is a bit located at address 0x0C[0]. This bit is part of the location "ercs".

Read done when '1', clears when "exr" set to '1'.

ercs.rip

The field "rip" is a bit located at address 0x0C[8]. This bit is part of the location "ercs".

Read in progress when '1'.

ercs.exr

The field "exr" is a bit located at address 0x0C[15]. This bit is part of the location "ercs".

Initiate extended read by writing with '1'. Sets "rip" and clears "rdn". Write-only, always reads back 0.

Location 0x0E:0x0F ("erdh")

erdh.read_data_hi

The field "read_data_hi" is a bit field located at address 0x0E[15:0]. This bit field is part of the location "erdh".

Upper 16 bits of data from extended read operation, valid when RDN set to '1'.

Location 0x10:0x11 ("erdl")

erdl.read_data_lo

The field "read_data_lo" is a bit field located at address 0x10[15:0]. This bit field is part of the location "erdl".

Lower 16 bits of data from extended read operation, valid when RDN set to '1'.

Location 0x1E:0x1F ("ctrl")

ctrl.initiate_special

The field "initiate_special" is a bit field located at address 0x1E[7:0]. This bit field is part of the location "ctrl".

For certain actions from "special" bit field, a code must be set to "initiate special". The following actions may be triggered by writing this field (the code must be written after the ctrl.special field is written):

0x46 initiates turns counter reset.
0x5A initiates hard reset.
0xA5 initiates EEPROM reload.
0xB9 initiates CVH self-test or functional BIST.

Read always returns 0x00.

ctrl.spo

The "spo" bit is bit 11 of the CTRL row. It is the SPI override bit.

If set to 1, then MISO is forced to be SPI output. This overrides PWM and SENT.

ctrl.cle

The field "cle" is a bit located at address 0x1E[8]. This bit is part of the location "ctrl".

Clear error register "err" when written with '1'. Clears bits that were previously read from the "err". Bits that were not yet read will not be cleared, so the user needs to read ERR first. Write-only, always returns 0.

ctrl.clw

The field "clw" is a bit located at address 0x1E[9]. This bit is part of the location "ctrl".

Clear warning (WARN) register when set to '1'. Clears bits that were previously read from the WARN, so the user needs to read WARN first. Write-only, always returns 0.

ctrl.cls

The field "cls" is a bit located at address 0x1E[10]. This bit is part of the location "ctrl".

Clear bits "sdn" and "bdn" from "status" register when set to '1'. Write-only, returns 0 when read.

ctrl.special

The field "special" is a bit field located at address 0x1E[15:12]. This bit field is part of the location "ctrl".

Special actions. Some of the actions will only be invoked after the "initiate_special" field is written with the correct value. This field will return 0x00 on completion.

0000 – No action.

0001 – Enable EEPROM low voltage margin. IC must be unlocked.

0010 – Enable EEPROM high voltage margin. IC must be unlocked.

0011 – Turns counter load from EWD. Starts after writing 0x46 to "initiate_special".

0100 – Turns counter reset. Starts after writing 0x46 to "initiate_special".

0101 – Reload EEPROM. Requires unlock of part. Starts after writing 0xA5 to "initiate_special".

0111 – Hard reset. Requires unlock of part. Starts after writing 0x5A to "initiate_special".

1001 – Run CVH self-test. Starts after writing 0xB9 to "initiate_special".

1010 – Run logic BIST (on PLL logic). Starts after writing 0xB9 to "initiate_special".

1011– Run both the CVH self-test and Logic BIST In parallel. Starts after writing 0xB9 to the ctrl.initiate_special field.

1101 – Re-sample PWM errors (errors must have cleared for this to have an effect).

1110 – Clear fatal PWM errors (EUE, WDE, STE).

1111 – Clear fatal and resample all PWM errors.

Location 0x20:0x21 ("ang")

ang.angle

The field "angle" is a bit field located at address 0x20[11:0]. This bit field is part of the location "ang".

Angle from PLL after processing. Angle in degrees = unsigned 12-bit value × (360 / 4096).

ang.p

The field "p" is a bit located at address 0x20[12]. This bit is part of the location "ang".

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of 1's in the 16-bit word.

ang.uv

The field "uv" is a bit located at address 0x20[13]. This bit is part of the location "ang".

Undervoltage flag (real time). OR of analog and digital UV flags. Conditions are realtime, but are masked by the Shadow mask bits.

ang.ef

The field "ef" is a bit located at address 0x20[14]. This bit is part of the location "ang".

Error flag. Will be '1' if any unmasked bit in ERR or WARN is set.

Location 0x22:0x23 ("sta")

sta.aok

The field "aok" is a bit located at address 0x22[0]. This bit is part of the location "sta".

Angle output OK. PLL is in lock.

sta.bip

The field "bip" is a bit located at address 0x22[1]. This bit is part of the location "sta".

Boot in progress.

sta.cstr

The field "cstr" is a bit located at address 0x22[2]. This bit is part of the location "sta".

CVH self-test running.

sta.lbr

The field "lbr" is a bit located at address 0x22[3]. This bit is part of the location "sta".

LBIST running.

sta.bdn

The field "bdn" is a bit located at address 0x22[4]. This bit is part of the location "sta".

Boot complete. EEPROM loaded and any startup self-tests are complete.

sta.sdn

The field "sdn" is a bit located at address 0x22[5]. This bit is part of the location "sta".

Special access (from ctrl register) done. Clears to '0' when SPECIAL triggered, set '1' when complete.

sta.rot

The field "rot" is a bit located at address 0x22[7]. This bit is part of the location "sta".

Rotation direction based on hysteresis ('0' = increasing angles, '1' = decreasing angles).

sta.dieid

The field "dieid" is a bit field located at address 0x22[9:8]. This bit field is part of the location "sta".

DIE ID from EEPROM. Programmed by Allegro at factory.

Location 0x24:0x25 ("err")

This is the error register. All errors are latched, meaning they will remain high after they have occurred just once. Errors need to be read and then cleared to remove them. It is important that the user clears errors, so that subsequent errors become visible. This is especially important for the "rst" error flag (reset), which is always enabled after power on. Not removing it means that an unexpected reset cannot be discovered afterwards.

err.rst

The field "rst" is a bit located at address 0x24[0]. This bit is part of the location "err".

Reset condition. Sets on power-on reset or on hard reset. Does not set on LBIST.

err.msl

The field "msl" is a bit located at address 0x24[1]. This bit is part of the location "err".

Magnetic sense low fault. Magnetic sense was below the MagSenseLow limit.

err.uva

The field "uva" is a bit located at address 0x24[2]. This bit is part of the location "err".

Undervoltage detector tripped. Will be set again after clearing if the undervoltage situation persists. Based on analog regulator.

err.uvd

The field "uvd" is a bit located at address 0x24[3]. This bit is part of the location "err".

Undervoltage detector tripped. Will be set again after clearing if the undervoltage situation persists. Based on digital regulator.

err.wde

The field "wde" is a bit located at address 0x24[4]. This bit is part of the location "err".

Oscillator watchdog tripped.

err.eue

The field "eue" is a bit located at address 0x24[5]. This bit is part of the location "err".

EEPROM uncorrectable error. A multi-bit EEPROM read occurred.

err.zie

The field "zie" is a bit located at address 0x24[6]. This bit is part of the location "err".

Zero-crossing integrity error. A zero crossing did not occur within the maximum time expected, likely indicating missing magnet or extreme rotation speed.

err.plk

The field "plk" is a bit located at address 0x24[7]. This bit is part of the location "err".

PLL lost lock.

err.avg

The field "avg" is a bit located at address 0x24[9]. This bit is part of the location "err".

Angle averaging error. The ORATE is too high for the velocity and the averaging is corrupted.

err.stf

The field "stf" is a bit located at address 0x24[10]. This bit is part of the location "err".

Self-test failure.

err.war

The field "war" is a bit located at address 0x24[11]. This bit is part of the location "err".

Warning. Some unmasked error bits are set in the WARN register. If WAR in mask register "MSK" is set, this will be forced to 0.

Location 0x26:0x27 ("warn")

warn.tov

The field "tov" is a bit located at address 0x26[0]. This bit is part of the location "warn".

Turns Counter Overflow Error. The turns counter surpassed its maximum value of ±256 full rotation. This is not dependent on the resolution of "turns" (45 or 180 degrees).

warn.msh

The field "msh" is a bit located at address 0x26[1]. This bit is part of the location "warn".

Magnetic sense high fault. Magnetic sense has exceeded the MagSenseHigh limit.

warn.bsy

The field "bsy" is a bit located at address 0x26[2]. This bit is part of the location "warn".

Extended access overflow. An EXW or EXR was initiated while previous extended read or write was in progress.

warn.tcw

The field "tcw" is a bit located at address 0x26[3]. This bit is part of the location "warn".

Turns counter warning (over ±135 degrees delta).

warn.sat

The field "sat" is a bit located at address 0x26[4]. This bit is part of the location "warn".

Aggregate saturation flag. Shows that any internal signals have saturated, likely to have been cause by extremely strong or weak fields.

warn.ese

The field "ese" is a bit located at address 0x26[5]. This bit is part of the location "warn".

EEPROM soft error. A correctable (single-bit) EEPROM read occurred.

warn.tr

The field "tr" is a bit located at address 0x26[6]. This bit is part of the location "warn".

Temperature out of range. The temperature sensor calculated a temperature below –60°C or above 180°C. Temperature will saturate at those limits.

warn.xee

The field "xee" is a bit located at address 0x26[7]. This bit is part of the location "warn".

Extended execute error. A command intiated by an extended write failed. Write failed due to access error (not unlocked) or EEPROM write failure.

warn.sen

The field "sen" is a bit located at address 0x26[9]. This bit is part of the location "warn".

SENT contention error.

warn.crc

The field "crc" is a bit located at address 0x26[10]. This bit is part of the location "warn".

Incoming SPI CRC error. Packet was discarded.

warn.ier

The field "ier" is a bit located at address 0x26[11]. This bit is part of the location "warn".

Interface error. Invalid number of bits in SPI packet, or bit 15 of MOSI data = '1'. Packet was discarded.

Also Manchester error or SENT contention.

Location 0x28:0x29 ("tsen")

tsen.temperature

The field "temperature" is a bit field located at address 0x28[11:0]. This bit field is part of the location "tsen".

Current junction temperature from internal temperature sensor relative to room temperature (signed value). Value is in 1/8 of a degree. Temperature °C ≈ (tsen.temperature / 8) + 25.0.

Location 0x2A:0x2B ("field")

field.gauss

The field "gauss" is a bit field located at address 0x2A[11:0]. This bit field is part of the location "field".

Field strength in gauss. Field level is used for gross correction, and should not be used for accurate field readings. Value is typically ~10% low.

Location 0x2C:0x2D ("trns")

trns.turns

The field "turns" is a bit field located at address 0x2C[11:0]. This bit field is part of the location "trns".

Turns counter. Signed 45 or 180 degree increments.

Reading this field automatically latches the toff.turns_offset value and set toff.lat. Allowing all 21 bits of the turns delta field to be read with the same timestamp.

trns.p

The field "p" is a bit located at address 0x2C[12]. This bit is part of the location "trns".

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of 1's in the 16-bit word.

trns.tsre

The field "tsre" is a bit located at address 0x2C[13]. This bit is part of the location "trns".

Turns Source. Set to '1' to use the more accurate PLL as turns counter source (recommended). Set to '0' to use ZCD angle as turns counter (not recommended).

Location 0x2E:0x2F ("toff")

toff.turns_offset

The field "turns_offset" is a bit field located at address 0x2E[10:0]. This bit field is part of the location "toff".

This is either the 11 or 9 LSBs of the turns_delta register, depending on a 180 or 45 degree turns configuration. This field is latched whenever the turns address is read.

toff.p

The field "p" is a bit located at address 0x2E[12]. This bit is part of the location "toff".

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of 1's in the 16-bit word.

toff.lat

The field "lat" is a bit located at address 0x2E[14]. This bit is part of the location "toff".

Indicates that the "turns_offset" field is latched. If '1', indicates that the word "toff" was latched on a prior read of the "turns" register, and is consistent with that reading. Will return to '0' after reading.

Location 0x30:0x31 ("hang")

hang.angle_hys

The field "angle_hys" is a bit field located at address 0x30[11:0]. This bit field is part of the location "hang".

Angle from PLL after processing and application of hysteresis. Angle in degrees = unsigned 12-bit value × (360 / 4096).

hang.p

The field "p" is a bit located at address 0x30[12]. This bit is part of the location "hang".

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of 1's in the 16-bit word.

hang.uv

The field "uv" is a bit located at address 0x30[13]. This bit is part of the location "hang".

Undervoltage flag (real time). OR of analog and digital UV flags. Conditions are realtime, but are masked by the Shadow mask bits.

hang.ef

The field "ef" is a bit located at address 0x30[14]. This bit is part of the location "hang".

Error flag. Will be '1' if any unmasked bit in ERR or WARN is set.

Location 0x32:0x33 ("ang15")

ang15.angle_15

The field "angle_15" is a bit field located at address 0x32[14:0]. This bit field is part of the location "ang15".

15-bit compensated angle (not rounded).

Location 0x34:0x35 ("zang")

zang.angle_zcd

The field "angle_zcd" is a bit field located at address 0x34[11:0]. This bit field is part of the location "zang".

Angle from ZCD. Angle in degrees = unsigned 12-bit value × (360 / 4096).

zang.p

The field "p" is a bit located at address 0x34[12]. This bit is part of the location "zang".

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of 1's in the 16-bit word.

zang.uv

The field "uv" is a bit located at address 0x34[13]. This bit is part of the location "zang".

Undervoltage flag (real time). OR of analog and digital UV flags. Conditions are realtime, but are masked by the Shadow mask bits.

zang.ef

The field "ef" is a bit located at address 0x34[14]. This bit is part of the location "zang".

Error flag. Will be '1' if any unmasked bit in ERR or WARN is set.

Location 0x36:0x37 ("td_high")

td_high.turns_delta_high

The field "turns_delta_high" is a bit field located at address 0x36[11:0]. This bit field is part of the location "td_high".

Upper 9 bits (sign extended to 12) of the turns delta counter.

When read, the contents of "td_low" (address 0x38:0x39) are latched and td_low.lat bit is set. This allows all 25 bits (sign extended) of the turns_delta value to be read at the same time-stamp.

td_high.p

The field "p" is a bit located at address 0x36[12]. This bit is part of the location "td_high".

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of 1's in the 16-bit word.

td_high.tsrc

The field "tsrc" is a bit located at address 0x36[14]. This bit is a part of the location "td_high".

Turns Source. When '1', indicates the PLL is the turns counter source. When '0', the ZCD signal path (uncompensated) is the source.

td_high.ef

The field "ef" is a bit located at address 0x36[14]. This bit is part of the location "td_high".

Error flag. Will be '1' if any unmasked bit in ERR or WARN is set.

Location 0x38:0x39 ("td_low")

td_low.turns_delta_low

The field "turns_delta_low" is a bit field located at address 0x38[11:0]. This bit field is part of the location "td_low".

Lower 12 bits of the turns delta. This is the angle offset at 12-bit resolution.

This value is latched when reading the td_high register, allowing the entirety of the turns_delta to be read with the same time-stamp.

td_low.p

The field "p" is a bit located at address 0x38[12]. This bit is part of the location "td_low".

Odd parity computed across all bits in this register. Value is chosen in such a way that there should always be an odd number of 1's in the 16-bit word.

td_low.lat

The filed "lat" is a bit located at address 0x38[13]. This bit is part of the location "td_low".

Inidicates that the "td_low" field is latched. If '1', indicates that "td_low" was latched on a prior read of the "td_high" register, and is consistent with that reading. Will return to '0' after reading.

td_low.ef

The field "ef" is a bit located at address 0x38[14]. This bit is part of the location "td_low".

Error flag. Will be '1' if any unmasked bit in ERR or WARN is set.

Location 0x3A:0x3B ("ptang")

ptang.pll_turns_angle

The field "pll_turns_angle" is a bit field located at address 0x3A[11:0]. This bit field is part of the location "ptang".

Angle from PLL after processing, as used for the turns counter.

May have hysteresis based on "h2a" configuration in EEPROM.

Angle in degrees = unsigned 12-bit value × (360 / 4096).

ptang.p

The field "p" is a bit located at address 0x3A[12]. This bit is part of the location "ptang".

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of 1's in the 16-bit word.

ptang.uv

The field "uv" is a bit located at address 0x3A[13]. This bit is part of the location "ptang".

Undervoltage flag (real time). OR of analog and digital UV flags. Conditions are realtime, but are masked by the Shadow mask bits.

ptang.ef

The field "ef" is a bit located at address 0x3A[14]. This bit is part of the location "ptang".

Error flag. Will be '1' if any unmasked bit in ERR or WARN is set.

Location 0x3C:0x3D ("key")

key.cul

The field "cul" is a bit located at address 0x3C[0]. This bit is part of the location "key".

Customer unlocked if '1'.

key.keycode

The field "keycode" is a bit field located at address 0x3C[15:8]. This bit field is part of the location "key".

Customer access keycode is entered here; value is 0x27_81_1F_77.

Always reads back 0.

ALLEGRO
microsystems

EEPROM TABLE

The EEPROM register bitmap is shown below.

All EEPROM content can be read by the user. The EEPROM ECC field in bits [31:26] of each word are not shown here.

Table 17: EEPROM / Shadow Memory Map

Shadow Memory Address	EEPROM Address	Register Name	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																												Bits
0x57	0x17	CU2	-x-	-x-	customer 2																							
0x58	0x18	PWE	-x-	-x-	zcd_turns_offset									tov	tr	msh	sat	ese	msl	uv	avg	zie	plk	stf	eue	wde
0x59	0x19	SEN	maxid		ss	sent_tick					sm	sent_mode			data_mode			cis	scn_mode			ns	zs	da	fa
0x5A	0x1A	MSK	-x-	-x-	ierm	crcm	senm	-x-	xeem	trm	esem	satm	tcwm	bsym	mshm	tovm	warm	stfm	avgm	-x-	plkm	ziem	euem	wdem	uvccm	uvam	mslm	rstm
0x5B	0x1B	MPWS	fp_adj		pen	pwm_band			pwm_freq			mepe	phe	peo	pes	eli	ls	zal	is	po	spdrv			dm	h2t	s17	sc
0x5C	0x1C	ANG	-x-	-x-	orate			rd	ro	hysteresis					zero_offset												
0x5D	0x1D	PLPC	-x-	-x-	t45	tcp	-x-	-x-	turns_init		-x-				-x-		-x-										
0x5E	0x1E	COM	-x-	-x-	lock			lbe	cse	dur	del	-x-	cud	dst	dhr	mag_thres_hi					mag_thres_lo						
0x5F	0x1F	CUS	-x-	-x-	customer																							
0x60	0x20	LIN	-x-	-x-	Linearization Error Segment 1											Linearization Error Segment 0											
0x61	0x21	LIN	-x-	-x-	Linearization Error Segment 3											Linearization Error Segment 2											
…	…	…	-x-	-x-	…												---											
0x6E	0x2E	LIN	-x-	-x-	Linearization Error Segment 29											Linearization Error Segment 28											
0x6F	0x2F	LIN	-x-	-x-	Linearization Error Segment 31											Linearization Error Segment 30											

EEPROM REFERENCE

Location 0x17 ("CU2")

Customer-usable field, intended for storing data or turns counter.

This word can be written even if EEPROM is locked. Write may be allowed without the unlock code based on COM.dur and COM.del settings (see word 0x1E).

CU2.customer 2

The field "customer 2" is a bit field located at address 0x17[23:0]. This bit field is part of the location "CU2".

Location 0x18 ("PWE")

PWE.wde

The field "wde" is a bit located at address 0x18[0]. This bit is part of the location "PWE".

PWM watchdog error enable. Duty cycle output 5% at half the selected PWM frequency.

PWE.eue

The field "eue" is a bit located at address 0x18[1]. This bit is part of the location "PWE".

PWM EEPROM uncorrectable error enable. Duty cycle 10.625% at half the selected PWM frequency.

PWE.stf

The field "stf" is a bit located at address 0x18[2]. This bit is part of the location "PWE".

PWM self-test failure error enable. Duty cycle 16.25% at half the selected PWM frequency.

PWE.plk

The field "plk" is a bit located at address 0x18[3]. This bit is part of the location "PWE".

PWM PLL Lost Lock error enable. Duty cycle 21.875% at half the selected PWM frequency.

PWE.zie

The field "zie" is a bit located at address 0x18[4]. This bit is part of the location "PWE".

PWM zero-crossing integrity error enable. Duty cycle 27.5% at half the selected PWM frequency.

PWE.avg

The field "avg" is a bit located at address 0x18[5]. This bit is part of the location "PWE".

PWM angle averaging error enable. Duty cycle is 33.125% at half the selected PWM frequency.

PWE.uv

The field "uv" is a bit located at address 0x18[6]. This bit is part of the location "PWE".

PWM undervoltage Fault enable (analog or digital). Duty cycle 38.75% at half the selected PWM frequency.

PWE.msl

The field "msl" is a bit located at address 0x18[7]. This bit is part of the location "PWE".

PWM magnetic Sense Low Fault enable. Duty cycle 44.375% at half the selected PWM frequency.

PWE.ese

The field "ese" is a bit located at address 0x18[8]. This bit is part of the location "PWE".

PWM EEPROM Soft Error enable. Duty cycle 50% at half the selected PWM frequency.

PWE.sat

The field "sat" is a bit located at address 0x18[9]. This bit is part of the location "PWE".

PWM saturation warning enable. Duty cycle 55.625% at half the selected PWM frequency.

PWE.msh

The field "msh" is a bit located at address 0x18[10]. This bit is part of the location "PWE".

PWM magnetic sense high fault enable. Duty cycle 61.25% at half the selected PWM frequency.

PWE.tr

The field "tr" is a bit located at address 0x18[11]. This bit is part of the location "PWE".

PWM temperature sensor out of range error enable. Duty cycle 66.875% at half the selected PWM frequency.

PWE.tov

The field "tov" is a bit located at address 0x18[12]. This bit is part of the location "PWE".

PWM turns counter overflow error enable. Duty cycle 72.5% at half the selected PWM frequency.

PWE.zcd_turns_offset

The field "zcd_turns_offset" is a bit field located at address 0x18[23:13]. This bit field is part of the location "PWE".

Offset to ZCD angle for purposes of aligning for turns counting. This is 11-bit angle resolution, and is added to the ZCD angle for turns purposes. If turns is configured to use the PLL (TCP = 1), it is important to use this to align the ZCD close to the PLL angle.

Location 0x19 ("SEN")

See SENT description in Appendix A for further details.

SEN.FA

The field "FA" is a bit located at address 0x19 [0]. This bit field is part of the location "SEN".

F_SAMPLE is an addressing pulse. If '0', it is a broadcast pulse.

SEN.XA

The field "XA" is a bit field located at address 0x19 [1]. This bit field is part of the location "SEN".

Addressing pulse. If '0', it is a broadcast pulse.

SEN.ZS

The field "ZS" is a bit located at address 0x19 [2]. This bit field is part of the location "SEN".

Sample-and-hold will be done in slot 0.

SEN.NS

The field "NS" is a bit located at address 0x19 [3]. This bit field is part of the location "SEN".

No sample. If '1', the F_SAMPLE pulse will not do a sample-and-hold.

SEN.SCN_MODE

The field "SCN_MODE" is a bit field located at address 0x19 [6:4]. This bit field is part of the location "SEN".

SCN nibble content mode:

0 - {0, 0, soft_flag, hard_flag}

1 - {serial msg sync, serial msg data, soft_flag, hard_flag}

2 - {ID[1], ID[0], soft_flag, hard_flag}

3 - {0, 0, 0, soft_flag | hard_flag}

4 - {0, 0, ID[1], ID[0]}

5 - {serial msg sync, serial msg data, ID[1], ID[0]}

6 - {soft_flag, hard_flag, ID[1], ID[0]}

7 - {serial msg sync, serial msg data, 0, soft_flag | hard_flag}

SEN.CIS

The field "CIS" is a bit located at address 0x19 [7]. This bit field is part of the location "SEN".

CRC includes SCN nibble if '1'.

SEN.DATA_MODE

The field "DATA_MODE" is a bit field located at address 0x19 [11:8]. This bit field is part of the location "SEN".

SENT data nibble content mode:

0 - Angle only (3 nibbles)

1 - Angle (3) + rotating status (2)

2 - Angle (3) + rotating data (3)

3 - Unused

4 - Angle (3) + rotating status (2) + Alive (1)

5 - Angle (3) + Alive(2) + ~First Nibble (1) (Secure sensor format)

6 - Angle16 (4)

7 - Angle16 (4) + Rotating status (1) + Alive (1)

8 - Angle only (3 nibbles) + ID (1)

9 - Angle (3) + rotating status (2) + ID (1)

10 - Angle (3) + rotating data (2) + ID (1)

11 - Unused

12 - Angle (3) + rotating status (1) + Alive (1) + ID (1)

13 - Angle (3) + Alive(1) + ~First Nibble (1) + ID (1)

14 - Angle16 (4) + ID (1)

15 - Angle16 (4) + Alive (1) + ID (1)

SEN.SENT_MODE

The field "SENT_MODE" is a bit field located at address 0x19 [14:12]. This bit field is part of the location "SEN".

0 - Disabled

1 - Streaming (no pause pulses)

2 - Streaming but aligned to angle update (pause pulses)

3 - TSENT, data sampled just before data nibbles

4 - TSENT, data sampled at falling edge of trigger (after minimum width)

5 - ASENT

6 - SSENT

7 - Long SSENT

NOTE: If PEN = 1, then PWM has precedence and SENT will be disabled.

NOTE: If both PWM and SENT are disabled, Manchester is active (unless disabled or CTRL.SPO is 1).

SEN.SM

The field "SM" is a bit located at address 0x19 [15]. This bit field is part of the location "SEN".

Slot Marking. SSENT only. If '1', SSENT will output a bus high delay after an addressing pulse based on slot ID.

SEN.SENT_TICK

The field "SENT_TICK" is a bit field located at address 0x19 [22:16]. This bit field is part of the location "SEN".

SENT tick time, N × period of 16 MHz clock (forced to minimum of 2 clocks internally).

SEN.SS

The field "SS" is a bit located at address 0x19 [23]. This bit field is part of the location "SEN".

Slot sync. SSENT only. If '1', then SSENT will synchronize to the bus after a reset based on other sensor's slot marking. Only valid if SM = 1.

SEN.MAXID

The field "MAXID" is a bit field located at address 0x19 [25:24]. This bit field is part of the location "SEN".

Max sensor ID on bus, for SSENT. Defines highest sensor ID on bus, after which the slot counting wraps back to 0.

Location 0x1A ("MSK")

MSK.rstm

The field "rstm" is a bit located at address 0x1A[0]. This bit is part of the location "MSK".

Reset mask. Set to '1' to hide the error bit.

MSK.mslm

The field "mslm" is a bit located at address 0x1A[1]. This bit is part of the location "MSK".

Magnetic Sense Low Fault Mask. Set to '1' to hide the error bit.

MSK.uvam

The field "uvam" is a bit located at address 0x1A[2]. This bit is part of the location "MSK".

Analog undervoltage Fault Mask. Set to '1' to hide the error bit.

MSK.uvdm

The field "uvdm" is a bit located at address 0x1A[3]. This bit is part of the location "MSK".

Digital undervoltage Fault Mask. Set to '1' to hide the error bit.

MSK.wdem

The field "wdem" is a bit located at address 0x1A[4]. This bit is part of the location "MSK".

Watchdog Error Mask. Set to '1' to hide the error bit.

MSK.euem

The field "euem" is a bit located at address 0x1A[5]. This bit is part of the location "MSK".

EEPROM Uncorrectable Error Mask. Set to '1' to hide the error bit.

MSK.ziem

The field "ziem" is a bit located at address 0x1A[6]. This bit is part of the location "MSK".

Zero-crossing integrity error mask. Set to '1' to hide the error bit.

MSK.plkm

The field "plkm" is a bit located at address 0x1A[7]. This bit is part of the location "MSK".

PLL Lost Lock error mask. Set to '1' to hide the error bit.

MSK.avgm

The field "avgm" is a bit located at address 0x1A[9]. This bit is part of the location "MSK".

Angle averaging fault mask. Set to '1' to hide the error bit.

MSK.stfm

The field "stfm" is a bit located at address 0x1A[10]. This bit is part of the location "MSK".

Self-test failure error mask. Set to '1' to hide the error bit.

MSK.warm

The field "warm" is a bit located at address 0x1A[11]. This bit is part of the location "MSK".

If set to 1, will not set WAR bit in the ERR register when unmasked warnings are present.

MSK.tovm

The field "tovm" is a bit located at address 0x1A[12]. This is part of the location "MSK".

Turns Counter Overflow Error Mask. Set to '1' to hid the error bit.

MSK.mshm

The field "mshm" is a bit located at address 0x1A[13]. This bit is part of the location "MSK".

Magnetic Sense High Fault Mask. Set to '1' to hide the error bit.

MSK.bsym

The field "bsym" is a bit located at address 0x1A[14]. This bit is part of the location "MSK".

Indirect access busy error mask. Set to '1' to hide the error bit.

MSK.tcwm

The field "tewm" is a bit located at address 0x1A[15]. This bit is part of the location "MSK".

Turns counter warning mask. Set to '1' to hide the error bit.

MSK.satm

The field "satm" is a bit located at address 0x1A[16]. This bit is part of the location "MSK".

Aggregate saturation flag mask. Set to '1' to hide the error bit.

MSK.esem

The field "esem" is a bit located at address 0x1A[17]. This bit is part of the location "MSK".

EEPROM Soft Error Mask. Set to '1' to hide the error bit.

MSK.trm

The field "trm" is a bit located at address 0x1A[18]. This bit is part of the location "MSK".

Temperature sensor out of range error mask. Set to '1' to hide the error bit.

MSK.xeem

The field "xeem" is a bit located at address 0x1A[19]. This bit is part of the location "MSK".

Execute Error Mask. Set to '1' to hide the error bit.

MSK.crcm

The field "crcm" is a bit located at address 0x1A[22]. This bit is part of the location "MSK".

CRC Error Mask (SPI). Set to '1' to hide the error bit.

MSK.ierm

The field "ierm" is a bit located at address 0x1A[23]. This bit is part of the location "MSK".

Interface Error Mask. Set to '1' to hide the error bit.

Location 0x1B ("PWS")

PWS.sc

The field "sc" is a bit located at address 0x1B[0]. This bit is part of the location "PWS".

SPI CRC (incoming) validated if SC = 1, ignored if SC = 0.

PWS.s17

The field "s17" is a bit located at address 0x1B[1]. This bit is part of the location "PWS".

SPI ignore 17th clock to allow negative edge host sampling.

PWS.ht2

The field "ht2" is a bit located at address 0x1B[2]. This bit is part of the location "PWS". Turns uses hysteresis if '1'.

   0 – Use non-hysteresis angle for turns counter

   1 – Use hysteresis angle for turns counter

This affects special register PTANG (0x3A).

PWS.dm

The field "dm" is a bit located at address 0x1B[3]. This bit is part of the location "PWS".

Disable Manchester interface.

If '1', any Manchester input.

PWS.SPDRV

SENT and PWM pin drive strength.

PWS.zal

The field "zal" is a bit located at address 0x1B[9]. This bit is part of the location "PWS".

Zero offset after linearization:

 0 = Before linearization and rotation
 1 = After linearization

PWS.PO

POR offline. SSENT only. If '1', SSENT will be offline at POR. If '0', SSENT will go online with slot counter 0.

PWS.ls

The field "ls" is a bit located at address 0x1B[10]. This bit is part of the location "PWS".

Linearization scale:

 0 = ±22.5 degrees
 1 = ±45 degrees

PWS.IS

Idle sync (SSENT only). If '1', an idle SENT bus > 511 ticks will reset the slot counter to 0.

PWS.eli

The field "eli" is a bit located at address 0x1B[11]. This bit is part of the location "PWS".

Enable linearization:

 0 = Disabled
 1 = Enabled

PWS.pes

The field "pes" is a bit located at address 0x1B[12]. This bit is part of the location "PWS".

PWM error select (if "peo" = 1).

 0 - PWM tristated, must reset (or set "peo" back to 0 in shadow) to release the PWM output.

 1 - PWM carrier frequency halved and highest priority error output on PWM as selected duty cycle.

PWS.peo

The field "peo" is a bit located at address 0x1B[13]. This bit is part of the location "PWS".

PWM error output enable. If '1', "pes" selects the response to an enabled error.

PWS.phe

The field "phe" is a bit located at address 0x1B[14]. This bit is part of the location "PWS".

PWM hysteresis enable. If 1, use hysteresis on angle going to PWM.

PWS.mepe

The field "mepe" is a bit located at address 0x1B[15]. This bit is part of the location "PWS".

If '1' Manchester, Auxiliary Interrupt Pulse and F_AUX pulses are enabled, else Auxiliary Interrupt Pulse and F_AUX pulses are ignored, and Manchester communication is only accessible when PWM and SENT are deactivated.

PWS.pwm_freq

The field "pwm_freq" is a bit field located at address 0x1B[19:16]. This bit field is part of the location "PWS".

PWM frequency select. Together with the PWS.PWM_BAND field, defines the PWM carrier frequency. See the PWM output section for more details.

PWS.pwm_band

The field "pwm_band" is a bit field located at address 0x1B[22:20]. This bit field is part of the location "PWS".

PWM frequency band. Together with the PWS.PWM_FREQ field, defines the PWM carrier frequency. See the PWM output section for more details.

PWS.pen

The field "pen" is a bit located at address 0x1B[23]. This bit is part of the location "PWS".

When set to '1', PWM is enabled and overrides any SENT setting.

If '0', SENT_MODE field determine state of PWM/SENT pin.

PWS.FP_ADJ

Function pulse adjust. Long SSENT (SENT_MODE 7) only. Increases the lower threshold of the F_OUTPUT pulse by the number of ticks in this field (0-3).

Location 0x1C ("ANG")

ANG.zero_offset

The field "zero_offset" is a bit field located at address 0x1C[11:0]. This bit field is part of the location "ANG".

Post-compensation zero offset (or DC adjust) at angle resolution. This value is subtracted from the measured angle. PWS.ZAL bit determines if zero_offset is applied before or after linearization.

ZAL = 0 zero_offset comes before linearization.
ZAL = 1, zero_offset comes after linearization.

ANG.hysteresis

The field "hysteresis" is a bit field located at address 0x1C[17:12]. This bit field is part of the location "ANG".

Angle hysteresis threshold, angle resolution × 4 (14 bit). Range is about 0 to 1.384 degrees.

ANG.ro

The field "ro" is a bit located at address 0x1C[18]. This bit is part of the location "ANG".

Rotation Direction (post-linearization). If set to 0, increasing angle movement is in the clockwise direction when looking down on the top of the die. If set to 1, increasing angle movement is in the counter-clockwise direction.

ANG.rd

The field "rd" is a bit located at address 0x1C[19]. This bit is part of the location "ANG".

Rotate die. Rotates final angle by 180 degrees. This is the very last step in the angle processing algorithm. This is a convenient setting to adjust one die in a dual-die package for conformance to the other die.

ANG.orate

The field "orate" is a bit field located at address 0x1C[23:20]. This bit field is part of the location "ANG".

Reduces the output rate by averaging samples. 2^{orate} samples will be averaged. ORATE values above 12 are reduced to 12 in the logic, meaning that up to 4096 samples = 4 ms can be selected as averaging time.

Location 0x1D ("LPC")

LPC.tcp

The field "tcp" is a bit located at address 0x1D[11]. This bit is part of the location "LPC".

Turns counter PLL:

   0 – Turns used ZCD angle.

   1 – Turns uses PLL angle, except if PLL lock is lost. Make sure the "zcd_turns_offset" aligns the ZCD angle close to the PLL angle.

LPC.turns_init

The field "turns_init" is a bit field located at address 0x1D[19:18]. This bit field is part of the location "LPC".

Turns initialization at power up.

   00, 01 – Turns counter zeroed at power-up.
   10 – Turns counter set to full settings angle (turns register may be non-zero).
   11 – Turns counter set to settled angle offset from 180 or 45 configuration (MSB 10 or 12 bits zeroed), turns register will start out zero.

LPC.t45

The field "t45" is a bit located at address 0x1D[23]. This bit is part of the location "LPC".

Turns counter resolution is 45° if set to a '1', and 180° if set to a '0'.

Location 0x1E ("COM")

COM.mag_thres_lo

The field "mag_thres_lo" is a bit field located at address 0x1E[5:0]. This bit field is part of the location "COM".

Magnetic field low comparator value, field value equals low field error threshold in gauss divided by 16.

COM.mag_thres_hi

The field "mag_thres_hi" is a bit field located at address 0x1E[11:6]. This bit field is part of the location "COM".

Magnetic field high comparator value, field value equals maximum field threshold in gauss divided by 32. If set to 0, high threshold is disabled.

COM.dhr

The field "dhr" is a bit located at address 0x1E[12]. This bit is part of the location "COM".

Disable hard reset in serial CTRL register special if '1'.

COM.dst

The field "dst" is a bit located at address 0x1E[13]. This bit is part of the location "COM".

Disable self-test initiation in serial CTRL register special if '1'.

COM.cud

The field "cud" is a bit located at address 0x1E[14]. This bit is part of the location "COM".

If '1', the "customer" word 0x1F will use the "dur" and "del" configuration in addition to the "customer2" word 0x17.

COM.del

The field "del" is a bit located at address 0x1E[16]. This bit is part of the location "COM".

Disable EEPROM lock for CUST2 (EEPROM word 0x17) and, if CUD = 1, CUST word 0x1F. EEPROM lock will not affect write-ability of word 0x17 (and 0x1F if enabled).

COM.dur

The field "dur" is a bit located at address 0x1E[17]. This bit is part of the location "COM".

Disable unlock requirement for CUST2 (EEPROM word 0x17) and if CUD = 1, CUST word 0x1F.

COM.cse

The field "cse" is a bit located at address 0x1E[18]. This bit is part of the location "COM".

Enable CVH self-test at power-up.

COM.lbe

The field "lbe" is a bit located at address 0x1E[19]. This bit is part of the location "COM".

Power-up logic BIST enable.

COM.lock

The field "lock" is a bit field located at address 0x1E[23:20]. This bit field is part of the location "COM".

Lock options:

1100 – Lock EEPROM writes.
0011 – Lock EEPROM writes AND shadow register writes.

Location 0x1F ("CUS")

CUS.customer

The field "customer" is a bit field located at address 0x1F[23:0]. This bit field is part of the location "CUS". This field may be written with customer tracking, ID, or any other pertinent data.

Location 0x20 ("LIN00")

LIN00.Linearization Error Segment 0

The field "Linearization Error Segment 0" is a bit field located at address 0x20[11:0]. This bit field is part of the location "LIN00".

Correction value at segment boundary. Signed, resolution is based on LS bit. Will be subtracted from sensor angle to produce linearized angle.

For LS = 0, range is ±22.5 degrees.
For LS = 1, range is ±45 degrees.

LIN00.Linearization Error Segment 1

The field "Linearization Error Segment 1" is a bit field located at address 0x20[23:12]. This bit field is part of the location "LIN00".

Correction value at segment boundary. Signed, resolution is based on LS bit. Will be subtracted from sensor angle to produce linearized angle.

For LS = 0, range is ±22.5 degrees.
For LS = 1, range is ±45 degrees.

NOTE: linearization segments 2…29 have been omitted from the datasheet for reasons of brevity.

Location 0x2F ("LIN15")

LIN15.Linearization Error Segment 30

The field "Linearization Error Segment 30" is a bit field located at address 0x2F[11:0]. This bit field is part of the location "LIN15".

Correction value at segment boundary. Signed, resolution is based on LS bit. Will be subtracted from sensor angle to produce linearized angle.

For LS = 0, range is ±22.5 degrees.
For LS = 1, range is ±45 degrees.

LIN15.Linearization Error Segment 31

The field "Linearization Error Segment 31" is a bit field located at address 0x2F[23:12]. This bit field is part of the location "LIN15".

Correction value at segment boundary. Signed, resolution is based on LS bit. Will be subtracted from sensor angle to produce linearized angle.

For LS = 0, range is ±22.5 degrees.
For LS = 1, range is ±45 degrees.

SAFETY AND DIAGNOSTICS

The A33003 was developed in accordance to the ASIL design flow. It incorporates several diagnostics.

Alive Counter

A 32-bit counter increments periodically from zero after power-on or hard reset. It is read via AUX.ALV. The alive increment period is 8.192 ms.

The alive counter can overflow. The overflow period of the counter is $[2^{32} \times 8.192]$ milliseconds. This period is approximately 400 days.

Oscillator Watchdogs

The watchdogs run constantly when in full power or "wake" modes. They are disabled during sleep mode, and are reset when waking up to ensure there is not a false positive due to a partial clock count. These watchdogs are intended to detect gross failures of either oscillator. Logic running on clocks based on each oscillator effectively counts clock periods produced in the other clock domain and compares to expected limits.

Logic Built-In Self-Test (LBIST)

Logic BIST is implemented to verify the integrity of the A33003 logic. It can be executed in parallel with the CVH self-test. LBIST is effectively a form of auto-driven scan. The logic to be tested is broken into 31 scan chains. The chains are fed in parallel by a 31-bit linear feedback shift register (LFSR) to generate pseudorandom data. The output of the scan chains are fed back into a multiple input shift register (MISR) that accumulates the shifted bits into a 31-bit signature.

LBIST takes approximately 30 ms to complete.

LBIST can be enabled to run on power up by setting COM.LBE bit in EEPROM (0x1E bit 19).

The test is complete following initialization when either:

- STA.sdn = 1 (special done) or
- STA.lbr = 0 (LBIST not running).

A failure is indicated by ERR.stf = 1.

CVH Self-Test

CVH self-test is a method of verifying the operation of the CVH transducer without applying an external magnetic field. This feature is useful for both manufacturing test and for integration debug. The CVH self-test is implemented by changing the switch configuration from the normal operating mode into a test configuration, allowing a test current to drive the CVH in place of the magnetic field. By changing the direction of the test current and by changing the elements in the CVH that are driven, the self-test circuit emulates a changing angle of magnetic field. The measured angle is monitored to determine a passing or failing device.

CVH self-test typically takes 52 ms to verify.

Self-test can be run on power-up, by setting the EEPROM field COM.CSE = 1.

Self-test can also be invoked via the serial control register by issuing the corresponding "special" command.
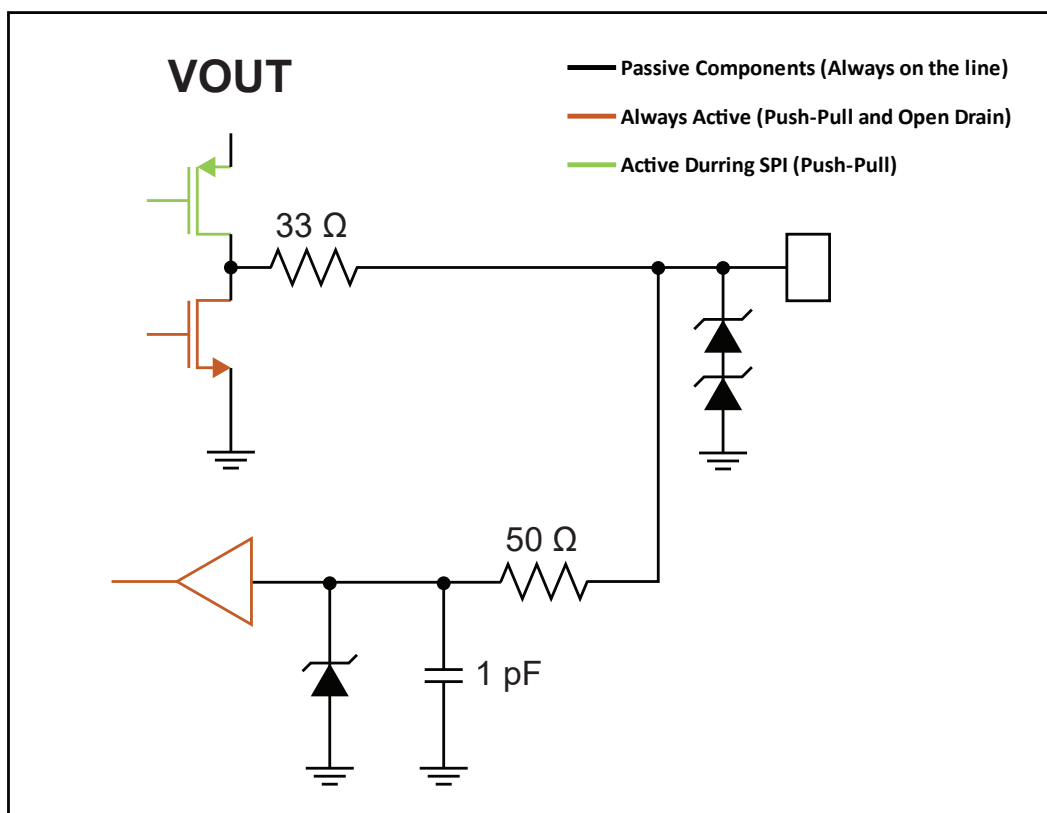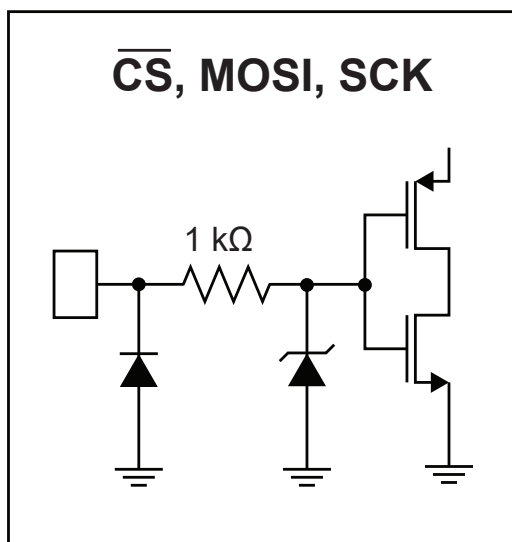
The test is complete when either:

- "STA.sdn" = 1 (special done) or
- "STA.cstr" = 0 (CVH self-test not running).

Failure is indicated by:

- "ERR.stf" = 1 (assuming it was cleared before test was run).

I/O STRUCTURES

$\overline{\text{CS}}$, MOSI, SCK

1 kΩ

VOUT

— Passive Components (Always on the line)

— Always Active (Push-Pull and Open Drain)

— Active Durring SPI (Push-Pull)

33 Ω

50 Ω

1 pF

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000381, Rev. 1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
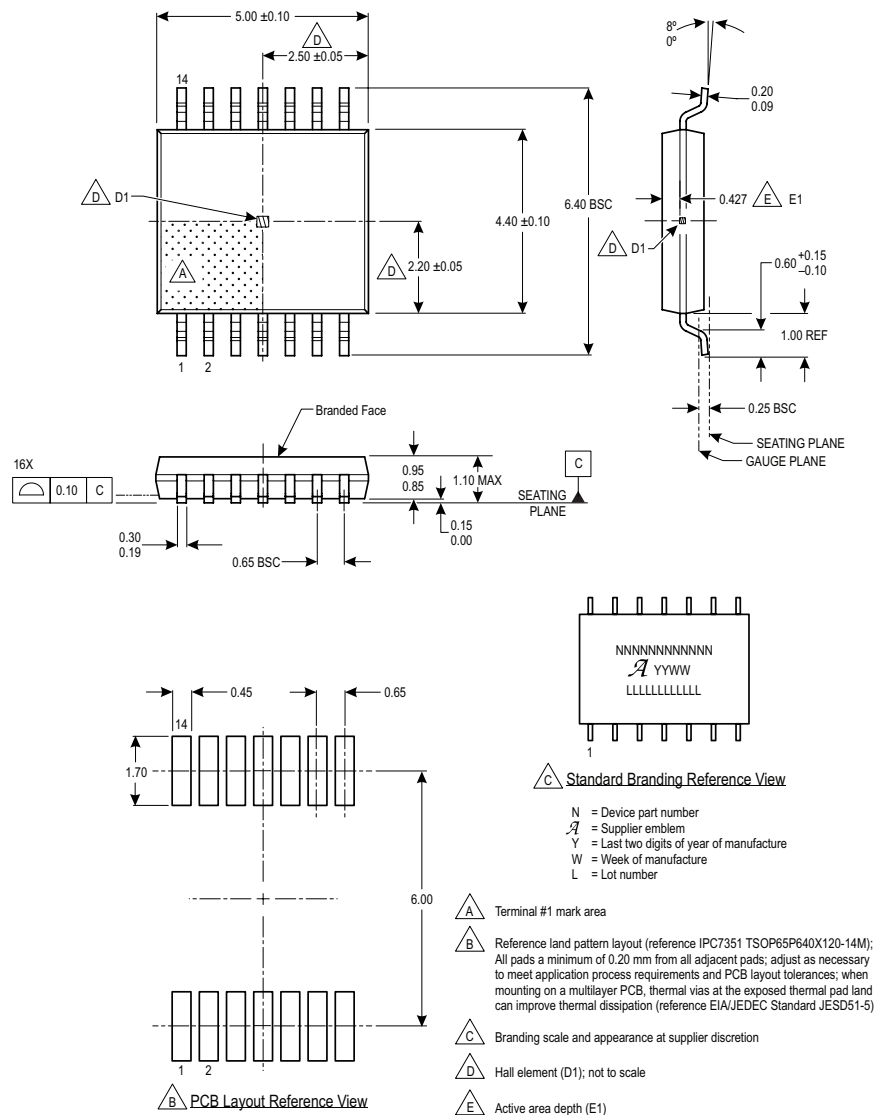Exact case and lead configuration at supplier discretion within limits shown

Standard Branding Reference View

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

A — Terminal #1 mark area

B — Reference land pattern layout (reference IPC7351 TSOP65P640X120-14M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C — Branding scale and appearance at supplier discretion

D — Hall element (D1); not to scale

E — Active area depth (E1)

PCB Layout Reference View

Figure 37: Package LU, 14-Pin TSSOP, Single Die

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000381, Rev. 1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

5.00 ±0.10
2.50 D
6.40 BSC
4.40 ±0.10
2.20 D
D1 D2
A
14
1   2

8°
0°
0.20
0.09
0.427 E E2
0.274 E E1
D2 D D D1
0.60 +0.15 −0.10
1.00 REF
0.25 BSC
SEATING PLANE
GAUGE PLANE

Branded Face
16X
0.10 C
0.95
0.85
1.10 MAX
0.15
0.00
SEATING PLANE
C
0.30
0.19
0.65 BSC

0.45   0.65
14
1.70
6.00
1   2

B PCB Layout Reference View

NNNNNNNNNNNN
$\mathcal{A}$ YYWW
LLLLLLLLLLLL
1

C Standard Branding Reference View

N = Device part number
$\mathcal{A}$ = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-14M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary
to meet application process requirements and PCB layout tolerances; when
mounting on a multilayer PCB, thermal vias at the exposed thermal pad land
can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall elements (D1, D2); not to scale

E Active area depth (E1, E2)

Figure 38: Package LU, 14-Pin TSSOP, Dual Die

APPENDIX A: SENT OUTPUT DESCRIPTION

SENT Output Mode

The SENT output converts the measured magnetic field angle to a binary value mapped to the Full-Scale Output (FSO) range of 0 to 4095, shown in Figure 39. This data is inserted into a binary pulse message, referred to as a frame, that conforms to the SENT data transmission specification (SAEJ2716 JAN2010).

The SENT frame can be configured by setting the following parameters in EEPROM (shown in Figure 39):

- SENT_MODE
- SENT_DRIVER
- DATA_MODE
- SCN_MODE
- SENT_ENABLE
- SENT_TICK
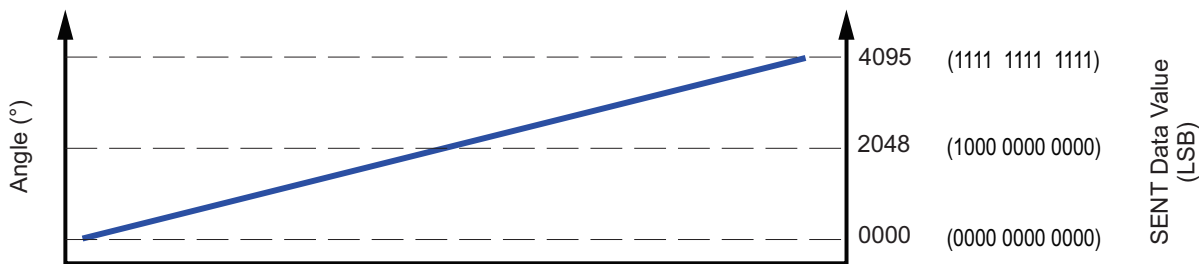
Figure 39: Angle is Represented as a 12-bit Digital Value

Table 18: Main SENT Parameter Location*

Address	Bits	Parameter Name	Description
0x19	22:16	SENT_TICK	Sets Tick rate coefficient.
	14:12	SENT_MODE	Sets frame update rate, enables TSENT, SSENT, ASENT.
	11:8	DATA_MODE	Set data nibble format.
	7	CIS	CRC nibble includes the Status and Communication Nibble data.
	6:4	SCN_MODE	Configure Status and Communication nibble contents.
0x1B	23	PEN	PWM enable. When "1" this overrides the SENT_MODE setting.
	6:4	SENT_DRIVER	SENT pin drive strength.

* For information on SSENT/ASENT configurations bits, see specific SSENT/ASENT section.

MESSAGE STRUCTURE

Data within a SENT message frame is represented as a series of nibbles, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval.

- The low-voltage interval acts as the delimiting state which acts as a boundary between each nibble. The length of this low-voltage interval is fixed at 5 ticks.

- The high-voltage interval performs the job of the information state and is variable in duration in order to contain the data payload of the nibble.

- The slew rate of the falling edge may be adjusted using the SENT_DRIVER parameter.

The duration of a nibble is denominated in ticks. The period of a tick is set by the SENT_TICK parameter. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The parts of a SENT message are arranged in the following required sequence (see Table 18):

1. **Synchronization and Calibration:** Flags the start of the SENT message.

2. **Status and Communication Nibble:** Provides A33003 status and the optional serial data determined by the setting of the SCN_MODE parameter.

3. **Data:** Angle information and optional data.

4. **CRC:** Error checking.

5. **Pause Pulse (optional):** Fill pulse between SENT message frames.

Figure 40: General Value Formation for SENT

0000 (left), 1111 (right)

Table 19: Nibble Composition and Value

Quantity of Ticks			Binary (4-bit) Value	Decimal Equivalent Value
Low-Voltage Interval	High-Voltage Interval	Total		
5	7	12	0000	0
5	8	13	0001	1
5	9	14	0010	2
⋮	⋮	⋮	⋮	⋮
5	21	26	1110	14
5	22	27	1111	15
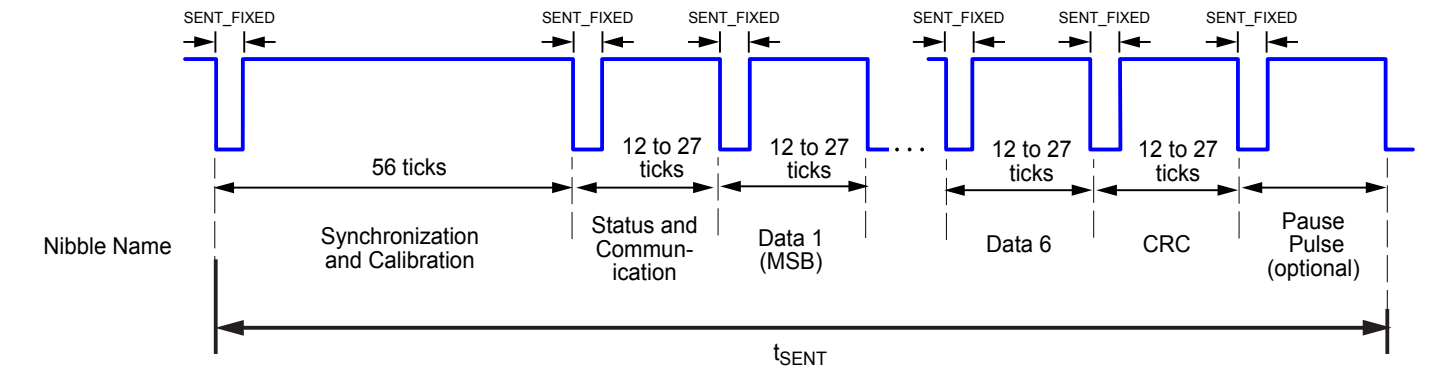
Figure 41: General Format for SENT Message Frame
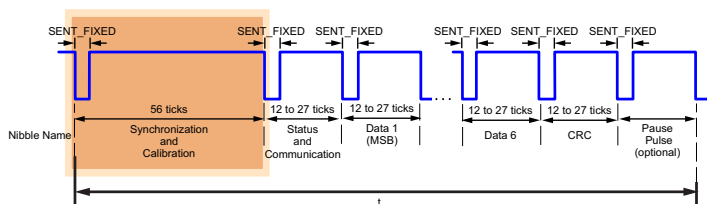
Synchronization and Calibration Pulse

Figure 42: Synchronization and Calibration Pulse within the SENT Message Frame

The Synchronization and Calibration pulse is 56 ticks wide, measured from falling-edge to falling edge, and delineates the start of a new message frame. The host microcontroller uses this pulse to rescale the subsequent nibble values to correct for clock variation between the controller and the sensor.
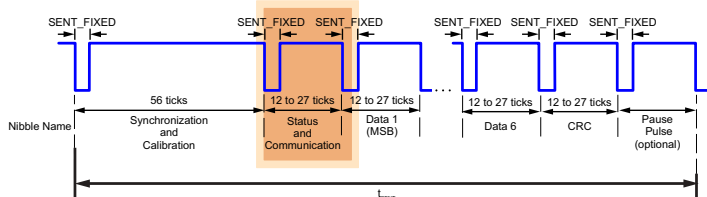
Status and Communication Nibble

Figure 43: Status and Communication Nibble within the SENT Message Frame

The Status and Communication Nibble (SCN) provides diagnostic information along with other status and environmental data. Nibble contents are controlled via the SCN_MODE field within EEPROM. By default, contents of the SCN are not included in the 4-bit CRC at the end of each SENT frame. The CIS bit within EEPROM enables CRC coverage of the SCN contents. It should be noted that this option is not specified in the J2716 SENT standard. With the CIS bit set, the CRC is no longer compliant with that outlined in the SENT specification.

The SCN has three different types of bit values which may be present, depending on the SCN_MODE setting. These are:

a) **Soft/Hard Error:** Overall condition of the A33003, separated into Soft and Hard error flags. Detailed error information can be obtained via the expanded data nibbles, set via DATA_MODE, or through the slow serial communication.

Hard Error Flag:

Hard error flags cannot be masked and will assert independent of EEPROM mask bits.

- Latched indefinitely if any of the following occur:
  □ Watchdog Timeout
  □ EEPROM hard error (multi-bit fault)
  □ Self-test error
- Temporarily sets but clears after the following conditions pass:
  □ Reset/POR
  □ ZCD integrity error
  □ Angle averaging error
  □ Temperature sensor out of range
  □ PLL not in lock

Soft Error Flag:

Soft error flag may be masked by setting the appropriate mask bit in EEPROM address 0x1A.

- Latched temporarily, clears on next SENT frame unless condition is still asserted.
  □ Any unmasked errors asserted

b) **ID data:** Die ID bits set via SA0 (SCLK) and SA1 (MOSI) pins.
- ID[0]: Value set by the logic level of the SA0 pin.
- ID[1]: Value set by the logic level of the SA1 pin.

c) **Serial Data:** Two bits, consisting of the SerialSync and SerialData bits. Together they form the Short Serial Message (per J2716 Section 5.2.4.1).
- SerialSync: Indicates the start of a 16-bit serial message.
- SerialData: Serial data, transmitted one bit at a time, MSB first.

Table 20: SCN Bit Contents

SCN_MODE	Bit 3	Bit 2	Bit 1	Bit 0
000	0	0	Soft	Hard
001	SerialSync	SerialData	Soft	Hard
010	ID[1]	ID[0]	Soft	Hard
011	0	0	0	Soft+Hard
100	0	0	ID[1]	ID[0]
101	SerialSync	SerialData	ID[1]	ID[0]
110	Soft	Hard	ID[1]	ID[0]
111	SerialSync	SerialData	0	Soft+Hard

Short Serial Message Format

The SENT specification allows additional data transfer via specific bits within the SCN. This data stream is also referred to as the "Slow Channel".

The A33003 implements "Short Serial Message Format" as described in paragraph 5.2.4.1 of the SAE-J2716 specification. A 16-bit data packet is transmitted one bit at a time over consecutive SENT message frames, starting with the MSB. The beginning of each 16-bit packet is indicated by a "1" in the SerialSync bit. The message data is transmitted bit-by-bit via the SerialData bit. The 16-bit message packet is separated into 3 different fields:

a) Message ID (4 bits):
   Four leading bits of the serial data packet, used to identify data contents. Data rotates through the 16 message IDs as shown in Table 21. The Message ID may be considered the 4 LSB of a 12-bit alive counter that increments every 16 SENT frames

b) Message Data (8 bits):
   Eight bits of data.

c) CRC (4 bits):
   CRC checksum, used to validate the Message ID and Data. Same CRC algorithm as that used for the SENT message frame.

Sixteen separate SENT frames are needed to construct a complete 16-bit serial message. To transmit all 8 unique serial data messages (Message ID 0-7), a total of 128 SENT transmission are necessary. 256 SENT transmissions are required for a complete rotation of the 16 message IDs.

Table 21: Short Serial Message Format in SENT Status and Communication Nibble

SNC Bit	Nibble #															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SerialSync	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SerialData	Message ID				Data								CRC			

Table 22: Serial Output Data

Message ID (4 bits)	Data (8 bits)
0 (8)	8-bit Alive counter (increments by one, every 0-15 rotation of the Message ID field))
1 (9)	Temperature in degrees Celsius, offset by +64 (subtract 64 to get measured temperature)
2 (10)	STATUS, bits [15:8] See Table 19.
3 (11)	STATUS, bits [7:0] See Table 19.
4 (12)	Magnetic field reading in gauss, divided by 8 (multiply by 8 to obtain gauss rating)
5 (13)	Customer[23:16] from EEPROM 0x1F.
6 (14)	Customer[15:8] from EEPROM 0x1F.
7 (15)	Customer[7:0] from EEPROM 0x1F.

SENT Data Nibbles:

The angle value is embedded within the first three (if using a 12-bit angle value) or four (if using a 16-bit angle value) nibbles of every SENT frame and transmitted MSB first. Additional information may be transmitted by extending the number of data nibbles, up to 6. The contents and number of data nibbles in every SENT frame is configured using the DATA_MODE field in EEPROM.
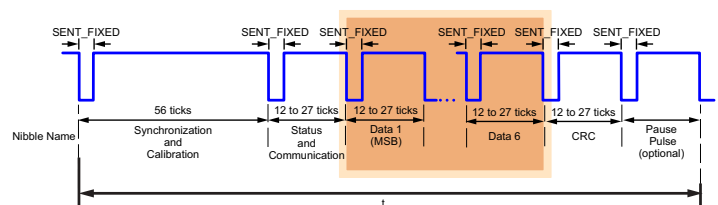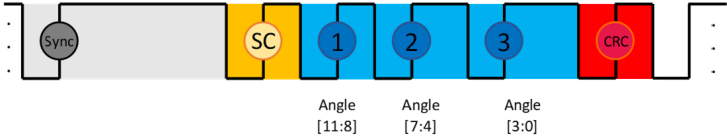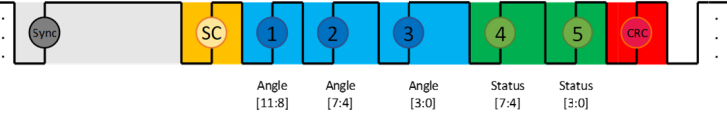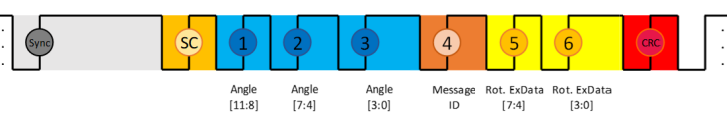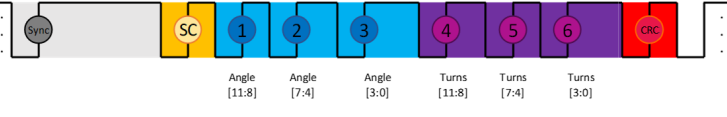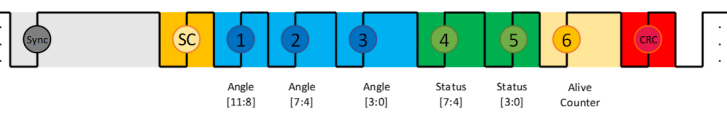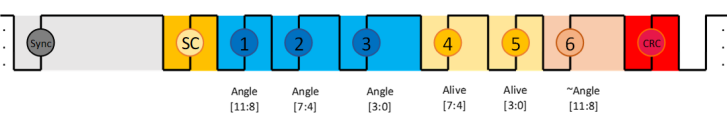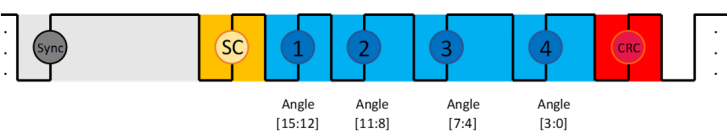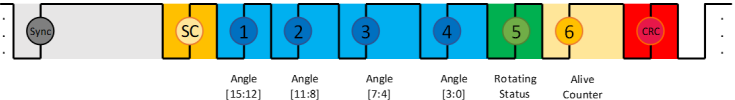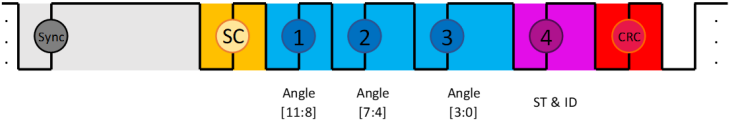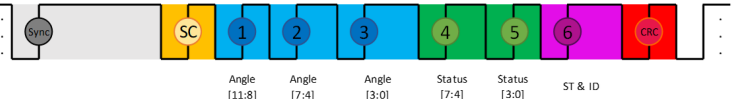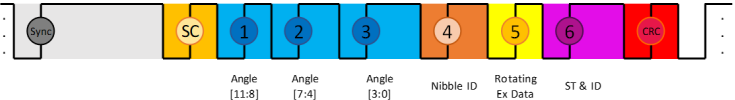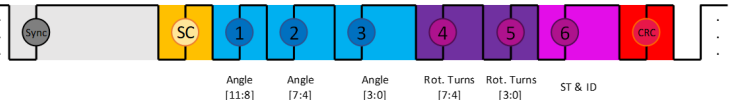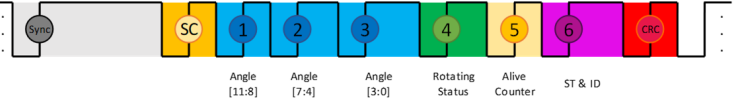

Figure 44: SENT Data Nibbles within the SENT Message Frame

SENT Data Mode Options

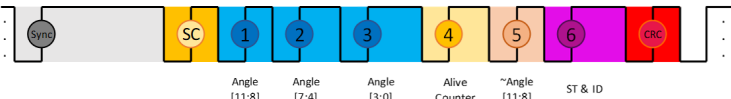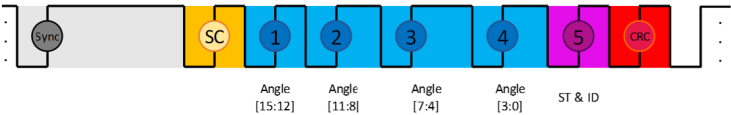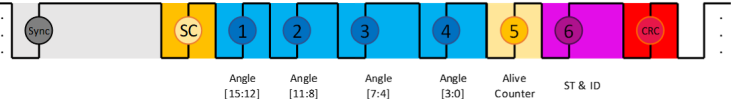|	
DATA_Mode = 0 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data CRC = Cyclical Redundancy Check	
DATA_Mode = 1 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data 4,5 = Rotating Status bits CRC = Cyclical Redundancy Check	 Status[0] = '0': Status[7:1] = Upper 7 bits of SENT status flags Status[0] = '1': Status [7:1] = Lower 7 bits of SENT status flags See Table 23 for details of each status flag.
DATA_Mode = 2 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data 4 = Message ID 5,6 = Rotating Extended Data CRC = Cyclical Redundancy Check	 Rotating Extended Data (Nibbles 5 and 6) follow the serial message format. Message ID (Nibble 4) indicates the ID for each 8-bit packet of the serial message. See Table 21 and Table 22.
DATA_Mode = 3 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data 4,5,6 = Turns Counter CRC = Cyclical Redundancy Check	
DATA_Mode = 4 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data 4,5 = Rotating Status 6 = Alive Counter CRC = Cyclical Redundancy Check	 Status[0] = '0': Status[7:1] = Upper 7 bits of SENT status flags Status[0] = '1': Status [7:1] = Lower 7 bits of SENT status flags
DATA_Mode = 5 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data 4,5 = Alive Counter 6 = 1's Complement of Data Nibble 1 CRC = Cyclical Redundancy Check	 When combined with SCN_MODE =3, this implements the "Single Secure Sensor" requirement outlined in SAE-J2716 Appendix A.
DATA_Mode = 6 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3,4 = Angle Data CRC = Cyclical Redundancy Check	

DATA_Mode = 7 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3,4 = Angle Data 5 = Rotating Status 6 = Alive Counter CRC = Cyclical Redundancy Check	 Angle [15:12] Angle [11:8] Angle [7:4] Angle [3:0] Rotating Status Alive Counter Status rotates through the Status register. Alive Counter [1:0] can be used to identify the quadrant of the Status data.
DATA_Mode = 8 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data 4 = Self-Test and ID CRC = Cyclical Redundancy Check	 Angle [11:8] Angle [7:4] Angle [3:0] ST & ID
DATA_Mode = 9 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data 4,5 = Rotating Status 6 = Self-Test and ID CRC = Cyclical Redundancy Check	 Angle [11:8] Angle [7:4] Angle [3:0] Status [7:4] Status [3:0] ST & ID Status[0] = '0': Status[7:1] = Upper 7 bits of SENT status flags Status[0] = '1': Status [7:1] = Lower 7 bits of SENT status flags
DATA_Mode = 10 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data 4 = Nibble ID 5 = Rotating Extended Data 6 = Self-Test Flag and ID CRC = Cyclical Redundancy Check	 Angle [11:8] Angle [7:4] Angle [3:0] Nibble ID Rotating Ex Data ST & ID Rotating Extended Data (Nibbles 5) follow the serial message format. Message ID = 0 indicates Rotating Data is 4 MSBs of 1st packet. Message ID = 1 indicates Rotating Data is 4 LSBs of 1st packet. See Table 21 and Table 22. Also see the detailed DATA_MODE descriptions below
DATA_Mode = 11 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data 4,5 = Rotating Turns Counter CRC = Cyclical Redundancy Check	 Angle [11:8] Angle [7:4] Angle [3:0] Rot. Turns [7:4] Rot. Turns [3:0] ST & ID Rotating Turns [7] = '0': Rotating Turns [6:0] = Upper half of turns register. Rotating Turns [7] = '1': Rotating Turns [6:0] = Lower half of turns register.
DATA_Mode = 12 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data 4 = Rotating Status 5 = Alive Counter 6 = Self-Test and ID CRC = Cyclical Redundancy Check	 Angle [11:8] Angle [7:4] Angle [3:0] Rotating Status Alive Counter ST & ID Status rotates through the Status register. Alive Counter [1:0] can be used to identify the quadrant of the Status data.

ALLEGRO microsystems

DATA_Mode = 13 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3 = Angle Data 4 = Alive Counter 5 = 1's Compliment of Nibble 1 6 = Self-Test and ID CRC = Cyclical Redundancy Check	 Modified version of the "Single Secure Sensor" implementation as outlined in Appendix A of SAE-J2716
DATA_Mode = 14 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3,4 = Angle Data 5 = Self-Test and ID CRC = Cyclical Redundancy Check	
DATA_Mode = 15 Data Nibbles: Sync = Synchronization Pulse SC = Status & Communication Nibble 1,2,3,4 = Angle Data 5 = Alive Counter 6 = Self-Test and ID CRC = Cyclical Redundancy Check	

Self-Test and ID Nibble

The Self-Test and ID (ST&ID) nibble is optional. It is included as one of the extended nibbles when using DATA_MODEs 4-7. This nibble consists of three data bits (MSB is always 0), shown below:

Bit 3	Bit 2	Bit 1	Bit 0
0	ST	ID[1]	ID[0]

Figure 45: ST & ID Nibble

The ST bit, indicates a failure of one of the three internal self-tests (CVH self-test and Logic BIST). If set, this indicates significant failure of the sensor, and a reset should be initiated.

ID[0] and ID[1] provide the sensor ID value as determined via the logic values of the SA0 and SA1 pins.

This nibble is particularly useful when sharing SENT lines, as it allows the Self-Test diagnostic results and corresponding sensor ID to be quickly determined without a significant latency penalty (only one nibble to the SENT frame).

SENT Status Bit Description

The A33003's extensive status and error flags may be read at any time via SPI, or by entering Manchester Communication Mode. To facilitate error/status flag reporting by way of the unidirectional SENT protocol, a selection of these flags are communicated via extra data nibbles when using DATA_MODEs 1, 4, 7, 9, or 12. These status flags are also transmitted via the slow serial protocol through the SCN.

The flags are 0 if the condition is clear and 1 if the condition is true. For transient conditions, the flag will clear after the bit is presented on the SENT output.

Table 23: SENT Status Flag Definitions

Bit	Symbol	Definition
15	SF15	PLL not in lock.
14	SF14	Angle averaging (ORATE) or zero-crossing integrity error.
13	SF13	POR (power-on-reset) occurred.
12	SF12	Temperature sensor out of range.
11	SF11	Self-test error (CVH self-test or LBIST).
10	SF10	EEPROM hard error.
9	SF9	Oscillator watchdog error.
8	R	Always 0. Indicates MSB byte.
7	SF7	Magnetic Sense Low.
6	SF6	Undervoltage, on V_{CC} line or analog regulator output.
5	SF5	EEPROM soft error.
4	SF4	Saturation in math computations.
3	SF3	SENT contention.
2	SF2	Magnetic sense high.
1	SF1	Turns counter overflow.
0	R	Always 1. Indicates LSB byte.

Status Flag Locations for SENT Data_mode 1, 4, and 9 (over 2 SENT Frames)

Nibble4				Nibble5			
SF15	SF14	SF13	SF12	SF11	SF10	SF9	R (0)

Nibble4				Nibble5			
SF7	SF6	SF5	SF4	SF3	SF2	SF1	R (1)

Status Flag Locations for SENT Data_mode 7 and 12 (over 4 SENT Frames)

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
SF15	SF14	SF13	SF12	X	X	0	0

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
SF11	SF10	SF9	R(0)	X	X	0	1

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
SF7	SF6	SF5	SF4	X	X	1	0

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
SF3	SF2	SF1	R(1)	X	X	1	1

Turns Count Information for SENT Data_mode 11 (over 2 SENT Frames)

Nibble4			Nibble5
0	0	Turns[11:10]	Turns[9:6]

Nibble4			Nibble5
1	0	Turns[5:4]	Turns[3:0]

Rotating Data Information for SENT Data_mode 10
(rotates over 16 SENT frames)

Nibble 4 (Rotating Data)				Nibble 5 (Rotating Data)			
NibID				NibData			
0	0	0	0	8-bit Alive counter MSBs [7:4]			
0	0	0	1	8-bit Alive counter LSBs [3:0]			
0	0	1	0	Temperature MSBs [7:4]			
0	0	1	1	Temperature LSBs [3:0]			
0	1	0	0	SF15	SF14	SF13	SF12
0	1	0	1	SF11	SF10	SF9	0
0	1	1	0	SF7	SF6	SF5	SF4
0	1	1	1	SF3	SF2	R	1
1	0	0	0	Magnetic Field [7:4]			
1	0	0	1	Magnetic Field [3:0]			
1	0	1	0	CUSTOMER [23:20]			
1	0	1	1	CUSTOMER [19:16]			
1	1	0	0	CUSTOMER [15:12]			
1	1	0	1	CUSTOMER [11:8]			
1	1	1	0	CUSTOMER [7:4]			
1	1	1	1	CUSTOMER [3:0]			

ALLEGRO
microsystems

SENT CRC Nibble

The CRC nibble is a 4-bit error checking code, implemented per the SAE-J2716 SENT "recommended" specification.

The CRC is calculated using the polynomial $x^4 + x^3 + x^2 + 1$, initialized to 0101.

By default, the checksum covers only the contents of the data nibbles (3-6 nibbles). By setting the CIS bit within EEPROM, the contents of the SCN are included within the CRC nibble which deviates from the SENT standard.
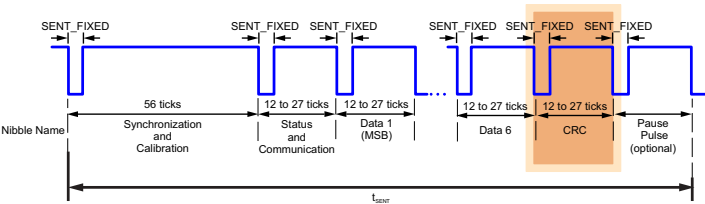

Figure 46: CRC Nibble within the SENT Message Frame

SENT Pause Pulse (Optional)

The Pause Pulse is an optional addition to the SENT message frame, transmitted following the CRC nibble. It acts to "fill-in" the frame until the beginning of the next SENT transmission.

The pulse may behave in one of two ways, based on the SENT_MODE setting.

With SENT_MODE set to 2, a Pause Pulse will be inserted until new angle data is available. The inserted Pause Pulse is a minimum of 12 Ticks in length. If a pause longer than 768 Ticks is required, the pulse will restart requiring a minimum of 12 more Ticks.

For SENT_MODE values greater than 3-7, the sensor operates in either triggered or addressable/sequential SENT mode. In these modes the sensor outputs a SENT message frame in response to host action (either a trigger or a function pulse). When not responding to the host the sensor will output a Pause Pulse of indefinite length (i.e. remains high until a host request).
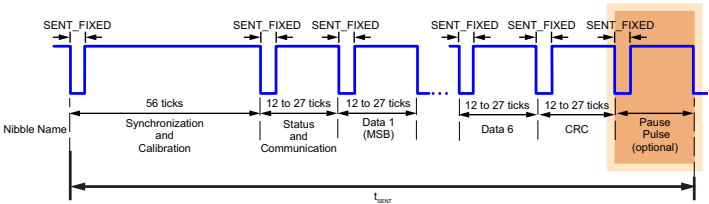
Figure 47: Pause Pulse within the SENT Message Frame

SENT_MODE 2	Low	High	Low	High
	5 Ticks	7 to 763 Ticks	5 Ticks	7 to 763 Ticks

SENT_MODEs 3 through 7	Low	High	Low (host)
	5 Ticks	Infinite (until pulled low by host)	Trigger (Min of 1.8 µs) or Function Pulse

Figure 48: SENT Pause Pulse

SENT OUTPUT MODE

The timing and method of SENT transmission may be configured using the SENT_MODE field within EEPROM. The method of SENT transmission falls within the following three categories:

1. Free Running SENT:
   Angle information is automatically placed on the SENT line with no prompting from the host. Depending on settings, the SENT message frames may be transmitted back-to-back, or synchronized with each update of the angle value.

2. Triggered SENT (TSENT):
   A SENT message frame occurs only when initiated by the host. The A33003 sensor will output a continuous Pause pulse, during this the host triggers a SENT frame by pulling the SENT line low for a minimum of $T_{Trig(MIN)}$. Once released the sensor responds with a SENT message frame

3. Shared SENT:
   Two distinct formats. Sequential SENT (SSENT) and Addressable SENT (ASENT). Allow sharing a single SENT line amongst four compatible devices.

SENT_MODE	Visual	Description
000_2 (0)	–	SENT disabled.
001_2 (1)		Streaming output with variable message duration and no pause pulse. Angle data is sampled near the end of the Status and Communication nibble. Maximum age at time of sampling is $2^{ORATE} \times 2$ µs. Depending on Tick time and ORATE setting, same data may be transmitted multiple times. This mode provides the quickest data delivery rate.
010_2 (2)		SENT message frames are synchronized with the device internal update rate. Pause pulse is inserted until fresh data becomes available. Angle data is sampled between 1 to 2 Tick times of the Synchronization pulse. Pause pulse varies in length between 12 to $2^{ORATE} \times 2$ µs (Pulse will restart after 768 ticks).
011_2 (3)		TSENT SCN sampling: Controller initiates a SENT transmission by pulling the line low, during a Pause Pulse. When the controller releases the output, after a delay of t_{dSENT} the SENT message begins. Angle data is latched at the end of the SCN. Data age may be up to $(2^{ORATE} + 2$ µs$) + t_{RESPONSE}$ when latched. This option is useful when the controller requires a prompt with minimum "age" of the angle data.
100_2 (4)		TSENT Falling edge sampling: Similar to SENT_MODE = 3, except angle data is latched once the output line is pulled low. Useful when multiple ICs are connected to a single controller. Allows synchronous sampled data to be retrieved one device at a time, by releasing the trigger for each individual sensor. Data age may by up to $(2^{ORATE} + 2$ µs$) + t_{RESPONSE}$ when latched.
101_2 (5)	–	Addressable SENT (ASENT). See Shared SENT section.
110_2 (6)	–	Sequential SENT (SSENT). See Shared SENT Section.
111_2 (7)	–	Long Sequential SENT. See Shared SENT Section.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SHARED SENT PROTOCOL

Addressable SENT (ASENT) and Sequential SENT (SSENT) are extensions of the Allegro Triggered SENT (TSENT) protocol. ASENT and SSENT allow multiple Allegro sensors with SENT output capability to coexist on a single shared SENT bus. The Host (ECU) is able to select one sensor at a time, addressing that sensor to respond with a SENT output packet, and thus poll each sensor on the bus over some period of time.

ASENT and SSENT, like Triggered SENT, require an open-drain system configuration, in which any sensor, or the Host, can pull the SENT line low. The SENT line is pulled high by an external resistor to a known VCC. A high level is attainable on the bus only when no device is actively pulling the line low.

In ASENT and SSENT, each sensor on the bus is assigned a unique SensorID number between 0 and 3, allowing up to 4 Sensors to co-exist on the bus. This SensorID number is assigned by the logic state of the SA0 and SA1 pins.
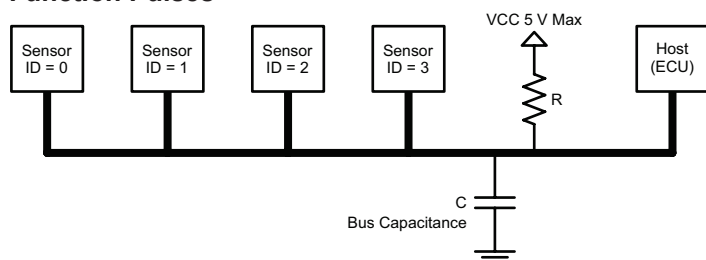
Function Pulses

Figure 49: Shared SENT Bus Example

This section describes the different function pulses that are referenced later during the ASENT and SSENT section.

The host communicates to a sensor or sensors via different Function Pulses, which are equivalent in nature to a TSENT trigger pulse, but with defined widths. A Function Pulse is placed on the SENT bus by the Host pulling the SENT line low for a defined number of Ticks greater than a normal SENT pulse low period.

The duration of the low time is measured by the Sensors and interpreted as a designated Function.
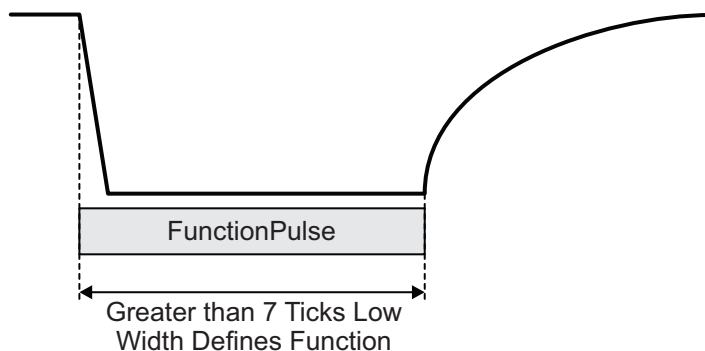

Figure 50: Function Pulse (Output by Host)

Functions that are acted upon by all sensors simultaneously are designated Broadcast Pulses. Functions that are acted upon by only one sensor are designated Addressing Pulses and are associated with a target sensor ID. A Function Pulse may be defined as both a Broadcast and an Addressing pulse. For instance, all sensors will sample and hold data, but only one will transmit a SENT packet.

A sensor that does not support a specific function will not respond to the Function Pulse.

Function Pulses must be greater in duration than the SENT pulse low time (5 Ticks on the A33003) to not be mistaken as a part of a normal SENT transmission

The duration of Function Pulses are defined in SENT Ticks in order to scale with the SENT frame itself. Min and Max pulse durations are set such that they satisfy electrical and timing characteristics.

The various Function Pulses with their expected Tick ranges are shown in Table 24 through Table 26.

Table 24: ASENT Functional Pulses

Function	Type	Related Options	Min Tick	Nom Tick	Max Tick	Description
F_OUTPUT	Addressing/ Broadcast	NO_SAMPLE	15	17	19	Addressed Sensor responds with SENT frame, containing either held data (from F_SAMPLE) or current data.
F_SAMPLE	Addressing/ Broadcast	NO_FSAMPLE SAMPLE_ADR	31	35	39	Sensors sample and hold their magnetic data, unless NO_FSAMPLE = 1. If SAMPLE_ADR = 1, this is also an AddressingPulse, and addressed Sensor responds with SENT frame.
F_AUX	Addressing/ Broadcast	Manchester Communication	56	63	70	Device enabled Manchester communication, if MEPE = '1'. Otherwise, ignored.

Table 25: SSENT Functional Pulses. SENT_MODE = 6

Function	Type	Related Options	Min Tick	Nom Tick	Max Tick	Description
F_OUTPUT	Addressing/ Broadcast	NO_SAMPLE ZERO_SAMPLE	15	17	19	Addressed Sensor responds with SENT frame, containing either held data (from Slot 0 sampling or F_SAMPLE) or current data. If ZERO_SAMPLING = 1 and Slot = 0, Sensors will sample-and-hold their magnetic data.
F_SAMPLE	Addressing/ Broadcast	NO_FSAMPLE SAMPLE_ADR	31	35	39	Sensors sample-and-hold their magnetic data, unless NO_FSAMPLE = 1. If SAMPLE_ADR = 1, this is also an Addressing Pulse, and addressed Sensor responds with SENT frame.
F_AUX	Addressing/ Broadcast	Manchester Communication	56	63	70	Device enabled Manchester communication, if MEPE = '1'. Otherwise, ignored.
F_SYNC	Broadcast		93	104	115	All sensors synchronize their Slot Counters such that the next Slot is for Sensor ID 0.

Table 26: Long SSENT Functional Pulses. SENT_MODE = 7

Function	Type	Related Options	Min Tick	Nom Tick	Max Tick	Description
F_OUTPUT	Addressing/ Broadcast	NO_SAMPLE ZERO_SAMPLE	9 [1]	Per micro controller spec	81	Addressed Sensor responds with SENT frame, containing either held data (from Slot 0 sampling) or current data. If ZERO_SAMPLING = 1 and Slot = 0, Sensors will sample-and-hold their magnetic data.
F_SYNC	Broadcast		105	140	171	All sensors synchronize their Slot Counters such that the next Slot is for Sensor ID 0.
F_AUX	Addressing/ Broadcast	Manchester Communication	216	240	264	Device enables Manchester communication, if MEPE = '1'. Otherwise, ignored.

[1] At tick times less than 1.5 µs, the nominal 5-tick low portion of a SENT pulse within the SENT frame may overlap with F_OUTPUT range, resulting in contention. The low side of the F_OUTPUT pulse may be increased via the PWS.fp_adj EEPROM field. All sensors sharing a bus must have the same fp_adj setting.

Sensor Measurement Range

Sensors measure Function Pulses to a wider range of tick times to allow for variance in falling/rising threshold and oscillator variance from sensor to sensor. The following table gives the sensor measurement ranges for each type of function pulse.

Function	Sensor Measurement Range ASENT or SSENT	Sensor Measurement Range SSENT Long
F_OUTPUT	13-27	7-94
F_SAMPLE	28-49	N/A
F_AUX	50-83	196-297
F_SYNC	84-133 (SSENT only)	95-195

SEQUENTIAL SENT (SSENT)

SSENT Addressing Protocol

The SSENT protocol requires Sensors on the bus to be polled in sequential order, meaning increasing, consecutive, and rotating order by Sensor ID starting with Sensor ID 0. The Slot for a Sensor is the time at which that Sensor is expected to respond to an Addressing Pulse and other Sensors are expected to not respond.

Each Sensor independently maintains a Slot Counter that is incremented each time the Sensor detects an Addressing Pulse. This Slot Counter becomes the Slot Number, which is used by the Sensor to decide which Sensor is being polled by the Host. The Slot Counter is compared to the Sensor ID, and if they match, that Sensor responds with the SENT Frame, and all other Sensors do not respond, although they increment their own Slot Counter.

If the Slot Counter is incremented past the total number of Sensors on the bus (MAX_SENSOR option), the Slot Counter is returned to 0. Each Sensor must be programmed consistently with the total number of Sensors so they all roll over to 0 at the same count. Sensors do not increment their Slot Counter on a Broadcast Pulse.

The SSENT protocol relies on each Sensor maintaining the exact same Slot Number by counting the Addressing Pulses. In order to synchronize all Sensors to the same Slot Number, the SSENT protocol has a broadcast F_SYNC pulse that is used by the Host to force all Sensors to reset their SlotCounter to 0.

Long SSENT (SENT_MODE = 7) allows the A33003 to work with existing shared SENT methodologies. The added overhead decreases the rate at which messages may be transmitted.

In order to reduce the burden on the Host, and also to improve detection and recovery from BusContention or system errors affecting the SENT bus, the SSENT protocol has the following Configuration Options that can be selected.

- SLOT_MARKING. When enabled, each Sensor will wait a different length of time following an Addressing Pulse, based on their Sensor ID. This leaves the SENT bus in a high state for a varying duration before the Sensor pulls the line low to begin the SENT Frame. All Sensors on the bus (including the addressed Sensor) measure this time to interpret the Sensor ID of the transmitting sensor. By comparing this to the Slot Counter, each Sensor can recognize if an unexpected Sensor responded to the Addressing Pulse. By default, the Sensor would then drop Offline, since it cannot be known which Sensor is out-of-sync. This Option increases the overhead on the bus and therefore reduces the maximum rate at which Sensors can be polled. SlotMarking increases the polling time of a Sensor by the Slot Marking time for that Sensor. All sensors on a bus must be configured with the same choice for this option.
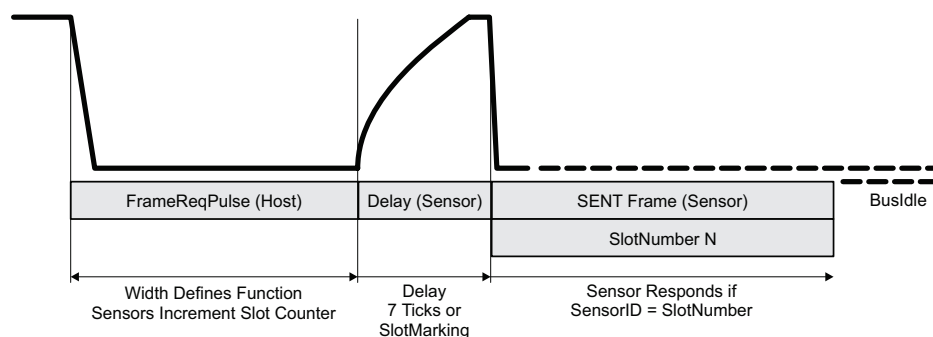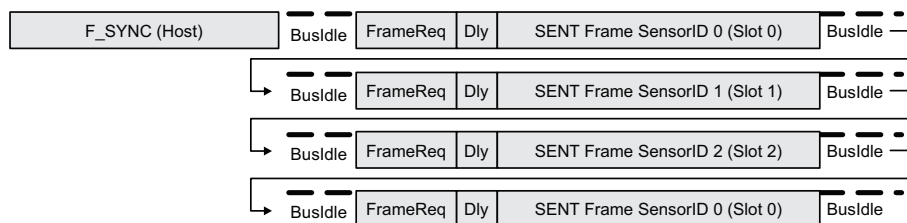

Figure 51: SSENT Sensor Addressing

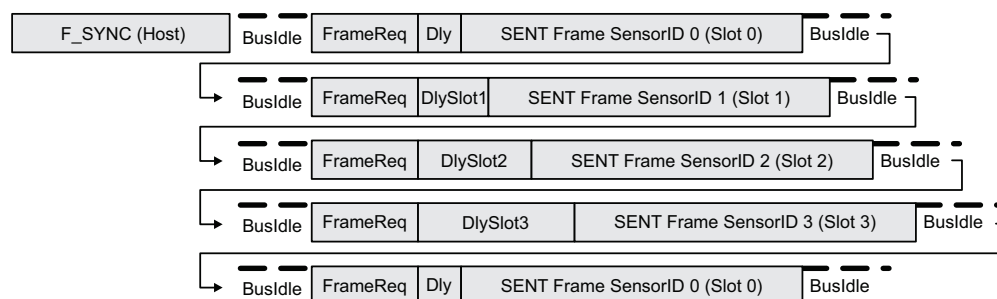**Figure 52: SSENT Sensor Addressing – No Slot Marking (3 Sensors on Bus)**

Figure 53: SSENT Sensor Addressing – With Slot Marking (4 Sensors on Bus)

Table 27: Slot Marking Delay Time

Sensor ID	Delay Time in Ticks (Nominal)
0	7*
1	18*
2	36*
3	62*

* Delay time not intended for use by host. Tick values are approximate and will differ from part to part due to oscillator variance.

- POR_OFFLINE. When enabled, a Sensor will stay Offline until the Host issues F_SYNC, or one of the other synchronization options takes effect (C_IDLE_SYNC). If disabled, a Sensor will power-up with its SlotCounter set to 0, and will go directly Online. This allows the Sensors to initialize without any Host interaction. However, if a Sensor gets power-on-reset after the bus is in operation, its counter may be out-of-sync with other Sensors, and this could result in bus contention.

- IDLE_SYNC. When enabled, a Sensor will monitor the bus for a long high (BusIdle) period greater than 510 ticks and reset its Slot Counter to 0. This option could be used if Sensor polling is expected to always be periodic and continuous, such that the only extended BusIdle time would be after power-up.

SSENT FUNCTION PULSES

- F_OUTPUT: Addressed sensor will return a SENT frame with sampled magnetic data. If there is data from a sample-and-hold operation available (F_SAMPLE or via C_ZERO_SAMPLE = 1), then that data is returned, otherwise current data is sampled and returned. A Sensor configured with C_ZERO_SAMPLE = 1 will sample-and-hold on the rising edge of the F_OUTPUT pulse for Slot 0. A Sensor configured with C_NO_SAMPLE = 1 and C_ZERO_SAMPLE = 0 will never sample-and-hold, so will always return current data in response to F_OUTPUT.

- F_SAMPLE: All sensors except those configured for NO_SAMPLE = 1 will sample-and-hold their data at the rising edge of the pulse. If SAMPLE_ADR = 0, this is a BroadcastPulse to a Sensor, and that Sensor will not respond. If SAMPLE_ADR = 1, this is also an AddressingPulse to a Sensor, and the addressed sensor will return a SENT frame with either the sampled or current data. The SAMPLE_ADR must be configured the same for all parts on the bus.

- F_SYNC: All Sensors will synchronize their Slot Numbers by setting their Slot Counters such that the next Addressing Pulse is for Slot 0.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ADDRESSABLE SENT (ASENT)

ASENT Addressing Protocol

The ASENT protocol allows Sensors to be polled in an arbitrary order. The Sensor ID is transmitted by the Host following any AddressingPulse as a series of 0, 1, 2, or 3 IncAdrPulses. After this sequence, the SENT line is left in a high state, and each sensor will recognize after a time period of about 18 nominal TICKs that there are no more IncAdrPulses coming. The sensor whose ID matches the number of IncAdrPulses received will respond.

ASENT Function Pulses

- F_OUTPUT: Addressed sensor will return a SENT frame with sampled magnetic data. If there is data available from a sample-and-hold operation (F_SAMPLE), then that data is returned, otherwise current data is sampled and returned. A Sensor configured with NO_SAMPLE = 1 will not sample-and-hold, so will always return current data in response to F_OUTPUT.

- F_SAMPLE: All sensors except those configured for NO_ SAMPLE = 1 will sample-and-hold their data at the rising edge of the pulse. If SAMPLE_ADR=0, this is a

BroadcastPulse to a Sensor, and that Sensor will not respond. If SAMPLE_ADR = 1, this is also an AddressingPulse to a Sensor, and the addressed sensor will return a SENT frame with either the sampled or current data. The SAMPLE_ADR must be configured the same for all parts on the bus.

- F_AUX: Sensor(s) will disable output, and wait for a Manchester Access or Exit code. SENT operation will resume if an incorrect Access code or an Exit code is sent to the device. Once the Access code is sent, the Exit code must be sent to return to SENT functionality, and incorrect Manchester messages will be ignored.

ASENT Host Requirements:

- The Host must initiate SENT frame output by selecting appropriate Function pulses.

- The Host must detect timeouts or SENT frame contention following any Function pulse and take appropriate recover action.
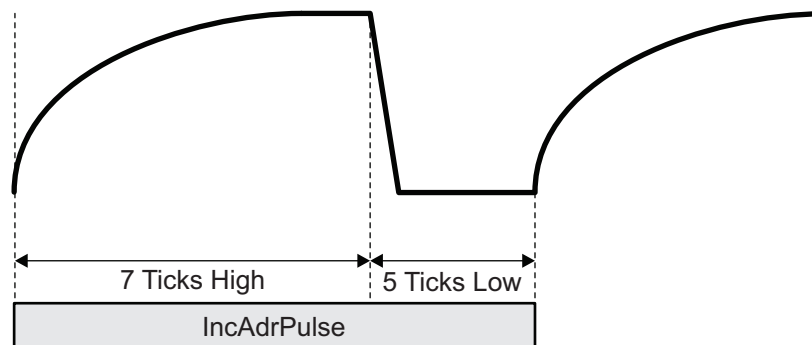

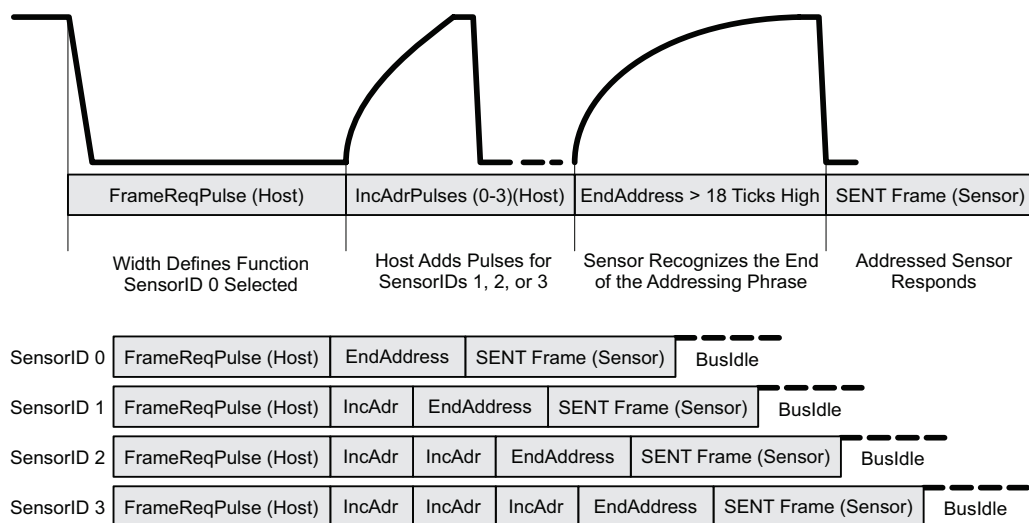**Figure 54: ASENT IncAdrPulse (Output by Host)**

Figure 55: ASENT Sensor Addressing

SENSOR MAGNETIC DATA SAMPLING

Sensors sample their magnetic data based on a combination of FunctionPulse and configuration options. There are two types of sampling supported: SampleOnOutput and SampleAndHold.

SampleOnOutput:

SampleOnOutput is when the Sensor samples magnetic data within a short time period preceding the transmission of that data in the SENT frame. This provides the Host with a minimal latency between the data sample and its reception at the Host. The sensor uses SampleOnOutput in the following cases:

• An F_OUTPUT function is addressed to that sensor and no held data is present.
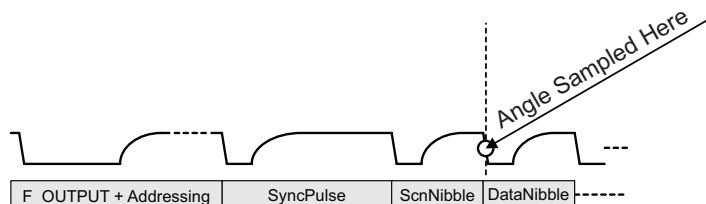

Figure 56: SampleOnOutput Example

SampleAndHold

SampleAndHold is when the Sensor samples magnetic data on the rising edge of a specific FunctionPulse and holds it for output in a SENT frame later in time, when addressed. This allows the data sampling from multiple sensors to be synchronized, with the tradeoff in latency. The sensor does a SampleAndHold of its magnetic data in the following cases:

• An F_SAMPLE function is broadcast, unless the sensor is configured with NO_FSAMPLE = 1.

• The Host initiates an F_OUTPUT function in SSENT mode, the SlotNumber is for Sensor ID 0, and the sensor is configured with ZERO_SAMPLE = 1.

Once the Sensor has data held from a SampleAndHold, it transmits it in the SENT frame the next time it is addressed. If the sensor is again polled before another SampleAndHold, then that Sensor will return the same data unless certain events intervene, in which case the SampleAndHold data is discarded. These events are:

• A diagnostic is executed that prevents the SENT interface from obtaining valid magnetic data from the sensors logic (CVH_SelfTest).

• The SENT interface is disabled, for instance the SENT line is taken over by the receipt of a Manchester Access Code.

If a sensor is polled and no SampleAndHold data is available (for instance, if the part comes online after a SampleAndHold has been issued), it will sample current data. It is not required that all Sensors on a shared bus be configured the same for sampling. This allows a subset of the Sensors on a shared bus to be synchronized for data sample, while others always perform Sample-OnOutput.
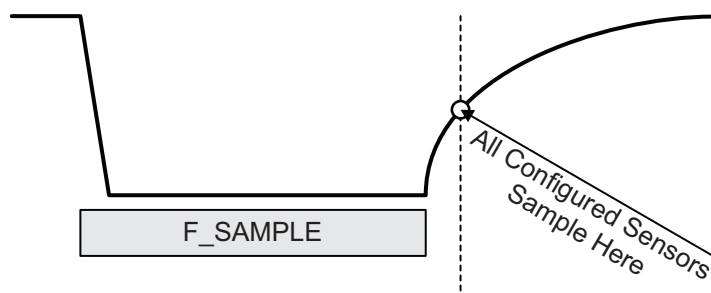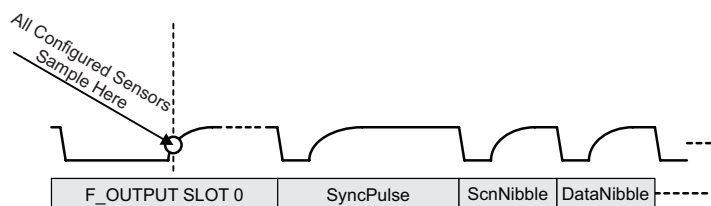
SENSOR STATES: OFFLINE, BUS SYNC, AND ONLINE

Figure 57: SampleAndHold (SSENT or ASENT)

Figure 58: SampleAndHold
SSENT with ZERO_SAMPLE = 1

Offline:

Offline is when the sensor is not actively interpreting the state of a shared SENT bus. In the Offline state, the Sensor will not drive the SENT bus. A Sensor is Offline:

- During Manchester.
- When unpowered, or after power-up.
- After a reset that would reset the SENT logic (POR).
- During CVH self test.
- After BusContention is detected (unless stated otherwise).

The Sensor exits Offline state into BusSync state once its SENT logic becomes functional, after it monitors the SENT bus long enough to flush any internal synchronization or filtering pipelines and sees the SENT bus high. This is necessary to guarantee that any subsequent low pulses are measured as their full duration.

Bus Sync:

BusSync is the state in which the Sensor determines to which Addressing Pulse it should respond. For ASENT, this state is unnecessary and it will immediately transition from Offline to Online. For SSENT, the Sensor will first monitor the SENT bus until it can synchronize its SlotCounter to the other Sensors on the bus before responding to any Addressing Pulses, but will always respond to Broadcast Pulses, even in the BusSync state.

A sensor configured for SSENT will set its SlotCounter and exit BusSync to Online when:

- The Host issues a F_SYNC pulse. The sensor immediately knows the next slot is for Sensor ID 0, and can then respond correctly.
- IDLE_SYNC is enabled and the bus is high (BusIdle) for at least a fixed (greater than 510 Ticks) period of time.
- POR_OFFLINE = 0, and the sensor exits power-on-reset.

Online:

In the Online state, the sensor is actively interpreting the shared bus, looking for and responding to Function Pulses. From Online, a sensor will go Offline when:

- It is powered down or reset.
- In response to a Manchester activation (F_AUX).
- It detects BusContention (SSENT mode).

SENT Message Frame Descriptions

The general format of a SENT message frame is shown in
Figure 41. The individual sections of a SENT message are
described in Table 28.

Table 28: SENT Message Frame Section Definitions

Section	Description
Synchronization and Calibration	
Function	Provide the external controller with a detectable start of the message frame. The large quantity of ticks distinguishes this section, for ease of distinction by the external controller.
Syntax	Tick count: 56
Status and Communication	
Function	Provides the external controller with the status of the A33003 and indicates the format and contents of the Data section.
Syntax	Nibbles: 1 Tick count: 12 to 27 Field width: 4 bits 1:0 Device status (indicates either a hard or soft error condition) 3:2 Message serial data protocol (set by SCN_MODE parameter)
Data	
Function	Provides the external controller with data selected by the SENT_DATA parameter.
Syntax	Nibbles: 3 to 6 Tick count: 12 to 27 (each nibble) Field width: 4 bits (each nibble)
CRC	
Function	Provides the external controller with cyclic redundancy check (CRC) data for certain error detection routines applied to the Data nibbles.
Syntax	Nibbles: 1 Tick count: 12 to 27 (each nibble) Field width: 4 bits
Pause Pulse	
Function	Additional time can be added at the end of a SENT message frame to synchronize each SENT message with the internal angle measurement updates, determined by the SENT_UPDATE parameter.
Syntax	Quantity of ticks: 12 tick minimum and 768 tick maximum (length determined by SENT_UPDATE option and by the individual structure of each SENT message. If a Pause pulse reaches 768 ticks, it restarts with a minimum length of 12 ticks) Quantity of bits: n/a

SENT Data Programming Parameters

Table 29: SCN_MODE (Register Address: 0x19, bits 6:4)

Function	Status and Communication Nibble Format Defines role of bits within the Status and Communication nibble																
Syntax	Field width: 3 bits																
Related Commands	–																
Values	SCN_MODE		Bit 3		Bit 2			Bit 1			Bit 0						
	000		0		0			Soft			Hard						
	001		SerialSync		SerialData			Soft			Hard						
	010		ID[1]		ID[0]			Soft			Hard						
	011		0		0			0			Soft+Hard						
	100		0		0			ID[1]			ID[0]						
	101		SerialSync		SerialData			ID[1]			ID[0]						
	110		Soft		Hard			ID[1]			ID[0]						
	111		SerialSync		SerialData			0			Soft+Hard						
Options	–																
Examples	The SerialSync and SerialData bits form a 16-bit message, transmitted over sixteen consecutive SENT frames. The message contents are arranged as shown below:																

SCN Bit	Nibble #															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SerialSync	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SerialData	Message ID				Data								CRC			

Short Serial Message

Table 30: SENT_DRIVER (Register Address: 0x1B, bits 6:4)

Function	Output Signal Configuration Sets configuration of the output signal slew-rate control. Sets the ramp rate on the gate of the output driver, thereby changing slew rate at the output.		
Syntax	Field width: 3 bits		
Related Commands	–		
Values	Code	Fall Time (80% to 20% Typical Values) (µs)	
		C_{LOAD} = 100 pF	C_{LOAD} = 1 nF
	000 (Default)	0.031	0.102
	001	0.075	0.105
	010	0.130	0.226
	011	0.180	0.296
	100	0.460	0.622
	101	0.930	1.100
	110	1.900	1.900
	111	2.900	2.700
Options	–		
Examples	–		

Table 31: DATA_MODE (Register Address: 0x19, bits 11:8)

Function	Data Nibble Format Quantity and contents of Data nibbles in message. (Does not relate to data contained in the Status and Communication nibble.)
Syntax	Field width: 4 bits
Related Commands	–
Values	0: Nibbles 1,2,3: Angle data (nibbles 4,5,6 skipped) 1: Nibbles 1,2,3: Angle Data Nibbles 4,5: Status bits, alternates between two 8-bit words 2: Nibbles 1,2,3: Angle Data Nibbles 4,5,6: Rotating Extended data (see Short Serial Output) 3: Nibbles 1,2,3: Angle Data Nibbles 4, 5, 6: Turns count data 4: Nibbles 1,2,3: Angle Data Nibbles 4, 5: Status bits. alternates between two 8-bit words Nibble 6: Alive counter 5: Nibbles 1,2,3: Angle Data Nibbles 4, 5: eight bit Alive counter Nibble 6: 1's complement of Nibble 1 6: Nibbles 1,2,3:, 4 Angle Data 7: Nibbles 1,2,3, 4: Angle Data Nibble 5: Status bits. Alternates between four 4-bit words. Nibble 6: Alive counter 8: Nibbles 1,2,3: Angle Data Nibble 4: Self-test and ID 9: Nibbles 1,2,3: Angle Data Nibbles 4, 5: Status bits, alternates between two 8-bits words. 10: Nibbles 1,2,3: Angle Data Nibbles 4,5: Rotating Extended data (see Short Serial Output) Nibble 6: Self-test and ID 11: Nibbles 1,2,3: Angle Data Nibbles 4, 5: 8-bit turns counter Nibble 6: Self-test and ID 12: Nibbles 1,2,3: Angle Data Nibbles 4, 5: Status bits, alternates between two 8-bit words. Nibble 6: Self-test and ID 13: Nibbles 1,2,3: Angle Data Nibble 4: alive counter Nibble 5: 1's complement of Nibble 1 Nibble 6: Self-test and ID 14: Nibbles 1,2,3, 4: Angle Data Nibble 5: Self-test and ID 15: Nibbles 1,2,3, 4: Angle Data Nibble 5: Alive counter Nibble 6: Self-test and ID
Options	–
Examples	–

Table 32: SENT_MODE (Register Address: 0x19, bits 14:12)

Function	Selects between the various SENT update rates. Also used to select various modes of triggerable SENT.
Syntax	Field width: 3 bits
Related Commands	–
Values	000: Disable, no SENT output. 001: No Pause pulse; new frame immediately follows previous frame. 010: SENT message frame synchronized to internal angle update rate. Pause pulse inserted to ensure each new SENT transmission corresponds to a fresh angle sample. 011: Triggered SENT mode (TSENT). Pause pulse held indefinitely until receipt of trigger pulse (OUT pulled low) from the controller, SENT message begins once output is released. Data latched near end of SCN. 100: Triggered SENT mode (TSENT). Pause pulse held indefinitely until receipt of trigger pulse (OUT pulled low) from the controller, SENT message begins once output is released. Data latched on falling edge of trigger. 101: Addressable SENT mode (ASENT). See Shared SENT section. 110: Sequential SENT mode (SSENT). See Shared SENT section. 111: Long SSENT. Supports alternative SENT line sharing protocol. See Shared SENT section.
Options	–
Examples	–

Table 33: SENT_TICK (Register Address: 0x19, bits 22:16)

Function	Tick Duration Sets the SENT Tick time: SENT_TICK/16 MHz = tick (µs)		
Syntax	Field width: 7 bits Any value from 0 to 127 can be used (although an internal limit of one clock period is forced)		
Related Commands	–		
Values	Code	Tick Time (µs)	Coefficient
	000 0000*	0.0625	1/16 (a minimum of one clock period is forced internally)
	000 0001*	0.0625	1/16
	000 0010*	0.125	2/16
	000 0011*	0.1875	3/16
	000 0100*	0.25	4/16
	000 1000	0.5	8/16
	001 0000	1	16/16
	001 1000	1.5	24/16
	011 0000	3	48/16
	110 0000	6	96/16
	111 1110	7.875	126/16
	111 1111	7.9375	127/16
Options	–		
Examples	–		

* Tick Times shorter than 0.5 µs are not guaranteed.

Table 34: CIS (Register Address: 0x19, bit 7)

Function	SENT CRC includes the Status and Communication Nibble (SCN)
Syntax	Field width: 1 bit
Related Commands	–
Values	0: SCN is not included in the CRC nibble. 1: SCN bits are covered via the CRC nibble (does not conform to the J2716 SENT standard)
Options	–
Examples	–

ASENT/SSENT SPECIFIC FIELDS

Table 35: MAXID (Register Address: 0x19, bits 25:24)

Function	Specifies highest sensor ID number on the shared SENT bus
Syntax	Field width: 2 bits
Related Commands	–
Values	00: Highest ID value is 0. Sensor is not sharing the SENT line 01: Highest ID value is 1. Two sensors are sharing the SENT line 10: Highest ID value is 2. Three sensors are sharing the SENT line 11: Highest ID value is 3. Four sensors are sharing the SENT line
Options	–
Examples	–

Table 36: NS (Register Address: 0x19, bit 3)

Function	No Sample. Sensor does not sample angle on receipt of an F_SAMPLE pulse	
Syntax	Field width: 1 bit	
Related Commands	–	
Values	0:	On receipt of an F_SAMPLE pulse, sensor samples and holds angle data
	1:	Sensor does not sample and hold data on receipt of an F_SAMPLE pulse
Options	–	
Examples	–	

Table 37: FA (Register Address: 0x19, bit 0)

Function	F_SAMPLE addressing. Sensor treats the F_SAMPLE pulse as an addressing pulse	
Syntax	Field width: 1 bit	
Related Commands	–	
Values	0:	F_SAMPLE is treated as a broadcast pulse. Sensor will sample and hold angle data on any F_SAMPLE pulse (unless NS = 1)
	1:	F_SAMPLE is treated as an addressing pulse. Sensor will only sample and hold angle data on an F_SAMPLE pulse if properly addressed (unless NS = 1)
Options	–	
Examples	–	

SSENT SPECIFIC FIELDS

Table 38: IS (Register Address: 0x1B, bit 8)

Function	IDLE_SYNC. Sensor resets slot counter if SENT bus idle for more than 510 Ticks (SSENT only).	
Syntax	Field width: 1 bit	
Related Commands	–	
Values	0:	Sensor takes no action for an idle SENT line
	1:	If SENT line is idle for greater than 510 Ticks, internal slot counter is reset to 0. All sensors sharing a SENT line should have matching IS settings
Options	–	
Examples	–	

Table 39: PO (Register Address: 0x1B, bit 7)

Function	POR_OFFLINE. Sensor stays offline after power on reset (SSENT only).	
Syntax	Field width: 1 bit	
Related Commands	–	
Values	0:	After a power-on-reset sensor will go online with a slot counter of 0
	1:	Sensor stays offline following a power-on-reset. Sensor goes online after slot counter synchronization via an F_SYNC pulse or IDLE_SYNC
Options	–	
Examples	–	

Table 40: SM (Register Address: 0x19, bit 15)

Function	SLOT_MARKING enable (SSENT only).
Syntax	Field width: 1 bit
Related Commands	–
Values	0: No Slot marking pulses 1: Sensor will output a bus high delay after an addressing pulse, based on sensor ID
Options	–
Examples	–

Table 41: ZS (Register Address: 0x19, bit 2)

Function	ZERO_SAMPLING. Sensor samples and holds data at Slot 0 (SSENT only)
Syntax	Field width: 1 bit
Related Commands	–
Values	0: No special action at slot = 0 1: Sensor performs a sample and hold when its slot counter resets to 0
Options	–
Examples	–

Table 42: FP_ADJ (Register Address: 0x1B, bits 25:24)

Function	Function Pulse Adjust. Only for Long SSENT (SENT_MODE = 7). Increases the lower threshold of F_OUTPUT pulse by 0-3 Ticks. Reduces possible misinterpretation of F_OUTPUT pulses at sub-1.5 µs Tick times
Syntax	Field width: 2 bits
Related Commands	–
Values	00: No Change to F_OUTPUT pulse width. Minimum width = 9 Ticks 01: Minimum width of F_OUTPUT increased by 1 Tick. Min = 10 Ticks 10: Minimum width of F_OUTPUT increased by 2 Ticks. Min = 11 Ticks 11: Minimum width of F_OUTPUT increased by 3 Ticks. Min = 12 Ticks
Options	–
Examples	–

APPENDIX B: ANGLE ERROR AND DRIFT DEFINITION

Angle error is the difference between the actual positon of the magnet and the position of the magnet as measured by the angle sensor IC (without noise). This measurement is done by reading the angle sensor IC output and comparing it with a high resolution encoder. Refer to the figure below.
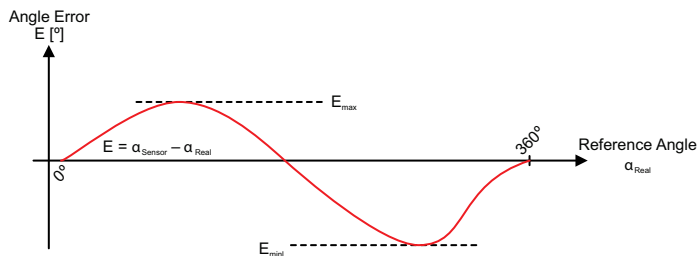

Figure 59: Angle Error Definition

Angle Error Definition

Throughout this document, the term "angle error" is used extensively. Thus, it is necessary to introduce a single angle error definition for a full magnetic rotation. The term "angle error" is calculated according to the following formula:

$$AngleError = max(\, |E_{max}| \, , \, |E_{min}| \,)$$

In other words, it is the maximum deviation from a perfect straight line between 0 and 360 degrees. For the purpose of a generic definition, the offset of the IC angle profile is removed prior to the error calculation, as seen in Figure 59. The offset itself will depend on the starting IC angle position relative to the encoder 0° and thus can differ anywhere from 0–360°.

Angle Drift

Angle drift is the change in the observed angular position over temperature, relative to 25°C.

During Allegro's factory trim, drift is measured at 150°C. The value is calculated using the following formula:

$$Angle_{Drift} = Angle_{25°C} - Angle_{150°C}$$

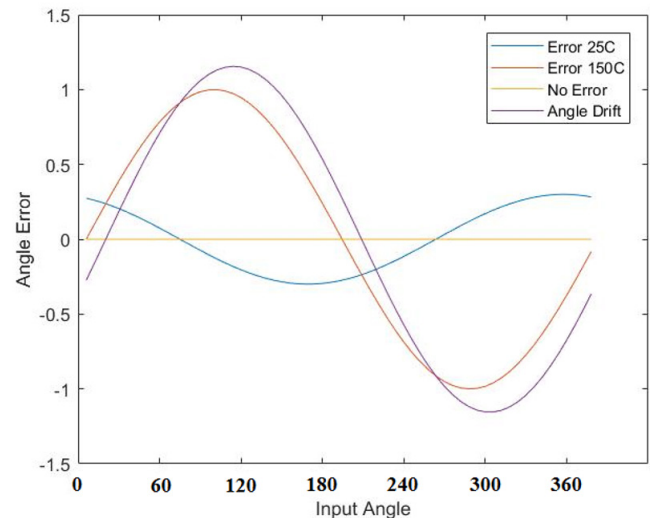where each Angle value is an array corresponding to 16 angular positions around a circle.

Figure 60: Angle Drift of 150°C in Reference to 25°C [1][2]

[1] Note that the data above is simply a representation of angle drift and not real data.

[2] Note the error at 25°C and 150°C are often out of phase. This can cause a drift larger than the maximum error specification of the part, as seen above.

REVISION HISTORY

Number	Date	Description
–	September 30, 2019	Initial release
1	November 22, 2019	Added footnote to Selection Guide table (page 2); updated footnote 4 (page 10)
2	October 6, 2020	Updated Interrupt Pulse Hold Time values (page 7); changed PWI to PWS (pages 23, 27, 50); corrected package drawing Hall element labels (page 62); updated Hard Error Flag and Soft Error Flag descriptions (page A-3); updated Sent Output Mode table (page A-12), tables 24-26 (page A-14); added Sensor Measurement Range section (page A-14).
3	October 14, 2020	Added footnote to Figure 3 (page 5); updated SEN.SENT_MODE description (page 53) and FWS.FP_ADJ description (page 56).
4	January 13, 2021	Updated ASIL status (page 1), Selection Guide (page 2), Bypass Pin Output Voltage (page 6), footnote 1 (page 9), Linearization section (pages 17-18), Package Drawing reference numbers (pages 62-63), Figure 46 (page A-11); added CRC section (page 27).
5	April 20, 2021	Updated "ISO 26262:2011" to "ISO 26262" (page 1), Features and Benefits (page 1-2), Angle Measurement section (page 13), Table 10 (page 32), Figure 29 (page 29), Figure 32 (page 31), and SENT Output Mode table (page A-12)

For the latest version of this document, visit our website:
www.allegromicro.com