S-5724 Series

www.ablic.com

LOW VOLTAGE OPERATION HIGH-SPEED BIPOLAR HALL EFFECT LATCH IC

© ABLIC Inc., 2012-2021

Rev.1.3_00

The S-5724 Series, developed by CMOS technology, is a high-accuracy hall effect latch IC that operates at a low voltage with a high-sensitivity, a high-speed detection and low current consumption.
The output voltage changes when the S-5724 Series detects the intensity level of magnetic flux density and a polarity change. Using the S-5724 Series with a magnet makes it possible to detect the rotation status in various devices.
High-density mounting is possible by using the small SOT-23-3 or the super-small SNT-4A packages.
Due to its high-accuracy magnetic characteristics, the S-5724 Series can make operation's dispersion in the system combined with magnet smaller.

Caution **This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, it is imperative to contact our sales representatives.**

■ Features

- Pole detection: Bipolar latch
- Output logic*1: V_{OUT} = "L" at S pole detection
  V_{OUT} = "H" at S pole detection
- Output form*1: Nch open-drain output, CMOS output
- Magnetic sensitivity: B_{OP} = 3.0 mT typ.
- Operating cycle (current consumption)*1: t_{CYCLE} = 50 µs (I_{DD} = 640.0 µA) typ.
  t_{CYCLE} = 1.25 ms (I_{DD} = 26.0 µA) typ.
  t_{CYCLE} = 6.05 ms (I_{DD} = 6.0 µA) typ.
- Power supply voltage range: V_{DD} = 1.6 V to 3.5 V
- Operation temperature range: Ta = –40°C to +85°C
- Built-in power-down circuit: Extends battery life (only SNT-4A)
- Lead-free (Sn 100%), halogen-free

***1.** The option can be selected.

■ Applications

- Digital still camera
- Plaything, portable game
- Home appliance

■ Packages

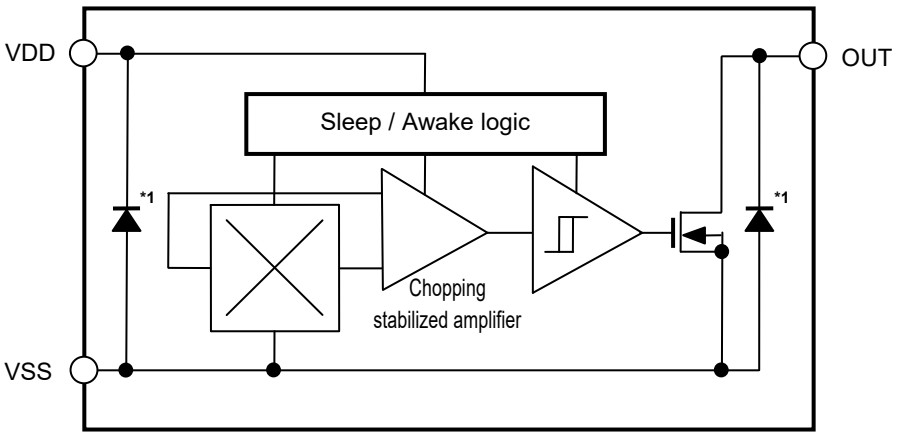
- SOT-23-3
- SNT-4A

Downloaded from Arrow.com.

■ Block Diagrams

1. Nch open-drain output product

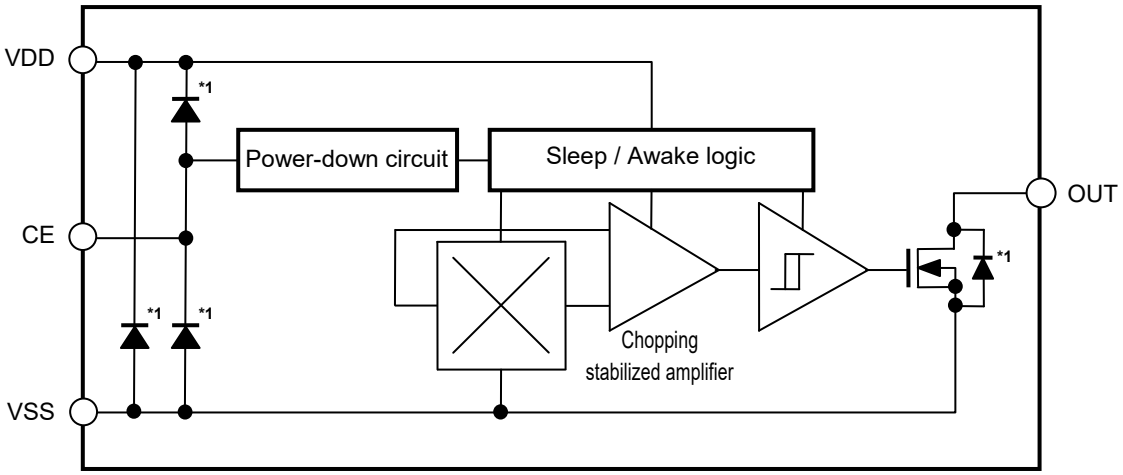
1. 1 Product without power-down function



***1.** Parasitic diode

Figure 1

1. 2 Product with power-down function (SNT-4A)



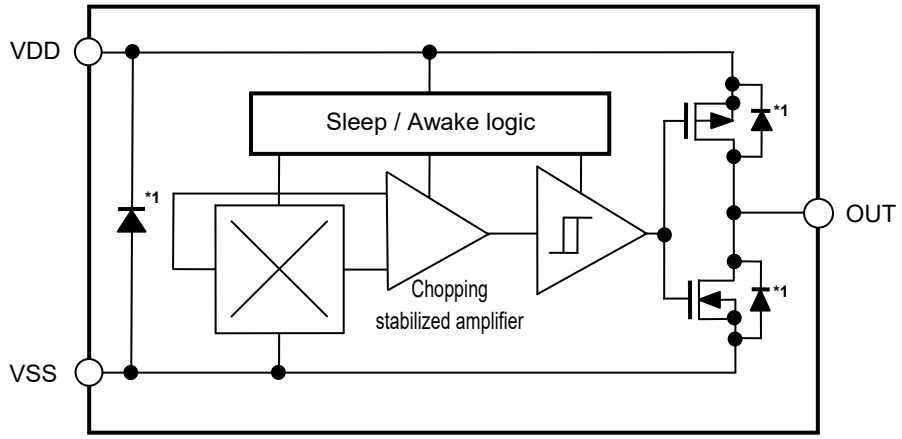
***1.** Parasitic diode

Figure 2

Downloaded from Arrow.com.

2. CMOS output product

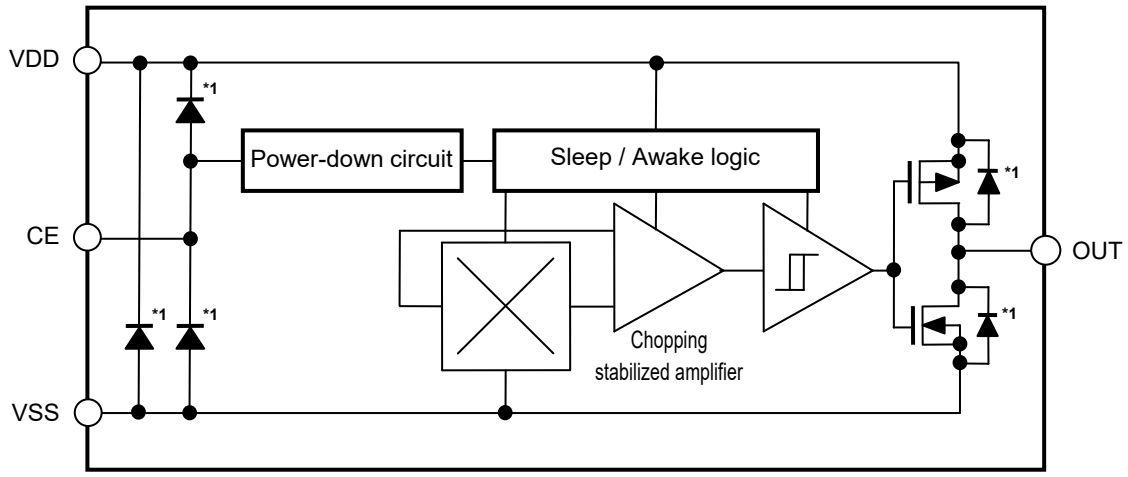
2. 1 Product without power-down function



***1.** Parasitic diode

Figure 3

2. 2 Product with power-down function (SNT-4A)



***1.** Parasitic diode

Figure 4

Downloaded from Arrow.com.

■ Product Name Structure

1. Product name

S-5724 x x B x 1 - xxxx U

Environmental code
- U: Lead-free (Sn 100%), halogen-free

Package name (abbreviation) and packing specifications*1
- M3T1: SOT-23-3, Tape
- I4T1: SNT-4A, Tape

Magnetic sensitivity
- 1: B_{OP} = 3.0 mT typ.

Output logic
- L: V_{OUT} = "L" at S pole detection
- H: V_{OUT} = "H" at S pole detection

Pole detection
- B: Bipolar latch

Output form
- N: Nch open-drain output
- C: CMOS output

Operating cycle
- C: t_{CYCLE} = 6.05 ms typ. (Without power-down function)
- D: t_{CYCLE} = 1.25 ms typ. (Without power-down function)
- E: t_{CYCLE} = 50 µs typ. (Without power-down function)
- H: t_{CYCLE} = 6.05 ms typ. (With power-down function, SNT-4A)
- I: t_{CYCLE} = 1.25 ms typ. (With power-down function, SNT-4A)
- J: t_{CYCLE} = 50 µs typ. (With power-down function, SNT-4A)

***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-3	MP003-C-P-SD	MP003-C-C-SD	MP003-Z-R-SD	–
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	PF004-A-L-SD

Downloaded from Arrow.com.

3. Product name list

3. 1 SOT-23-3

3. 1. 1 Nch open-drain output product

Table 2

Product Name	Operating Cycle (t_{CYCLE})	Power-down Function	Output Form	Pole Detection	Output logic	Magnetic Sensitivity (B_{OP})
S-5724CNBL1-M3T1U	6.05 ms typ.	Unavailable	Nch open-drain output	Bipolar latch	V_{OUT} = "L" at S pole detection	3.0 mT typ.
S-5724DNBL1-M3T1U	1.25 ms typ.	Unavailable	Nch open-drain output	Bipolar latch	V_{OUT} = "L" at S pole detection	3.0 mT typ.
S-5724ENBL1-M3T1U	50 μs typ.	Unavailable	Nch open-drain output	Bipolar latch	V_{OUT} = "L" at S pole detection	3.0 mT typ.

Remark Please contact our sales representatives for products other than the above.

3. 1. 2 CMOS output product

Table 3

Product Name	Operating Cycle (t_{CYCLE})	Power-down Function	Output Form	Pole Detection	Output logic	Magnetic Sensitivity (B_{OP})
S-5724CCBL1-M3T1U	6.05 ms typ.	Unavailable	CMOS output	Bipolar latch	V_{OUT} = "L" at S pole detection	3.0 mT typ.
S-5724DCBL1-M3T1U	1.25 ms typ.	Unavailable	CMOS output	Bipolar latch	V_{OUT} = "L" at S pole detection	3.0 mT typ.
S-5724ECBL1-M3T1U	50 μs typ.	Unavailable	CMOS output	Bipolar latch	V_{OUT} = "L" at S pole detection	3.0 mT typ.

Remark Please contact our sales representatives for products other than the above.

3. 2 SNT-4A

3. 2. 1 Nch open-drain output product

Table 4

Product Name	Operating Cycle (t_{CYCLE})	Power-down Function	Output Form	Pole Detection	Output logic	Magnetic Sensitivity (B_{OP})
S-5724INBL1-I4T1U	1.25 ms typ.	Available	Nch open-drain output	Bipolar latch	V_{OUT} = "L" at S pole detection	3.0 mT typ.

Remark Please contact our sales representatives for products other than the above.

3. 2. 2 CMOS output product

Table 5

Product Name	Operating Cycle (t_{CYCLE})	Power-down Function	Output Form	Pole Detection	Output logic	Magnetic Sensitivity (B_{OP})
S-5724HCBL1-I4T1U	6.05 ms typ.	Available	CMOS output	Bipolar latch	V_{OUT} = "L" at S pole detection	3.0 mT typ.
S-5724HCBH1-I4T1U	6.05 ms typ.	Available	CMOS output	Bipolar latch	V_{OUT} = "H" at S pole detection	3.0 mT typ.
S-5724ICBL1-I4T1U	1.25 ms typ.	Available	CMOS output	Bipolar latch	V_{OUT} = "L" at S pole detection	3.0 mT typ.
S-5724ICBH1-I4T1U	1.25 ms typ.	Available	CMOS output	Bipolar latch	V_{OUT} = "H" at S pole detection	3.0 mT typ.
S-5724JCBL1-I4T1U	50 μs typ.	Available	CMOS output	Bipolar latch	V_{OUT} = "L" at S pole detection	3.0 mT typ.
S-5724JCBH1-I4T1U	50 μs typ.	Available	CMOS output	Bipolar latch	V_{OUT} = "H" at S pole detection	3.0 mT typ.

Remark Please contact our sales representatives for products other than the above.

Downloaded from Arrow.com.

■ Pin Configurations

1. SOT-23-3

Top view

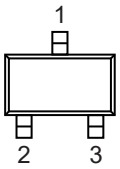


Figure 5

Table 6

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Power supply pin
3	OUT	Output pin

2. SNT-4A

Top view

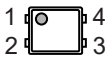


Figure 6

Table 7

Pin No.	Symbol	Description
1	VDD	Power supply pin
2	VSS	GND pin
3	CE	Enabling pin "H": Enables operation "L": Power-down
4	OUT	Output pin

Downloaded from Arrow.com.

■ Absolute Maximum Ratings

Table 8

(Ta = +25°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD}	V_{SS} – 0.3 to V_{SS} + 7.0	V
Input voltage		V_{CE}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output current		I_{OUT}	±1.0	mA
Output voltage	Nch open-drain output product	V_{OUT}	V_{SS} – 0.3 to V_{SS} + 7.0	V
	CMOS output product		V_{SS} – 0.3 to V_{DD} + 0.3	V
Power dissipation	SOT-23-3	P_D	430*1	mW
	SNT-4A		300*1	mW
Operation ambient temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

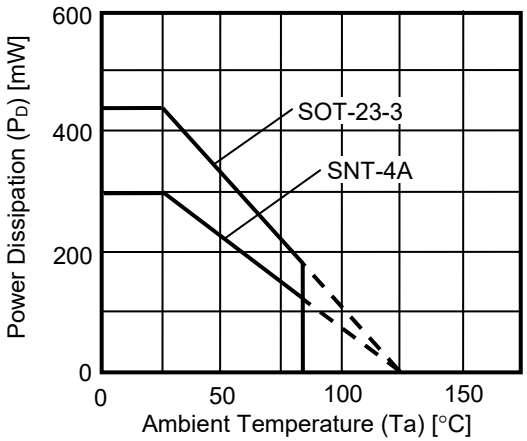


Figure 7 Power Dissipation of Package (When Mounted on Board)

Downloaded from Arrow.com.

■ Electrical Characteristics

1. Product without power-down function

1. 1 S-5724CxBxx

Table 9

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	6.0	11.0	µA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 3.5 V		–	–	1	µA	4
Awake mode time	t_{AW}	–		–	0.05	–	ms	–
Sleep mode time	t_{SL}	–		–	6.00	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	6.05	12.00	ms	–

1. 2 S-5724DxBxx

Table 10

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	26.0	45.0	µA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 3.5 V		–	–	1	µA	4
Awake mode time	t_{AW}	–		–	0.05	–	ms	–
Sleep mode time	t_{SL}	–		–	1.20	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	1.25	2.50	ms	–

Downloaded from Arrow.com.

1. 3 S-5724ExBxx

Table 11

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	640.0	1000.0	µA	1
Output voltage	V_{OUT}	Nch open-drain output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 3.5 V		–	–	1	µA	4
Awake mode time	t_{AW}	–		–	50	–	µs	–
Sleep mode time	t_{SL}	–		–	0	–	µs	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	50	100	µs	–

Downloaded from Arrow.com.

2. Product with power-down function (SNT-4A)

2. 1 S-5724HxBxx

Table 12

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	6.0	11.0	µA	1
Current consumption during power-down	I_{DD2}	V_{CE} = V_{SS}		–	–	1	µA	6
Output voltage	V_{OUT}	Nch open-drain outputproduct	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 3.5 V		–	–	1	µA	4
Awake mode time	t_{AW}	–		–	0.05	–	ms	–
Sleep mode time	t_{SL}	–		–	6.00	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	6.05	12.00	ms	–
Enabling pin input voltage "L"	V_{CEL}	–		–	–	V_{DD} × 0.3	V	–
Enabling pin input voltage "H"	V_{CEH}	–		V_{DD} × 0.7	–	–	V	–
Enabling pin input current "L"	I_{CEL}	V_{DD} = 1.85 V, V_{CE} = 0 V		–1	–	1	µA	7
Enabling pin input current "H"	I_{CEH}	V_{DD} = 1.85 V, V_{CE} = 1.85 V		–1	–	1	µA	8
Power-down transition time	t_{OFF}	–		–	–	100	µs	–
Enable transition time	t_{ON}	–		–	–	100	µs	–
Output logic update time after inputting "H" to enabling pin	t_{OE}	–		–	–	200	µs	–

Downloaded from Arrow.com.

2. 2 S-5724IxBxx

Table 13

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	26.0	45.0	µA	1
Current consumption during power-down	I_{DD2}	V_{CE} = V_{SS}		–	–	1	µA	6
Output voltage	V_{OUT}	Nch open-drain outputproduct	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 3.5 V		–	–	1	µA	4
Awake mode time	t_{AW}	–		–	0.05	–	ms	–
Sleep mode time	t_{SL}	–		–	1.20	–	ms	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	1.25	2.50	ms	–
Enabling pin input voltage "L"	V_{CEL}	–		–	–	V_{DD} × 0.3	V	–
Enabling pin input voltage "H"	V_{CEH}	–		V_{DD} × 0.7	–	–	V	–
Enabling pin input current "L"	I_{CEL}	V_{DD} = 1.85 V, V_{CE} = 0 V		–1	–	1	µA	7
Enabling pin input current "H"	I_{CEH}	V_{DD} = 1.85 V, V_{CE} = 1.85 V		–1	–	1	µA	8
Power-down transition time	t_{OFF}	–		–	–	100	µs	–
Enable transition time	t_{ON}	–		–	–	100	µs	–
Output logic update time after inputting "H" to enabling pin	t_{OE}	–		–	–	200	µs	–

Downloaded from Arrow.com.

2. 3 S-5724JxBxx

Table 14

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–		1.60	1.85	3.50	V	–
Current consumption	I_{DD}	Average value		–	640.0	1000.0	µA	1
Current consumption during power-down	I_{DD2}	V_{CE} = V_{SS}		–	–	1	µA	6
Output voltage	V_{OUT}	Nch open-drain outputproduct	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I_{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I_{OUT} = –0.5 mA	V_{DD} – 0.4	–	–	V	3
Leakage current	I_{LEAK}	Nch open-drain output product Output transistor Nch, V_{OUT} = 3.5 V		–	–	1	µA	4
Awake mode time	t_{AW}	–		–	50	–	µs	–
Sleep mode time	t_{SL}	–		–	0	–	µs	–
Operating cycle	t_{CYCLE}	t_{AW} + t_{SL}		–	50	100	µs	–
Enabling pin input voltage "L"	V_{CEL}	–		–	–	V_{DD} × 0.3	V	–
Enabling pin input voltage "H"	V_{CEH}	–		V_{DD} × 0.7	–	–	V	–
Enabling pin input current "L"	I_{CEL}	V_{DD} = 1.85 V, V_{CE} = 0 V		–1	–	1	µA	7
Enabling pin input current "H"	I_{CEH}	V_{DD} = 1.85 V, V_{CE} = 1.85 V		–1	–	1	µA	8
Power-down transition time	t_{OFF}	–		–	–	100	µs	–
Enable transition time	t_{ON}	–		–	–	100	µs	–
Output logic update time after inputting "H" to enabling pin	t_{OE}	–		–	–	200	µs	–

Downloaded from Arrow.com.

■ Magnetic Characteristics

Table 15

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OP}	–	1.4	3.0	4.0	mT	5
Release point*2	N pole	B_{RP}	–	–4.0	–3.0	–1.4	mT	5
Hysteresis width*3		B_{HYS}	$B_{HYS} = B_{OP} - B_{RP}$	–	6.0	–	mT	5

***1.** B_{OP}: Operation point
B_{OP} is the value of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to the S-5724 Series by the magnet (S pole) is increased (by moving the magnet closer).
V_{OUT} retains the status until a magnetic flux density of the N pole higher than B_{RP} is applied.

***2.** B_{RP}: Release point
B_{RP} is the value of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to the S-5724 Series by the magnet (N pole) is increased (by moving the magnet closer).
V_{OUT} retains the status until a magnetic flux density of the S pole higher than B_{OP} is applied.

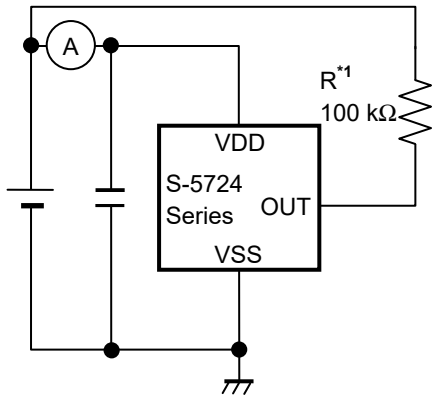
***3.** B_{HYS}: Hysteresis width
B_{HYS} is the difference between B_{OP} and B_{RP}.

Remark The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

Downloaded from Arrow.com.

■ Test Circuits

1. Product without power-down function



*1. Resistor (R) is unnecessary for the CMOS output product.

Figure 8 Test Circuit 1

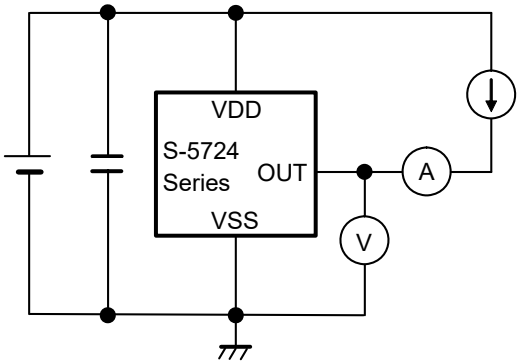


Figure 9 Test Circuit 2

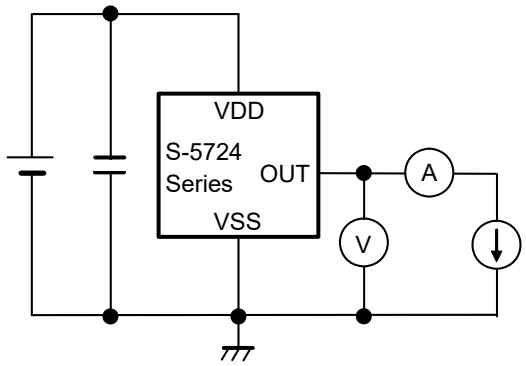


Figure 10 Test Circuit 3

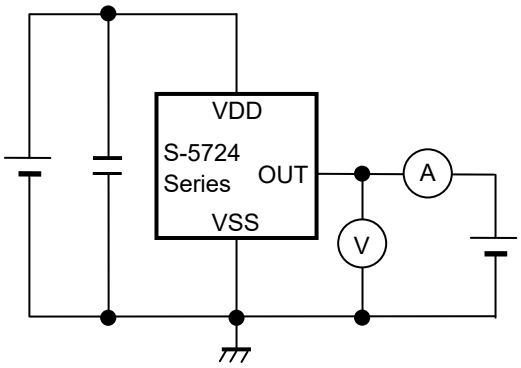
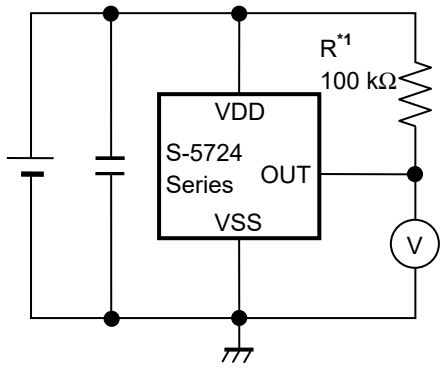


Figure 11 Test Circuit 4

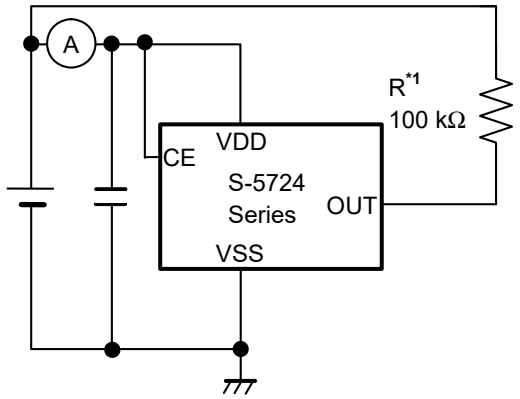


*1. Resistor (R) is unnecessary for the CMOS output product.

Figure 12 Test Circuit 5

Downloaded from Arrow.com.

2. Product with power-down function (SNT-4A)



*1. Resistor (R) is unnecessary for the CMOS output product.

Figure 13 Test Circuit 1

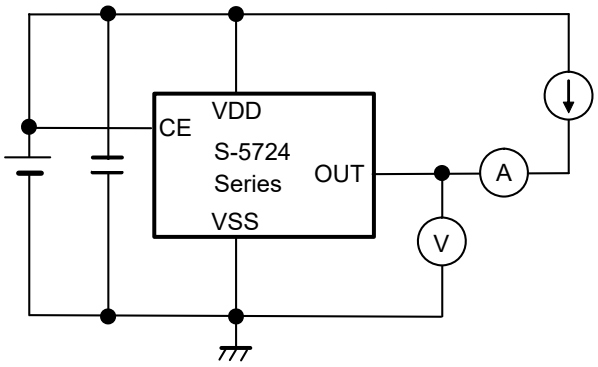


Figure 14 Test Circuit 2

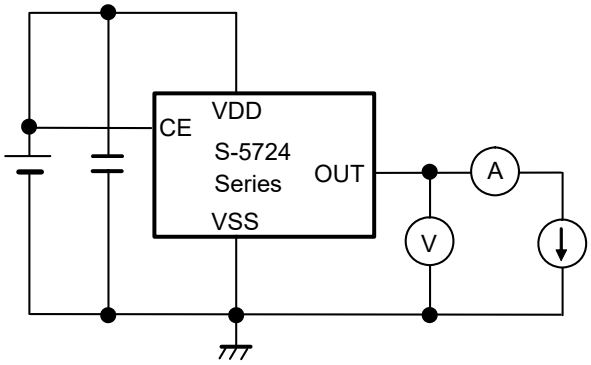


Figure 15 Test Circuit 3

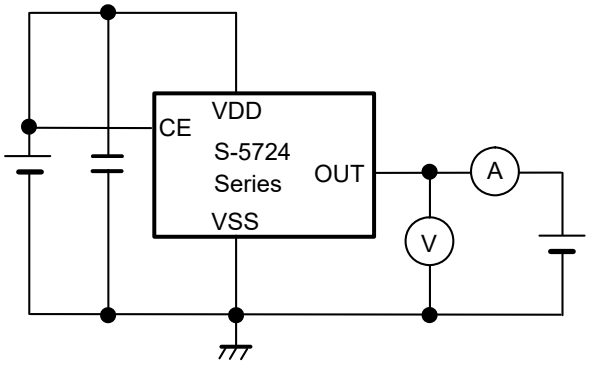
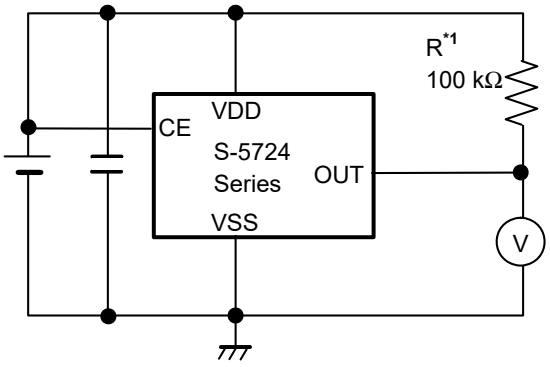
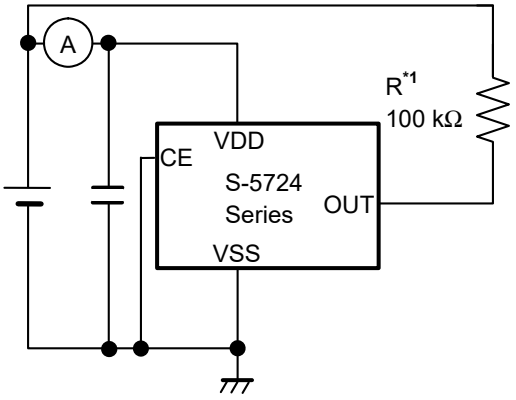


Figure 16 Test Circuit 4



*1. Resistor (R) is unnecessary for the CMOS output product.

Figure 17 Test Circuit 5



*1. Resistor (R) is unnecessary for the CMOS output product.

Figure 18 Test Circuit 6

Downloaded from Arrow.com.

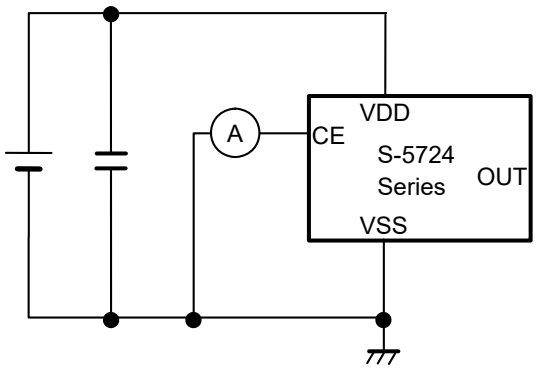


Figure 19 Test Circuit 7

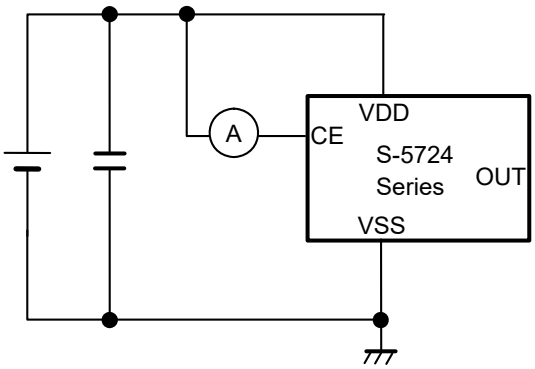
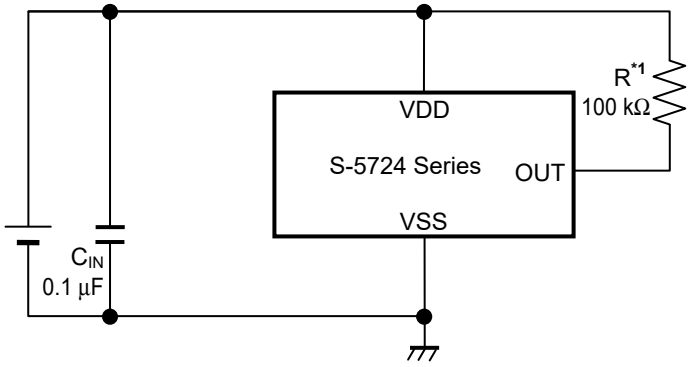


Figure 20 Test Circuit 8

Downloaded from Arrow.com.

■ Standard Circuits

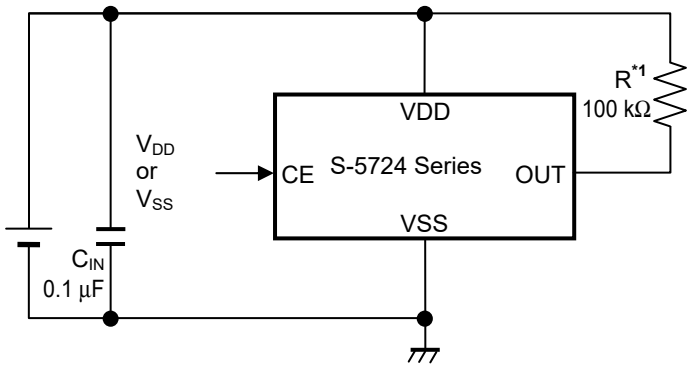
1. Product without power-down function



***1.** Resistor (R) is unnecessary for the CMOS output product.

Figure 21

2. Product with power-down function (SNT-4A)



***1.** Resistor (R) is unnecessary for the CMOS output product.

Figure 22

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

Downloaded from Arrow.com.

■ Operation

1. Direction of applied magnetic flux

The S-5724 Series detects the magnetic flux density which is vertical to the marking surface.
Figure 23 and **Figure 24** show the direction in which magnetic flux is being applied.

1. 1 SOT-23-3

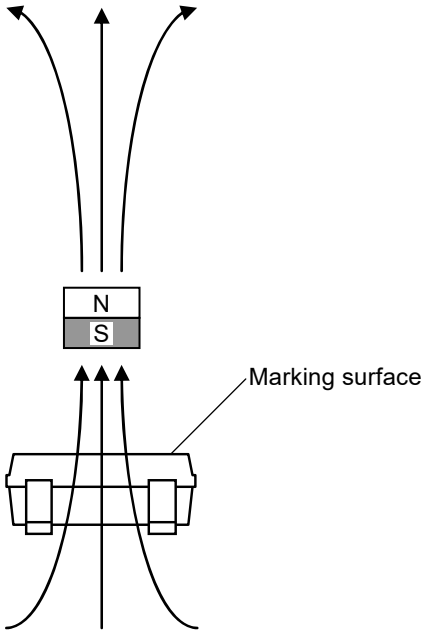


Figure 23

1. 2 SNT-4A

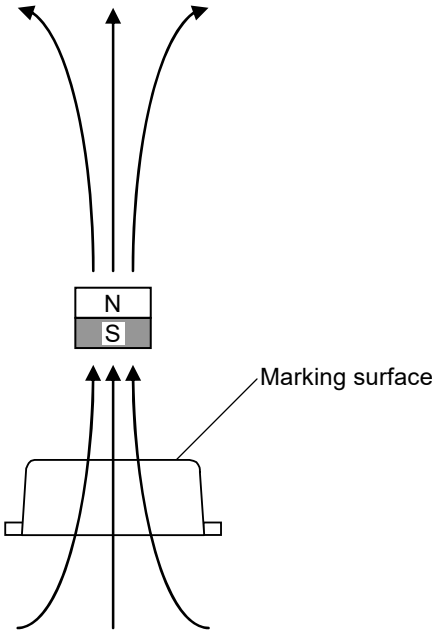


Figure 24

2. Position of Hall sensor

Figure 25 and **Figure 26** show the position of Hall sensor.
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

2. 1 SOT-23-3

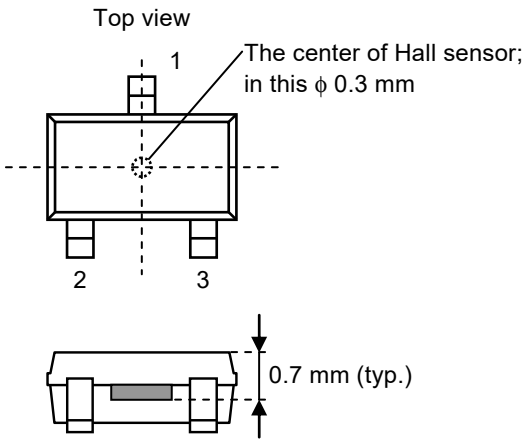


Figure 25

2. 2 SNT-4A

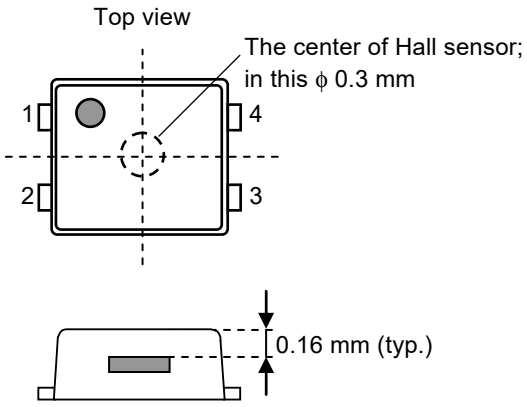


Figure 26

Downloaded from Arrow.com.

3. Basic operation

The S-5724 Series changes the output voltage (V_{OUT}) according to the level of the magnetic flux density and a polarity change (N pole or S pole) applied by a magnet.
Definition of the magnetic field is performed every operating cycle indicated in "■ **Electrical Characteristics**".

3. 1 Product with V_{OUT} = "L" at S pole detection

When the magnetic flux density of the S pole perpendicular to the marking surface exceeds the operation point (B_{OP}) after the S pole of a magnet is moved closer to the marking surface of the S-5724 Series, V_{OUT} changes from "H" to "L". When the N pole of a magnet is moved closer to the marking surface of the S-5724 Series and the magnetic flux density of the N pole is higher than the release point (B_{RP}), V_{OUT} changes from "L" to "H". In case of $B_{RP} < B < B_{OP}$, V_{OUT} retains the status.
Figure 27 shows the relationship between the magnetic flux density and V_{OUT}.

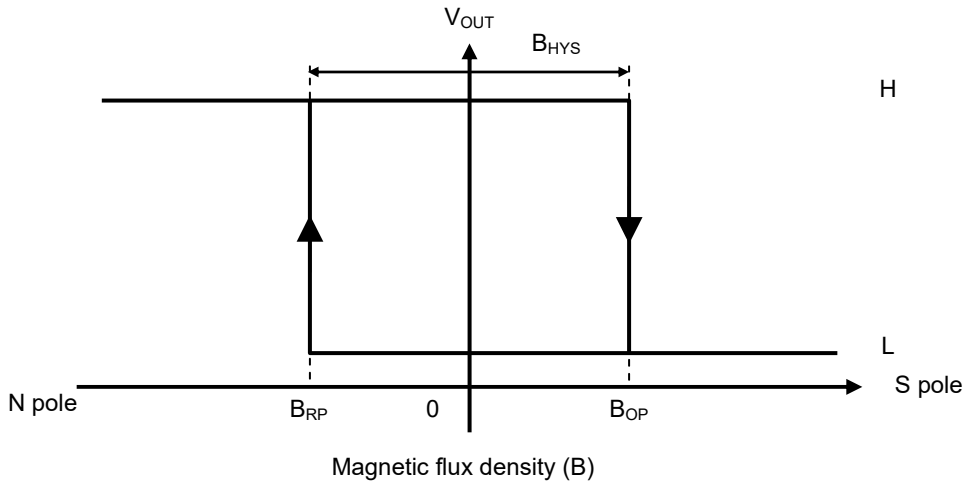


Figure 27

3. 2 Product with V_{OUT} = "H" at S pole detection

When the magnetic flux density of the S pole perpendicular to the marking surface exceeds B_{OP} after the S pole of a magnet is moved closer to the marking surface of the S-5724 Series, V_{OUT} changes from "L" to "H". When the N pole of a magnet is moved closer to the marking surface of the S-5724 Series and the magnetic flux density of the N pole is higher than B_{RP}, V_{OUT} changes from "H" to "L". In case of $B_{RP} < B < B_{OP}$, V_{OUT} retains the status.
Figure 28 shows the relationship between the magnetic flux density and V_{OUT}.

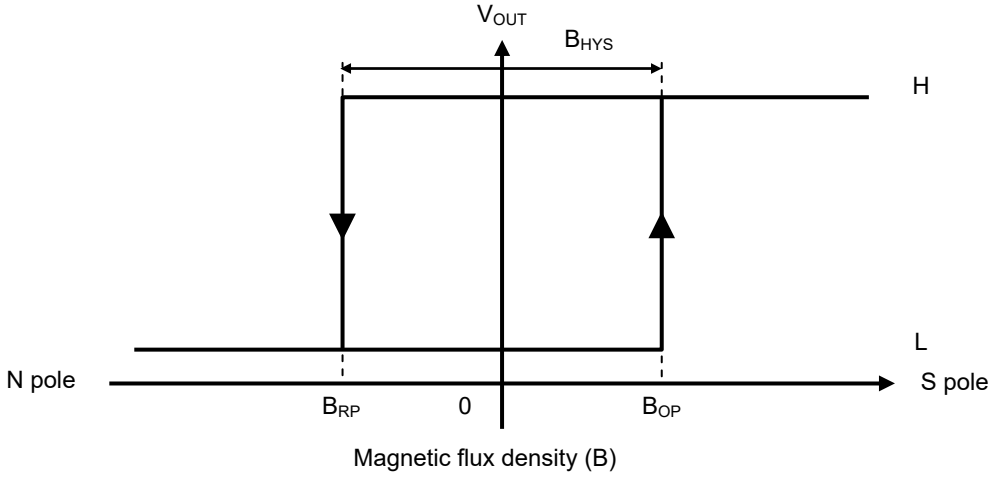


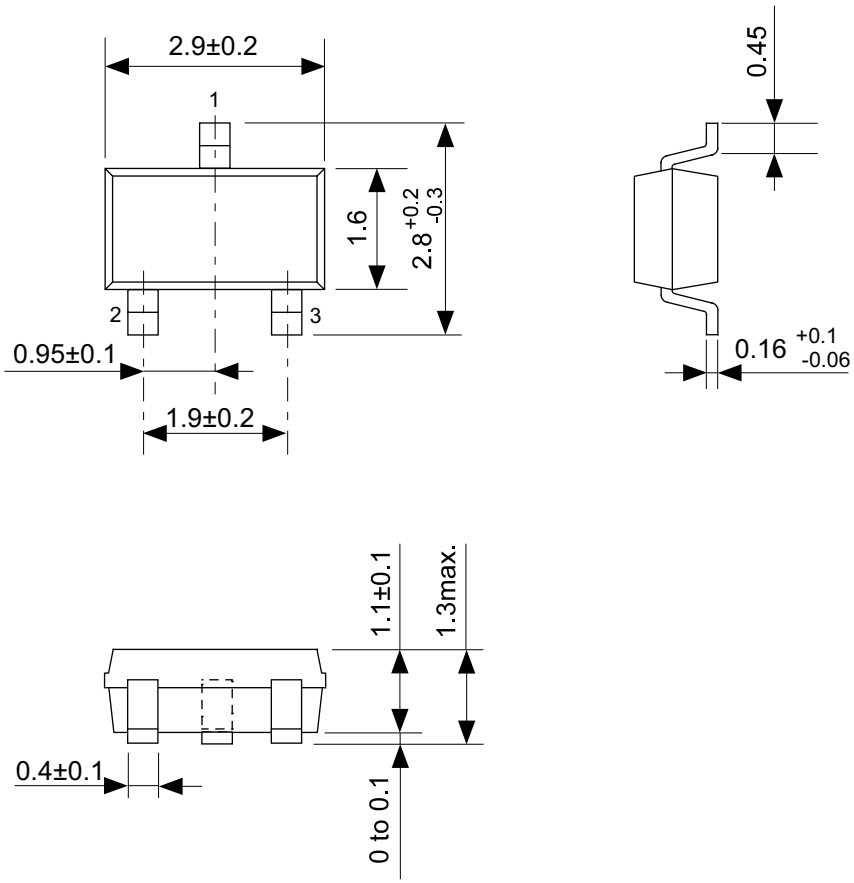
Figure 28

Downloaded from Arrow.com.

■ Precautions

- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by bend and distortion during mounting the IC on a board or handle after mounting.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

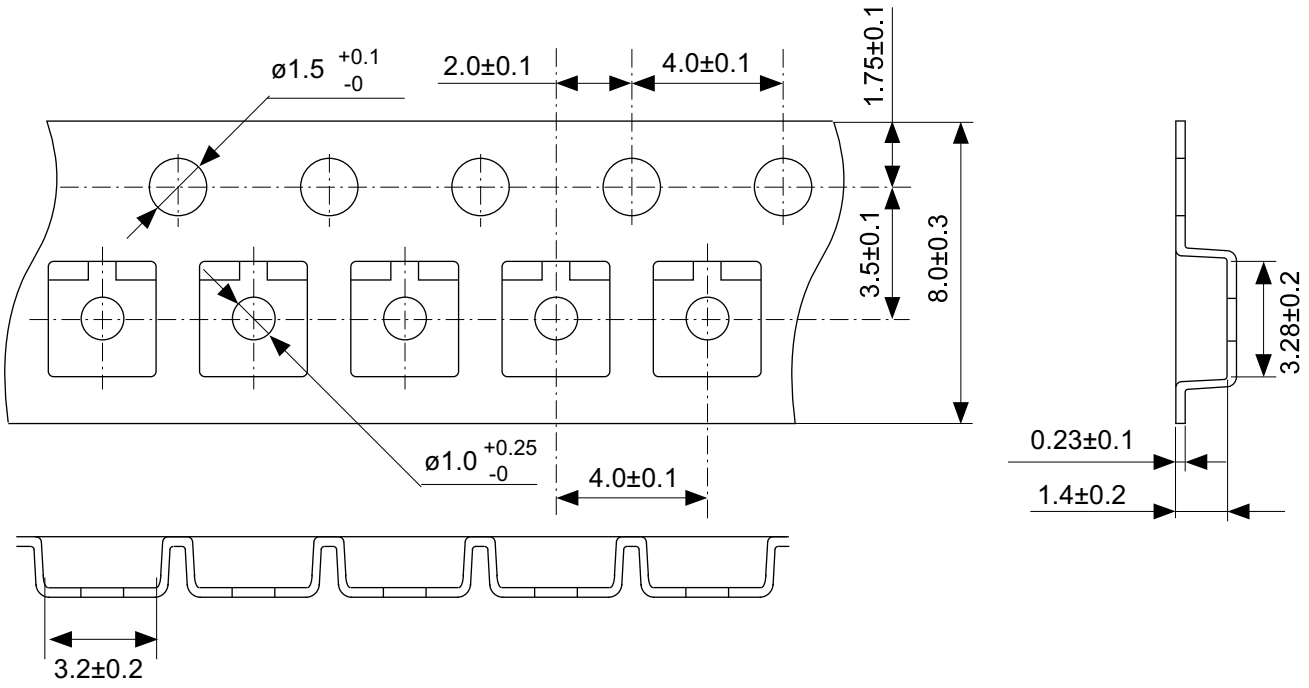
Downloaded from Arrow.com.

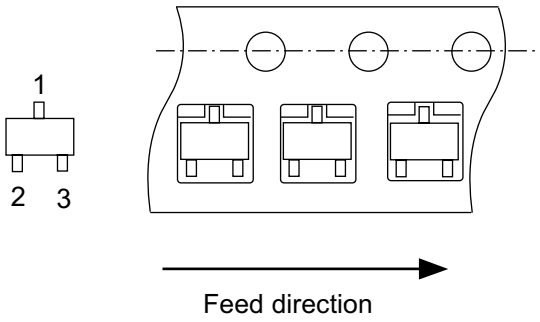


No. MP003-C-P-SD-1.1

TITLE	SOT233-C-PKG Dimensions
No.	MP003-C-P-SD-1.1
ANGLE	
UNIT	mm
ABLIC Inc.	

Downloaded from Arrow.com.

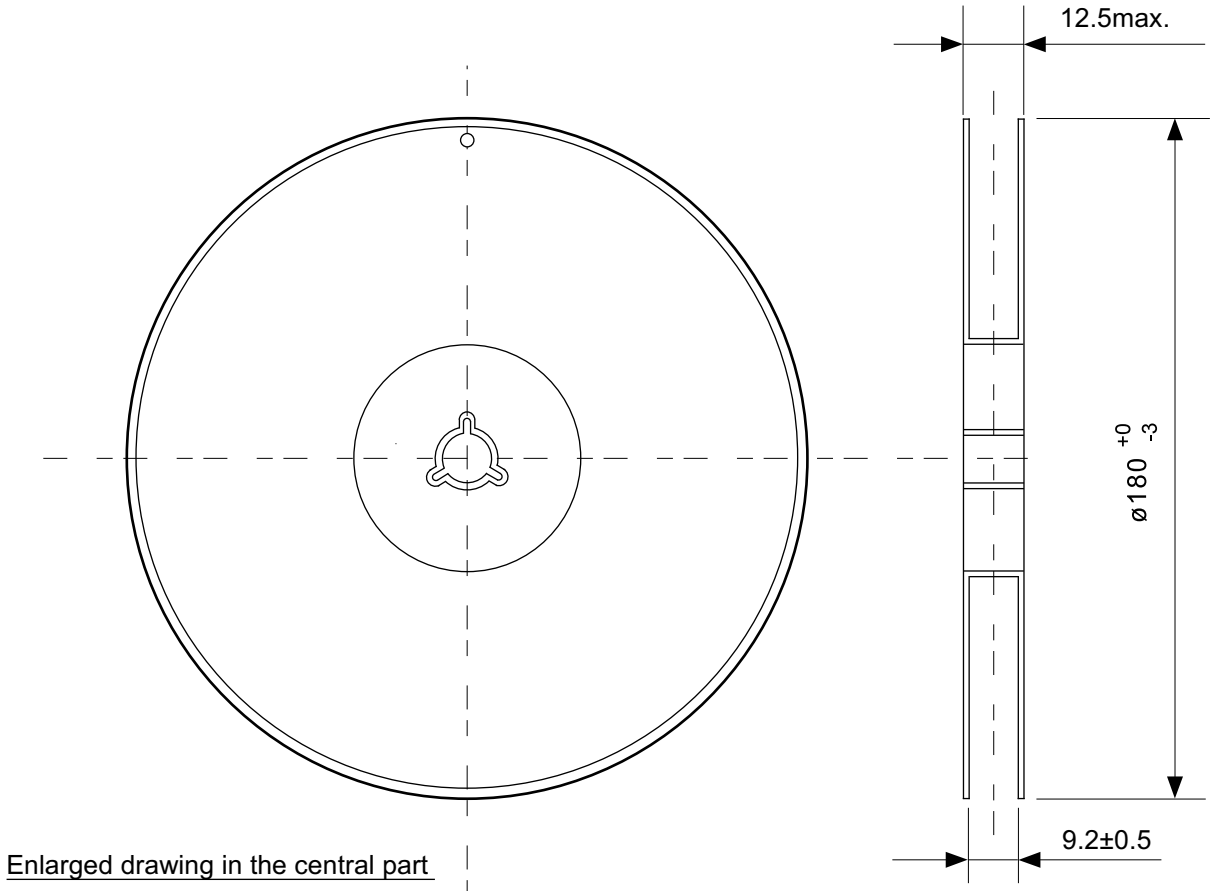




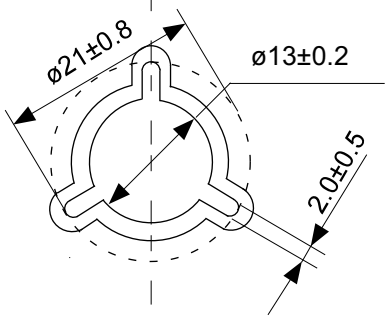
No. MP003-C-C-SD-2.0

TITLE	SOT233-C-Carrier Tape
No.	MP003-C-C-SD-2.0
ANGLE	
UNIT	mm
	ABLIC Inc.

Downloaded from Arrow.com.



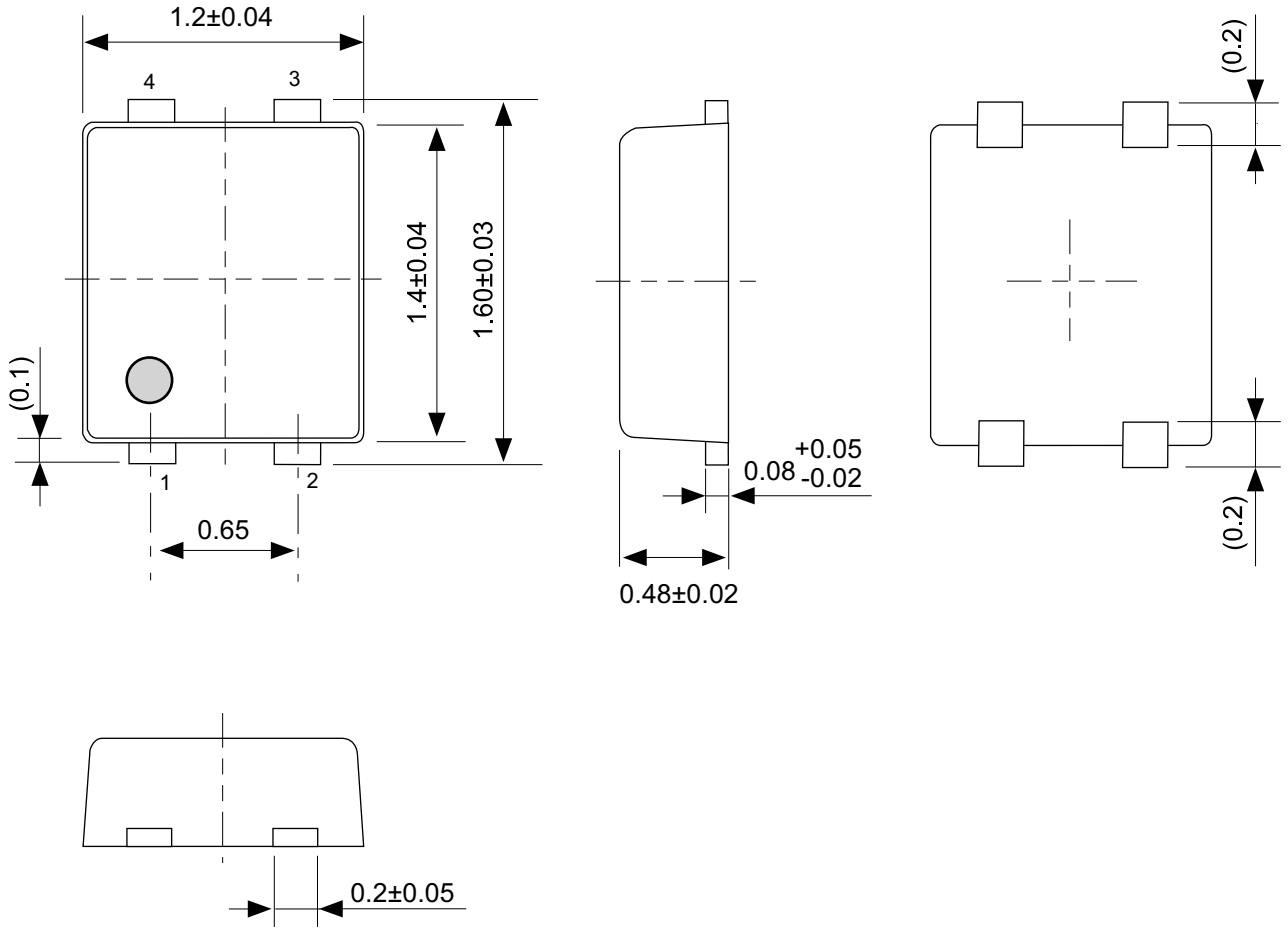
Enlarged drawing in the central part



No. MP003-Z-R-SD-1.0

TITLE	SOT233-C-Reel		
No.	MP003-Z-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

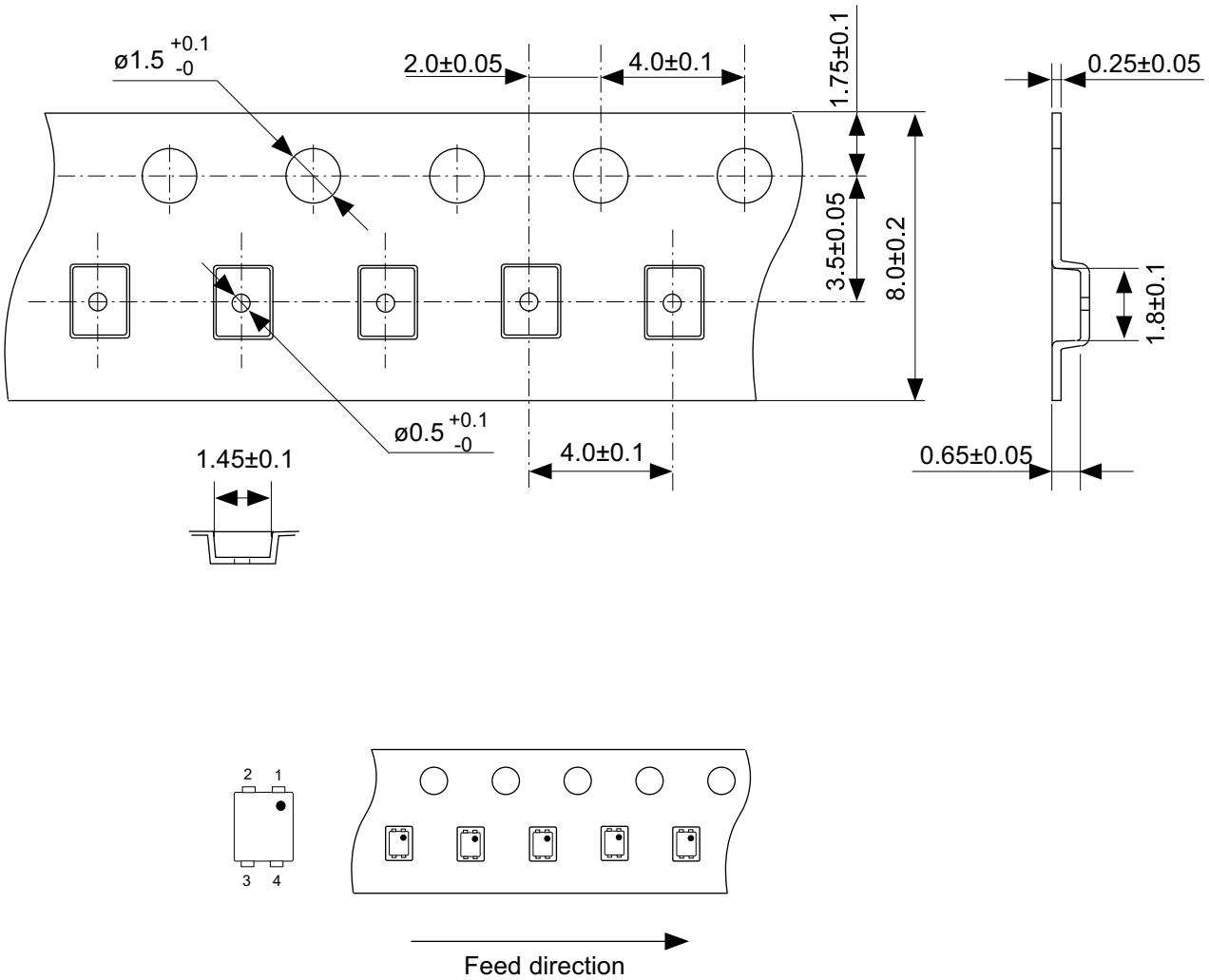
Downloaded from Arrow.com.



No. PF004-A-P-SD-6.0

TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-6.0
ANGLE	
UNIT	mm
ABLIC Inc.	

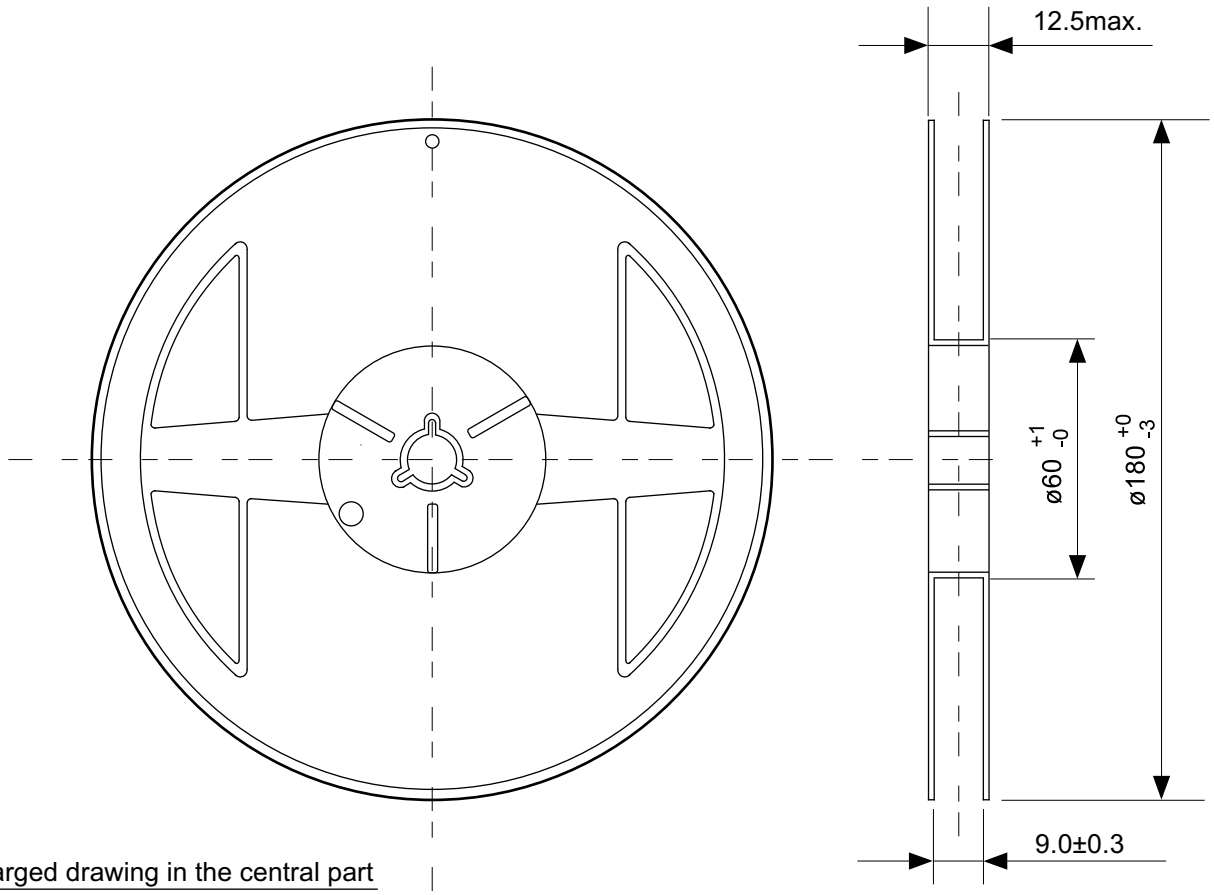
Downloaded from Arrow.com.



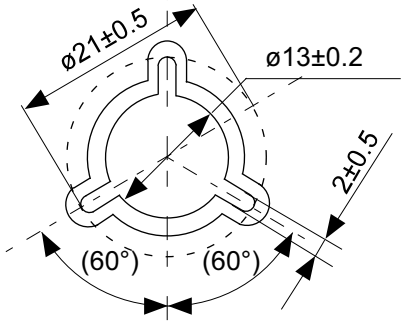
No. PF004-A-C-SD-2.0

TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

Downloaded from Arrow.com.



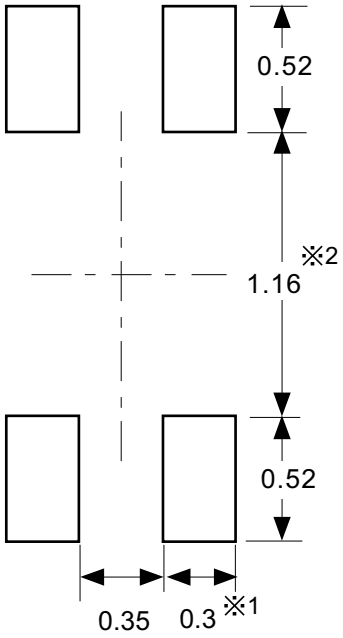
Enlarged drawing in the central part



No. PF004-A-R-SD-1.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

Downloaded from Arrow.com.



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は "SNTパッケージ活用の手引き" を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PF004-A-L-SD-4.1

TITLE	SNT-4A-A -Land Recommendation
No.	PF004-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

Downloaded from Arrow.com.

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07

Downloaded from Arrow.com.