MC10EPT20, MC100EPT20

3.3V LVTTL/LVCMOS to Differential LVPECL Translator

The MC10EPT20 is a 3.3 V TTL/CMOS to differential PECL translator. Because PECL (Positive ECL) levels are used, only +3.3 V and ground are required. The small outline SOIC−8 package and the single gate of the EPT20 makes it ideal for those applications where space, performance, and low power are at a premium.

The 100 Series contains temperature compensation.

Features

- 390 ps Typical Propagation Delay
- Maximum Input Clock Frequency > 1 GHz Typical
- Operating Range V_{CC} = 3.0 V to 3.6 V with GND = 0 V
- PNP TTL Input for Minimal Loading
- Q Output will Default HIGH with Input Open
- Pb−Free Packages are Available

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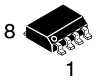
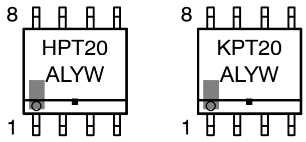
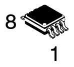
MARKING DIAGRAMS*

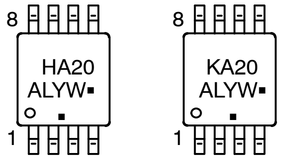


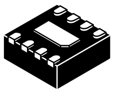
SO−8
D SUFFIX
CASE 751



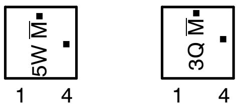


TSSOP−8
DT SUFFIX
CASE 948R





DFN8
MN SUFFIX
CASE 506AA



H = MC10
K = MC100
5W = MC10
3Q = MC100
$\overline{M}$ = Date Code

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

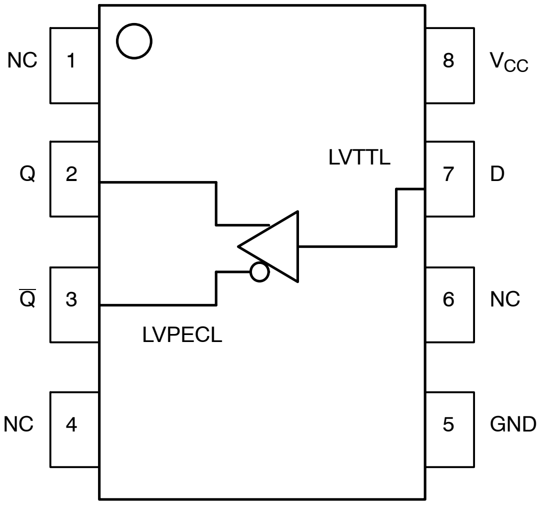


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

PIN	FUNCTION
$Q, \overline{Q}$	Differential PECL Outputs
D	LVTTL Input
V_{CC}	Positive Supply
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

Table 2. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		N/A
Internal Input Pullup Resistor		N/A
ESD Protection	Human Body Model	> 1.5 kV
	Machine Model	> 200 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in
Transistor Count		150 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Power Supply	GND = 0 V		6	V
V_I	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−8 SOIC−8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	SOIC−8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−8 TSSOP−8	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	TSSOP−8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T_{sol}	Wave Solder Pb Pb−Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power)

Table 4. LVTTL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current (V_{in} = 2.7 V)			20	μA
I_{IHH}	Input HIGH Current MAX (V_{in} = 6.0 V)			100	μA
I_{IL}	Input LOW Current (V_{in} = 0.5 V)			−0.6	mA
V_{IK}	Input Clamp Voltage (I_{in} = −18 mA)			−1.2	V
V_{IH}	Input HIGH Voltage	2.0			V
V_{IL}	Input LOW Voltage			0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. 10EPT PECL OUTPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0 V (Note 3)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	Positive Power Supply Current	18	23	28	18	23	28	19	24	29	mA
V_{OH}	Output HIGH Voltage (Note 4)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 4)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Output parameters vary 1:1 with V_{CC}.
4. All loading with 50 Ω to V_{CC} − 2.0 V.

Table 6. 100EPT PECL OUTPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0 V (Note 5)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Positive Power Supply Current	20	25	30	22	27	32	23	28	33	mA
V_{OH}	Output HIGH Voltage (Note 6)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 6)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Output parameters vary 1:1 with V_{CC}.
6. All loading with 50 Ω to V_{CC} − 2.0 V.

Table 7. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, GND = 0 V (Note 7)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Input Clock Frequency		> 1			> 1			> 1		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	280	350	430	300	370	450	320	400	490	ps
t_{SKEW}	Device−to−Device Skew (Note 8)			150			150			170	ps
t_{JITTER}	RMS Random Clock Jitter		1	2		1	2		1	2	ps
t_r t_f	Output Rise/Fall Times (20% − 80%) $Q, \overline{Q}$	70	100	170	80	120	180	90	140	190	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Measured using a LVTTL source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V.
8. Skew is measured between outputs under identical transitions.

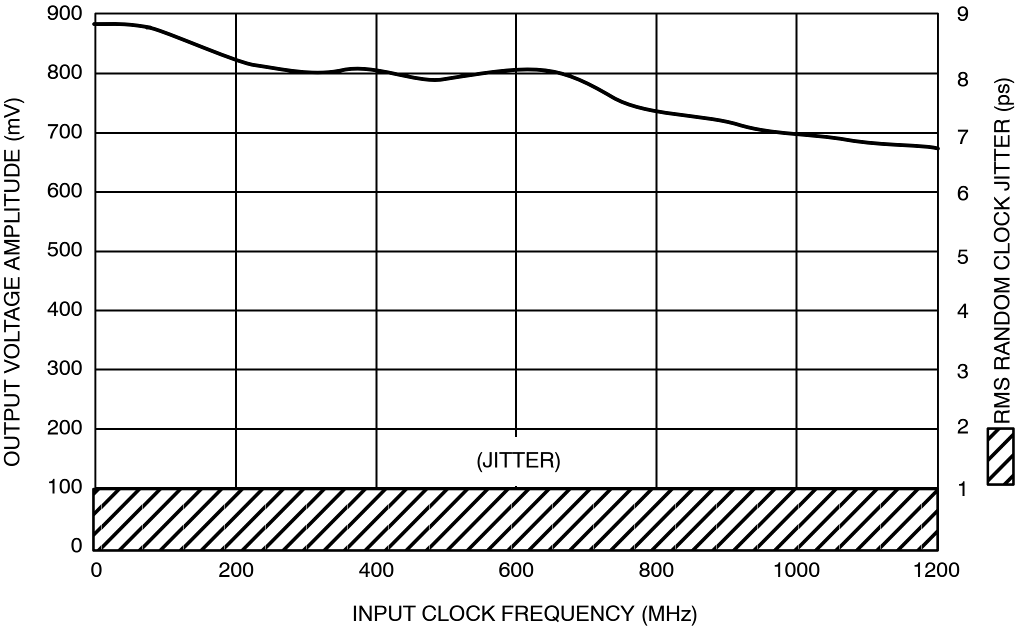


Figure 2. Output Voltage Amplitude (V_{OUTpp})/RMS Jitter vs. Input Clock Frequency at Ambient Temperature

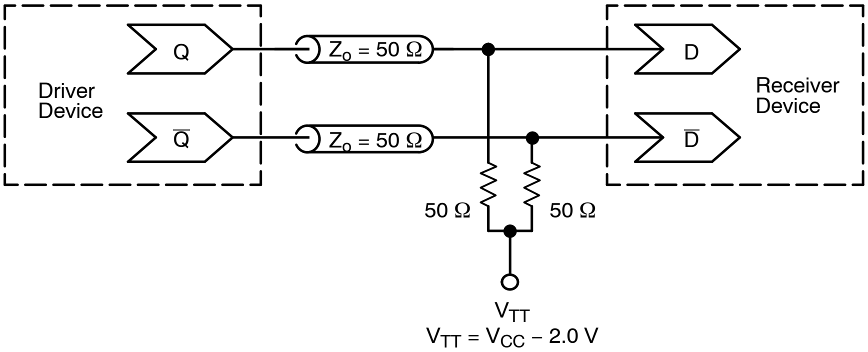


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
MC10EPT20D	SO−8	98 Units / Rail
MC10EPT20DG	SO−8 (Pb−Free)	98 Units / Rail
MC10EPT20DR2	SO−8	2500 / Tape & Reel
MC10EPT20DR2G	SO−8 (Pb−Free)	2500 / Tape & Reel
MC10EPT20DT	TSSOP−8	100 Units / Rail
MC10EPT20DTG	TSSOP−8 (Pb−Free)	100 Units / Rail
MC10EPT20DTR2	TSSOP−8	2500 / Tape & Reel
MC10EPT20DTR2G	TSSOP−8 (Pb−Free)	2500 / Tape & Reel
MC10EPT20MNR4	DFN8	1000 / Tape & Reel
MC10EPT20MNR4G	DFN8 (Pb−Free)	1000 / Tape & Reel
MC100EPT20D	SO−8	98 Units / Rail
MC100EPT20DG	SO−8 (Pb−Free)	98 Units / Rail
MC100EPT20DR2	SO−8	2500 / Tape & Reel
MC100EPT20DR2G	SO−8 (Pb−Free)	2500 / Tape & Reel
MC100EPT20DT	TSSOP−8	100 Units / Rail
MC100EPT20DTG	TSSOP−8 (Pb−Free)	100 Units / Rail
MC100EPT20DTR2	TSSOP−8	2500 / Tape & Reel
MC100EPT20DTR2G	TSSOP−8 (Pb−Free)	2500 / Tape & Reel
MC100EPT20MNR4	DFN8	1000 / Tape & Reel
MC100EPT20MNR4G	DFN8 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

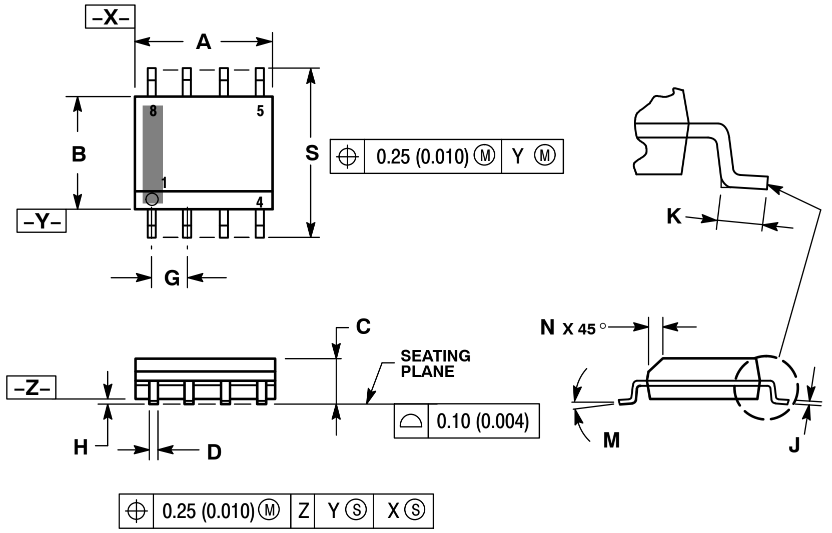
AN1405/D	–	ECL Clock Distribution Techniques
AN1406/D	–	Designing with PECL (ECL at +5.0 V)
AN1503/D	–	ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D	–	Metastability and the ECLinPS Family
AN1568/D	–	Interfacing Between LVDS and ECL
AN1672/D	–	The ECL Translator Guide
AND8001/D	–	Odd Number Counters Design
AND8002/D	–	Marking and Date Codes
AND8020/D	–	Termination of ECL Logic Devices
AND8066/D	–	Interfacing with ECLinPS
AND8090/D	–	AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

SOIC−8 NB

CASE 751−07

ISSUE AH

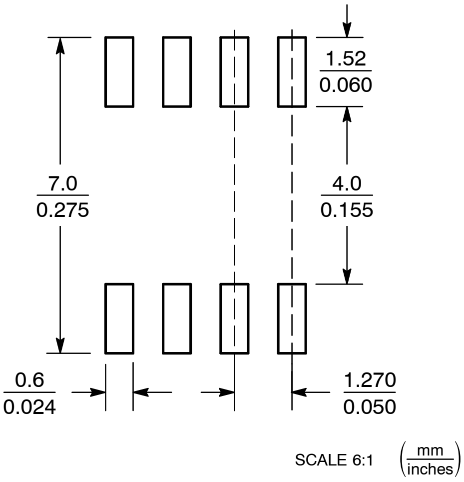


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

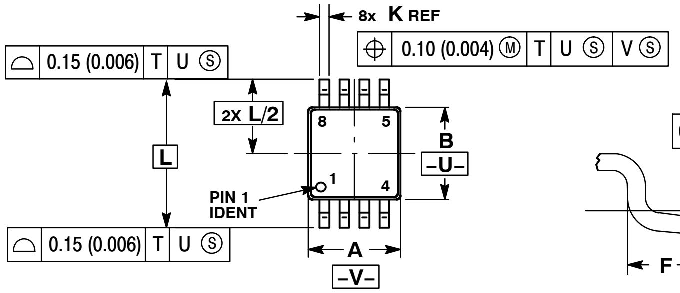
SOLDERING FOOTPRINT*

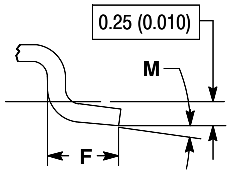


*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

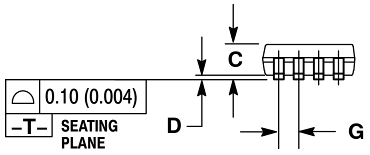
PACKAGE DIMENSIONS

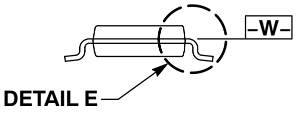
TSSOP−8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R−02
ISSUE A





DETAIL E





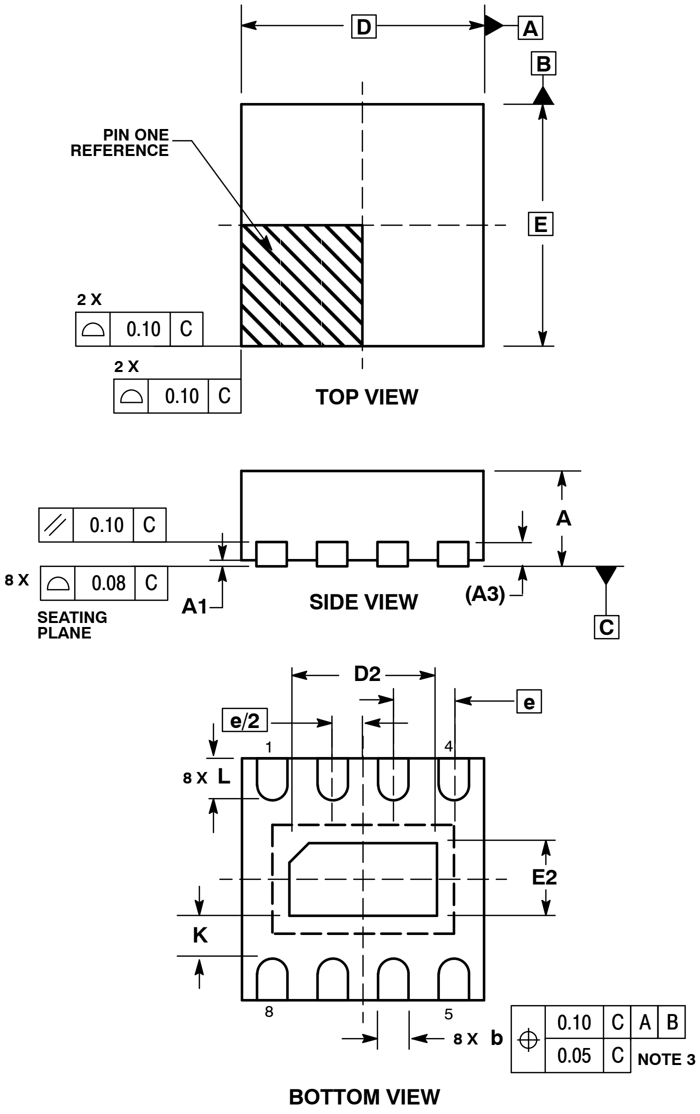
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

PACKAGE DIMENSIONS

DFN8
CASE 506AA−01
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	−−−
L	0.25	0.35

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