Lead-free Green

AP72250

0.6V TO 5.5V INPUT SYNCHRONOUS BOOST CONVERTER WITH 4.7A SWITCHES

Description

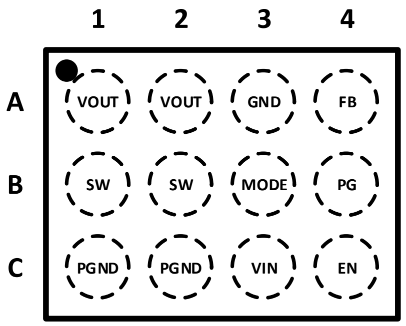
The AP72250 is a synchronous boost converter with a minimum 1V input startup voltage and can operate in a wide input voltage range of 0.6V to 5.5V. The device fully integrates a 20mΩ high-side power MOSFET and a 26mΩ low-side power MOSFET to provide high-efficiency step-up DC-DC conversion.

The AP72250 device is easily used by minimizing the external component count due to its adoption of peak current mode control, allowing it to handle wide input-to-output ratios. It also achieves outstanding performance in line and load transient responses and seamless transitions between boost and pass-through modes.

The device is available in a small 1.75mm x 1.35mm, 12-ball WLCSP.

Pin Assignments

(Top View)



X1-WLB1713-12

Features

- VIN: 0.6V to 5.5V
- Minimum Input Startup Voltage: 1V
- Output Voltage (VOUT): 1.7V to 5.5V
- 4.7A Switching Current
- 0.8V ± 1% Reference Voltage
- 20μA Low Quiescent Current (Pulse Frequency Modulation)
- 900kHz Switching Frequency
- Up to 89% Efficiency at 5mA Light Load
- Selectable Operation Mode
  - Pulse Frequency Modulation (PFM)
  - Ultrasonic Mode (USM)
  - Forced Pulse Width Modulation (FPWM)
- Power-Good Indicator with 5MΩ Internal Pull-up Resistor
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - Peak Current Limit
  - Negative (Valley) Current Limit
  - Output Short Circuit Protection (SCP)
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Applications

- Low voltage power cells
- Portable consumer devices
- Supercapacitor charge storages
- USB power supplies
- Power banks
- Industrial metering equipments

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Application Circuit

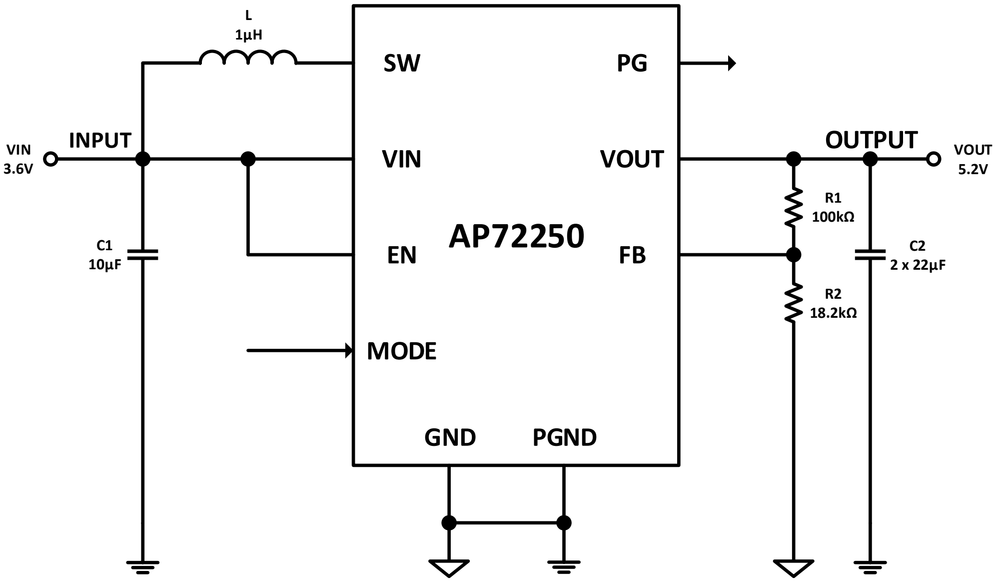

Figure 1. Typical Application Circuit

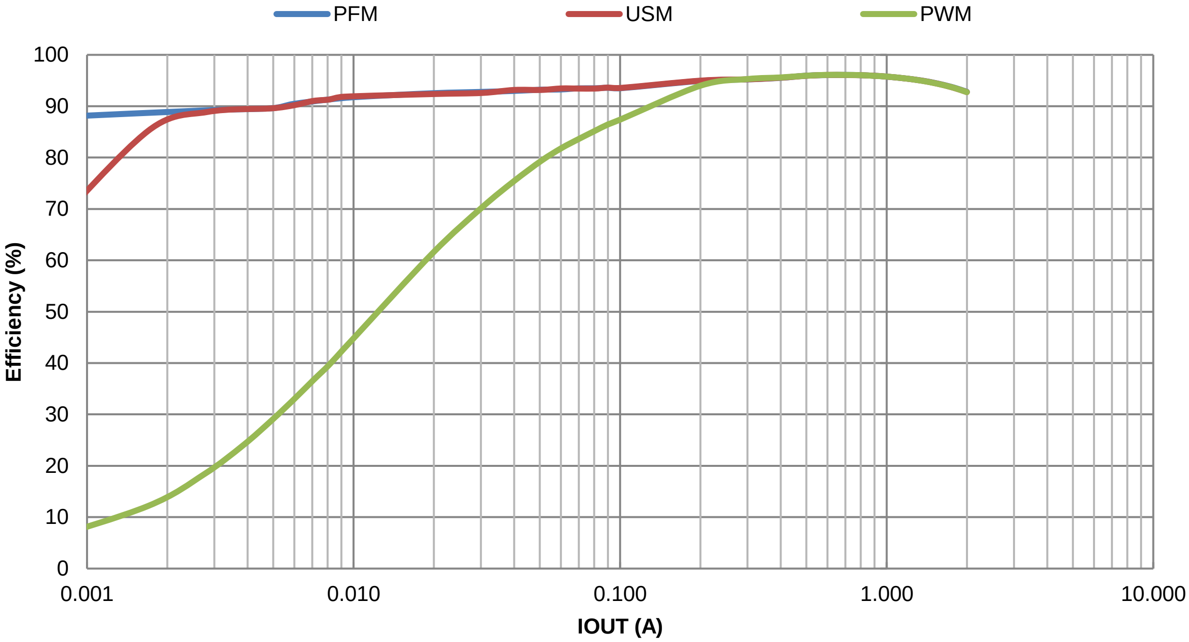

Figure 2. Efficiency vs. Output Current, VIN = 3.6V, VOUT = 5.2V, L = 1µH

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Pin Descriptions

Pin Name	Pin Number	Function
VOUT	A1, A2	Output Voltage Power Rail. Connect VOUT to the output load as shown in Figure 1.
GND	A3	Analog Ground used by the control circuitry.
FB	A4	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See **Setting the Output Voltage** section for more details.
SW	B1, B2	Power Switching Output. SW is the switching node that converts power to the output. Connect the inductor from SW to VIN.
MODE	B3	Mode Select. MODE is used to select the operation mode of the device. Connect MODE to GND to set the device to operate in PFM Mode. Leave MODE floating to set the device to operate in USM. Connect MODE to VCC to set the device to operate in Forced PWM.
PG	B4	Power-Good. Open drain power-good output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start. There is an internal 5MΩ pull-up resistor connected to PG.
PGND	C1, C2	Power Ground.
VIN	C3	Power Input. VIN supplies power to the IC as well as the step-up converter power MOSFETs. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. Drive VIN with a 0.6V (1.0V for startup) to 5.5V power source. See **Input Capacitor** section for more details.
EN	C4	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Connect to VIN or leave floating for automatic startup.

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Functional Block Diagram

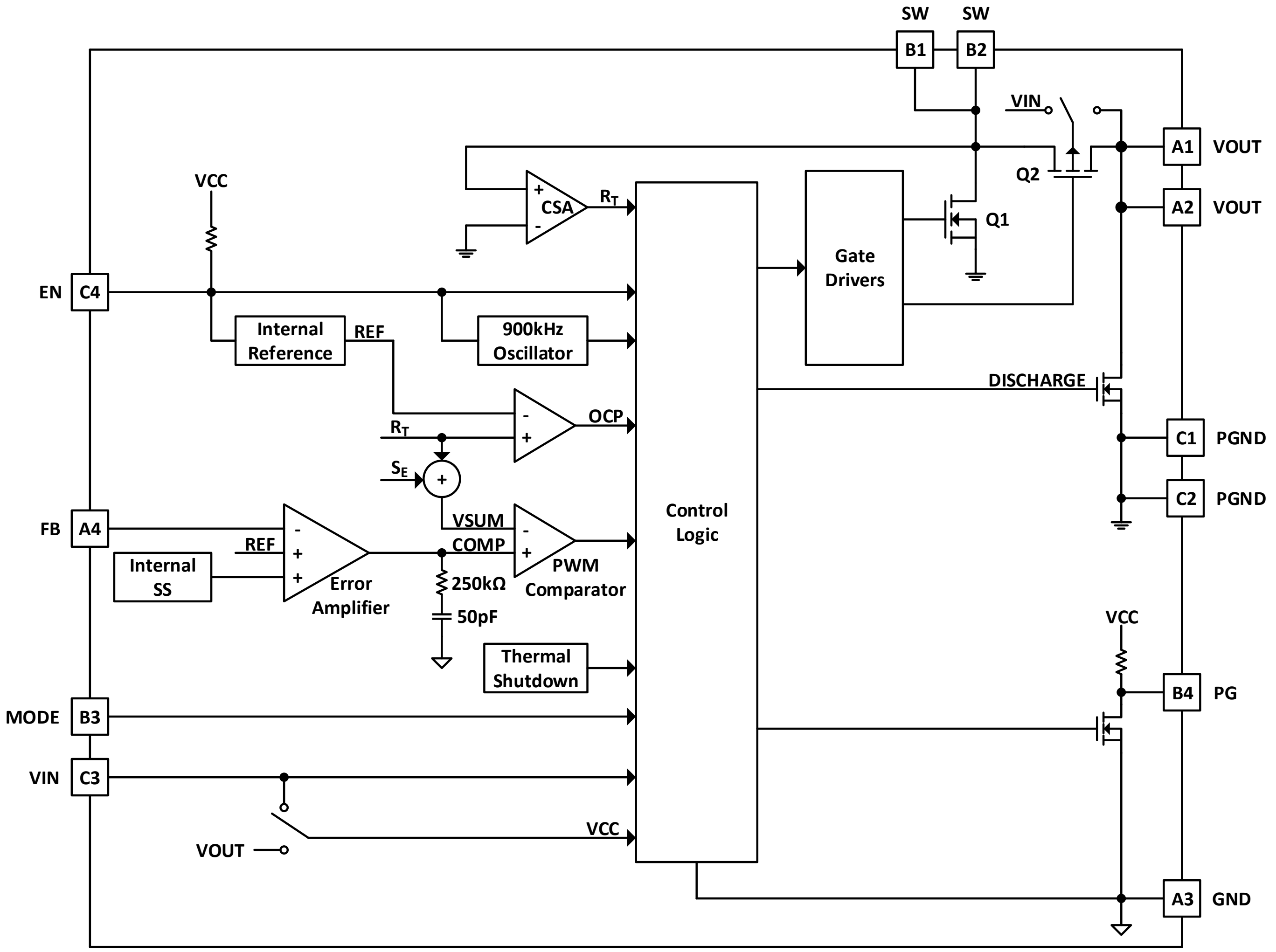

Figure 3. Functional Block Diagram

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Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
VIN	Supply Pin Voltage	-0.3 to +6.0 (DC)	V
		-0.3 to +7.0 (400ms)	
VOUT	Output Pin Voltage	-0.3 to +6.0 (DC)	V
		-0.3 to +7.0 (400ms)	
V_{FB}	Feedback Pin Voltage	-0.3 to +2.5	V
V_{SW}	Switch Pin Voltage	-1.0 to +6.0 (DC)	V
		-2.5 to +10.0 (20ns)	
V_{MODE}	Mode Select Pin Voltage	-0.3 to +6.0	V
V_{PG}	Power-Good Pin Voltage	-0.3 to +6.0	V
V_{EN}	Enable Pin Voltage	-0.3 to +6.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+160	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±2000	V
CDM	Charged Device Model	±1500	V

Notes: 4. Stresses greater than the *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.

5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	X1-WLB1713-12	90	°C/W
θ_{JC}	Junction to Case	X1-WLB1713-12	11	°C/W

Note: 6. Test condition for X1-WLB1713-12: Device mounted on FR-4 substrate, four-layer PCB, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions (Note 7) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	0.6	5.5	V
VOUT	Output Voltage	1.7	5.5	V
T_A	Operating Ambient Temperature	-40	+85	°C
T_J	Operating Junction Temperature	-40	+125	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

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Electrical Characteristics

(@T_J = +25°C, VIN = V_{EN} = 3.6V, unless otherwise specified. Min/Max limits apply across the recommended operating junction temperature range, -40°C to +125°C, and input voltage range, 0.6V to 5.5V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V, VIN = 5.5V	—	2.5	5.3	µA
I_Q	Quiescent Supply Current	V_{EN} = VIN, V_{FB} = 1.0V	—	20	30	µA
		V_{EN} = VIN, V_{MODE} = GND R1 = 1.05MΩ, R2 = 200kΩ	—	50	70	µA
		V_{EN} = VIN, V_{MODE} = Floating R1 = 1.05MΩ, R2 = 200kΩ	—	200	280	µA
		V_{EN} = V_{MODE} = VIN R1 = 1.05MΩ, R2 = 200kΩ	—	15	20	mA
POR	VIN Power-on Reset Rising Threshold	—	—	1.0	1.1	V
UVLO	VIN Undervoltage Lockout Falling Threshold	—	0.44	0.57	0.70	V
$R_{DS(ON)1}$	High-Side Power MOSFET On-Resistance (Note 8)	—	—	20	27	mΩ
$R_{DS(ON)2}$	Low-Side Power MOSFET On-Resistance (Note 8)	—	—	26	38	mΩ
$R_{DISCHARGE}$	VOUT Soft Discharge On-Resistance	—	100	200	300	Ω
I_{HS_LEAK}	HS Leakage Current	VOUT = 5.5V, V_{EN} = V_{SW} = 0V	—	—	0.8	µA
I_{PEAK_LIMIT}	LS Peak Current Limit (Note 8)	From Drain to Source, VIN or VOUT > 2V	4.15	4.7	5.8	A
I_{NCL}	HS Negative Current Limit	From Drain to Source	-2.4	-2.0	-1.6	A
I_{PFMPK}	PFM Peak Current Limit	—	1.2	1.5	1.8	A
I_{ZC}	Zero Cross Current Threshold	—	—	30	—	mA
f_{SW}	Oscillator Frequency	CCM	0.77	0.90	1.03	MHz
		V_{MODE} = Floating	20.5	25	—	kHz
V_{MODE_PFM}	PFM Mode Logic Threshold	V_{MODE} = GND	—	—	0.4	V
V_{MODE_USM}	Ultrasonic Mode Logic Threshold	V_{MODE} = Floating	—	0.55	—	V
V_{MODE_PWM}	PWM Mode Logic Threshold	V_{MODE} = VIN	0.7	—	—	V
I_{MODE}	MODE Input Current	V_{MODE} = 0V	—	0.2	—	µA
		V_{MODE} = 5.5V	—	0.2	—	µA
t_{OFF_MIN}	Minimum Off-Time	—	—	120	—	ns
V_{FB}	Feedback Voltage	CCM	0.792	0.800	0.808	V
V_{EN_H}	EN Logic High Threshold	VIN < 1.6V	0.78	—	—	V
		VIN > 1.6V	0.90	—	—	V
V_{EN_L}	EN Logic Low Threshold	—	—	—	0.2	V
I_{EN}	EN Input Current	V_{EN} = 5.5V	—	0.1	—	µA
		V_{EN} = 0V	—	0.1	—	µA
PG_{UV_FALL}	Undervoltage Falling Threshold	Percent of Output Regulation, Fault	—	75	—	%
PG_{UV_RISE}	Undervoltage Rising Threshold	Percent of Output Regulation, Good	—	80	—	%
PG_{OV_RISE}	Overvoltage Rising Threshold	Percent of Output Regulation, Fault	—	120	—	%
PG_{OV_FALL}	Overvoltage Falling Threshold	Percent of Output Regulation, Good	—	115	—	%
t_{PG_RD}	Power-Good Rise Delay Time	—	—	2	—	ms
t_{PG_FD}	Power-Good Fall Delay Time	—	—	5	—	µs
V_{PG_OL}	Power-Good Output Logic Low	I_{PG} = -1mA	—	—	0.4	V
R_{PG}	Power-Good Pull-up Resistor	—	—	5	—	MΩ
T_{SD}	Thermal Shutdown (Note 8)	—	—	+150	—	°C
T_{HYS}	Thermal Shutdown Hysteresis (Note 8)	—	—	+20	—	°C

Note: 8. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

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Typical Performance Characteristics (AP72250 @T_A = +25°C, VIN = 3.6V, VOUT = 5.2V, BOM = Table 1, unless otherwise specified.)

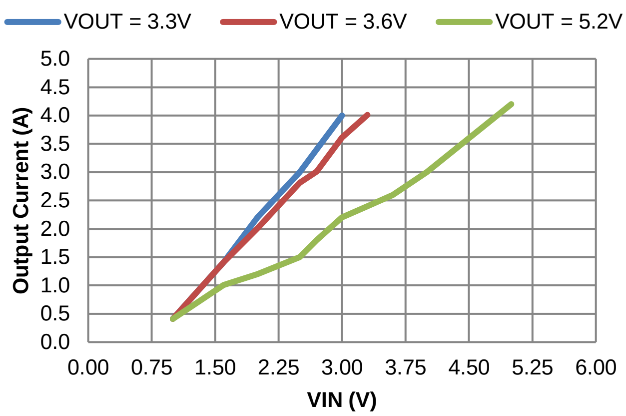

Figure 4. Output Current vs. Input Voltage

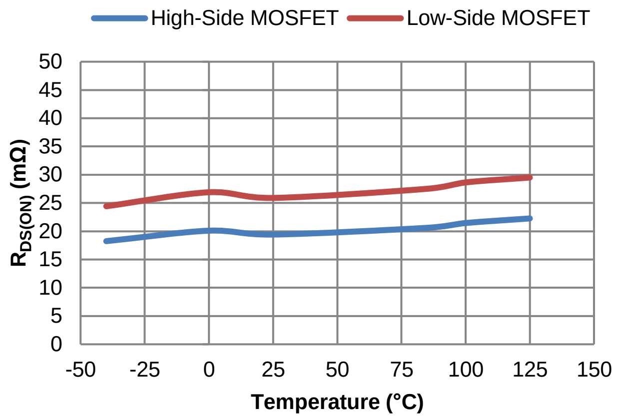

Figure 5. Power MOSFET $R_{DS(ON)}$ vs. Temperature

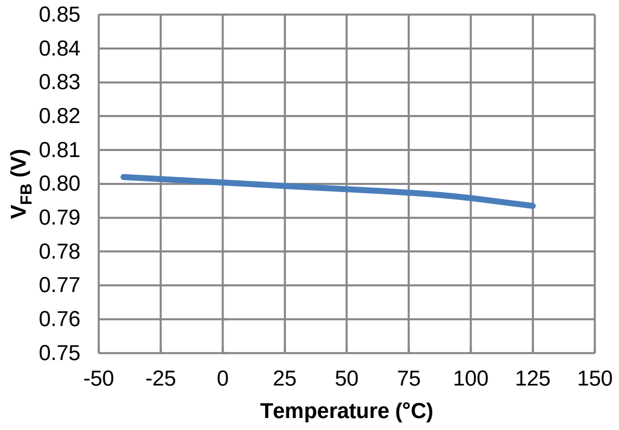

Figure 6. Feedback Voltage vs. Temperature, IOUT = 1A

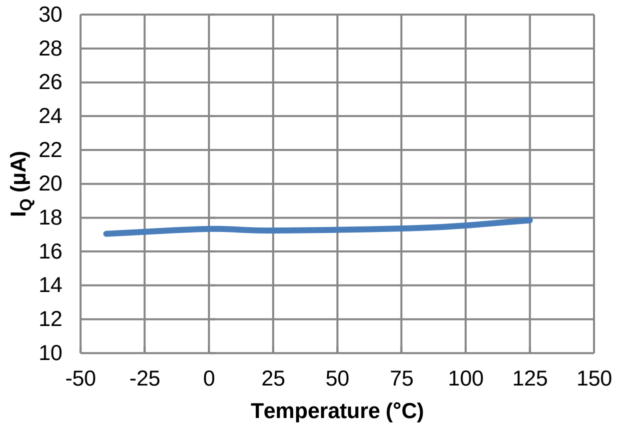

Figure 7. I_Q vs. Temperature, V_{EN} = VIN, V_{FB} = 1.0V

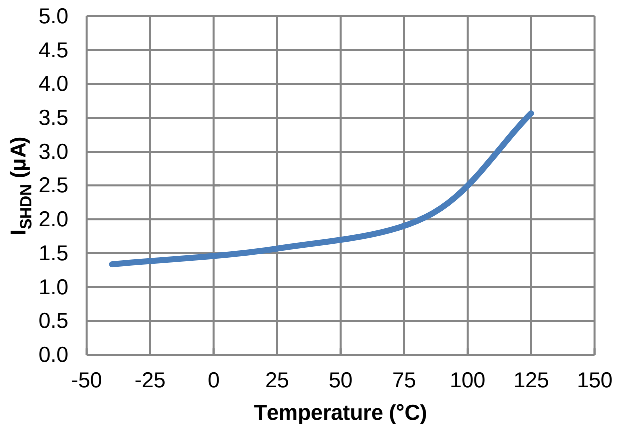

Figure 8. I_{SHDN} vs. Temperature

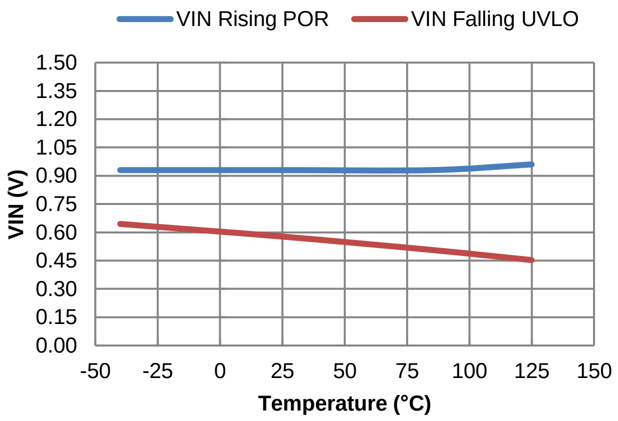

Figure 9. VIN Power-On Reset and UVLO vs. Temperature

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Typical Performance Characteristics (AP72250 @T_A = +25°C, VIN = 3.6V, VOUT = 5.2V, BOM = Table 1, unless otherwise specified.) (continued)

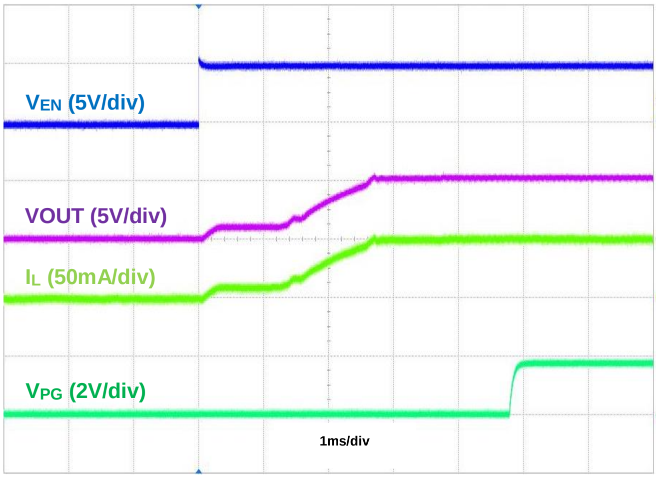

Figure 10. Startup Using EN, IOUT = 50mA

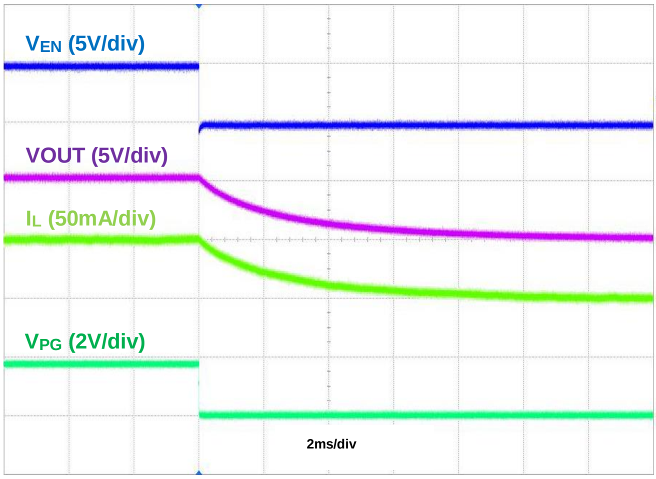

Figure 11. Shutdown Using EN, IOUT = 50mA

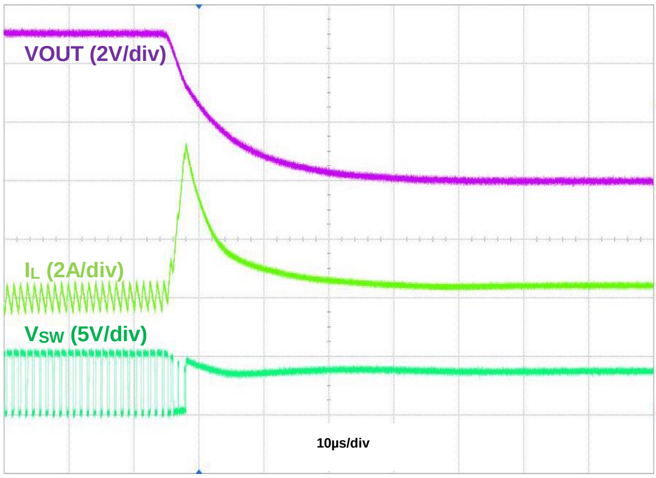

Figure 12. Output Short Protection, IOUT = 0A

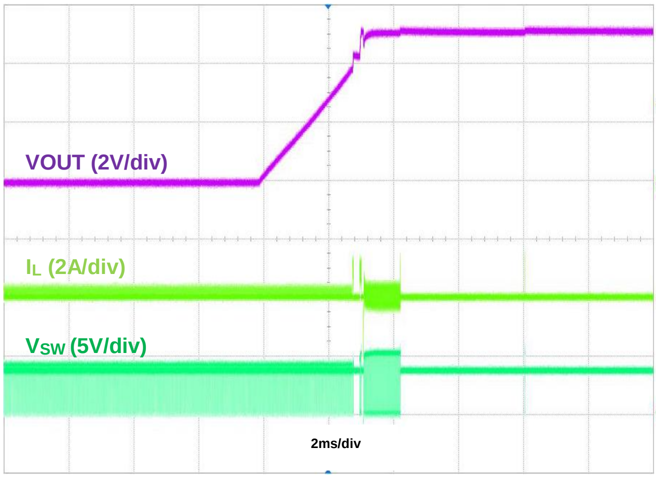

Figure 13. Output Short Recovery, IOUT = 0A

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Typical Performance Characteristics (AP72250 @T_A = +25°C, VIN = 3.6V, VOUT = 5.2V, MODE = PFM, BOM = Table 1, unless otherwise specified.) (continued)

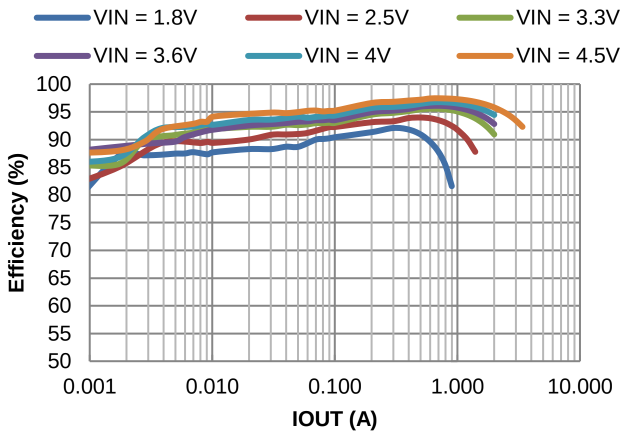

Figure 14. Efficiency vs. Output Current, VOUT = 5.2V

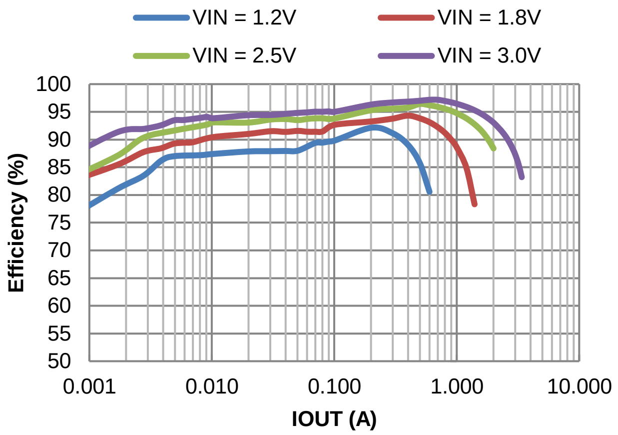

Figure 15. Efficiency vs. Output Current, VOUT = 3.3V

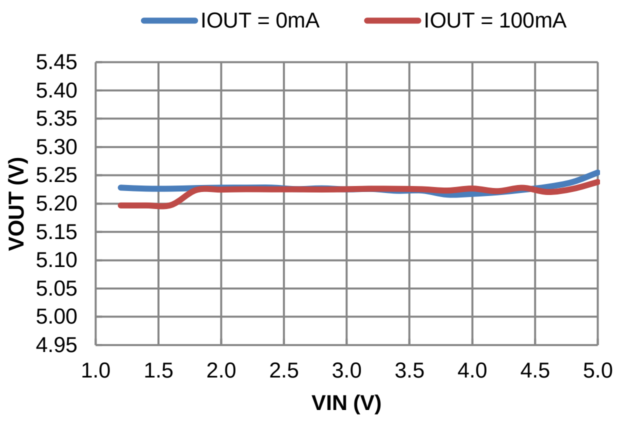

Figure 16. Line Regulation

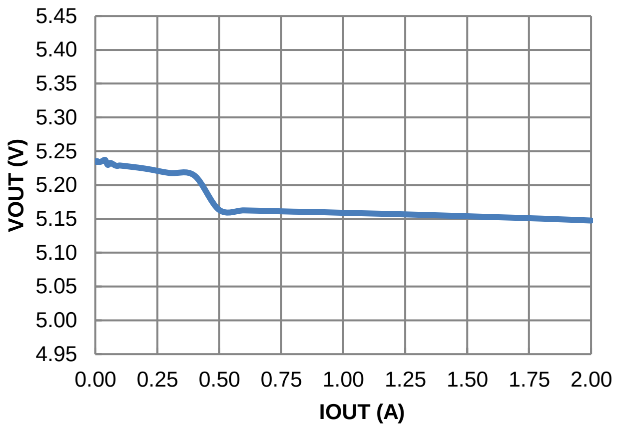

Figure 17. Load Regulation

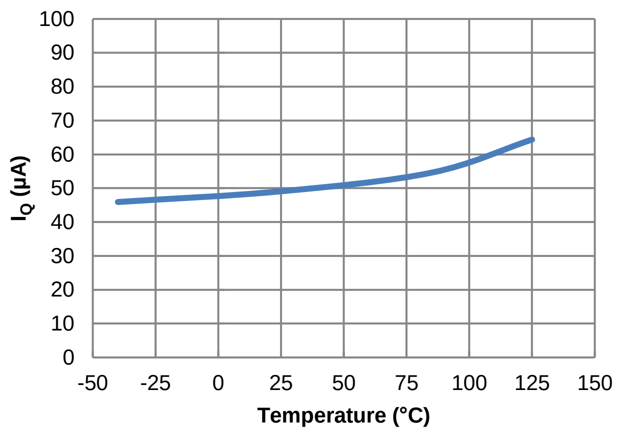

Figure 18. I_Q vs. Temperature,
V_{EN} = VIN, V_{MODE} = GND, R1 = 1.05MΩ, R2 = 200kΩ

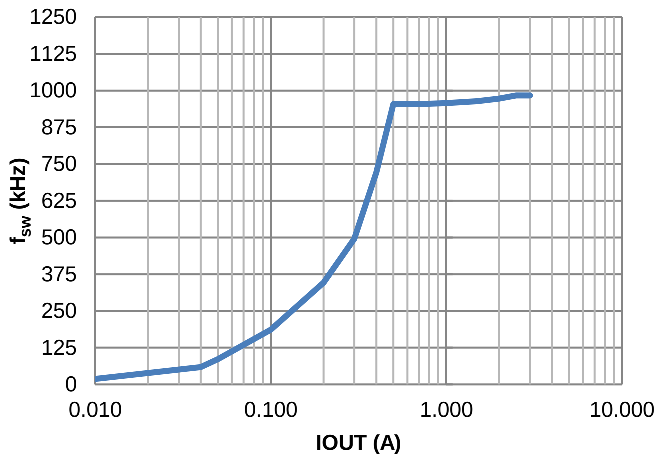

Figure 19. f_{SW} vs. Load

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Typical Performance Characteristics (AP72250 @T_A = +25°C, VIN = 3.6V, VOUT = 5.2V, MODE = PFM, BOM = Table 1, unless otherwise specified.) (continued)

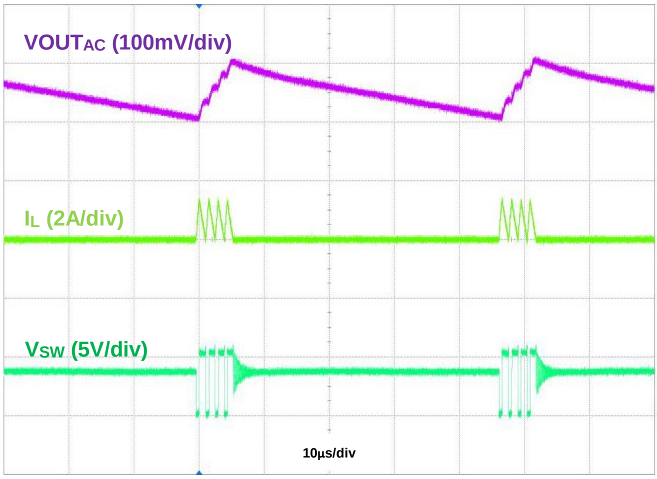

Figure 20. Output Voltage Ripple, VOUT = 5.2V, IOUT = 50mA

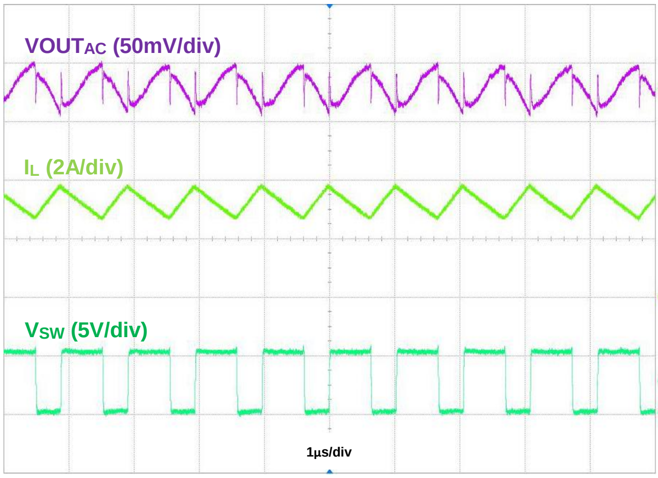

Figure 21. Output Voltage Ripple, VOUT = 5.2V, IOUT = 2A

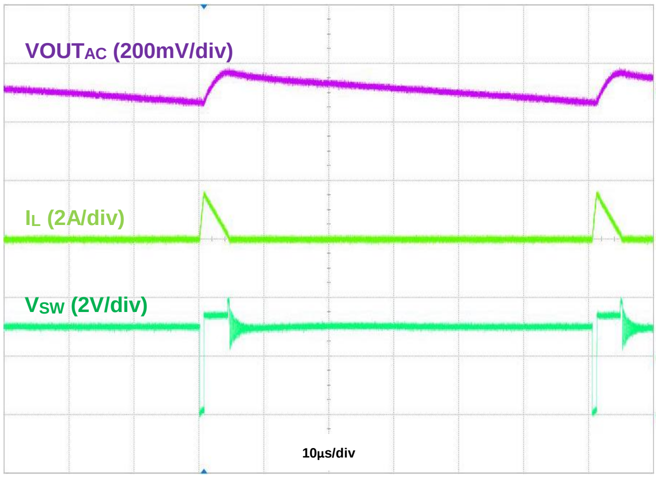

Figure 22. Output Voltage Ripple, VIN = 3V, VOUT = 3.3V, IOUT = 50mA

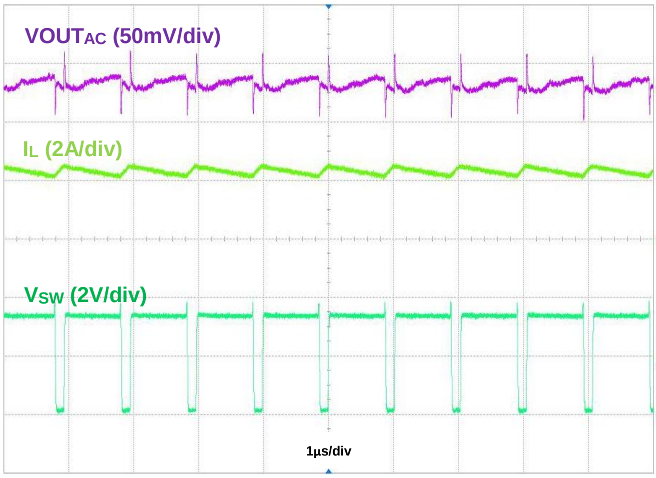

Figure 23. Output Voltage Ripple, VIN = 3V, VOUT = 3.3V, IOUT = 2A

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Typical Performance Characteristics (AP72250 @T_A = +25°C, VIN = 3.6V, VOUT = 5.2V, MODE = PFM, BOM = Table 1, unless otherwise specified.) (continued)

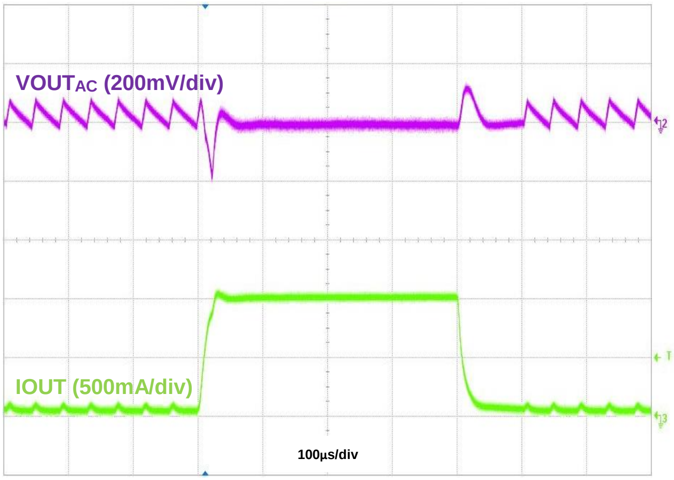

Figure 24. Load Transient, IOUT = 50mA to 1A to 50mA

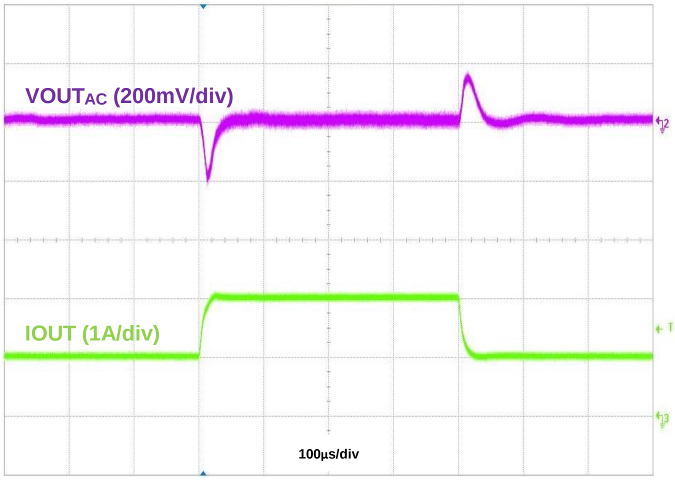

Figure 25. Load Transient, IOUT = 1A to 2A to 1A

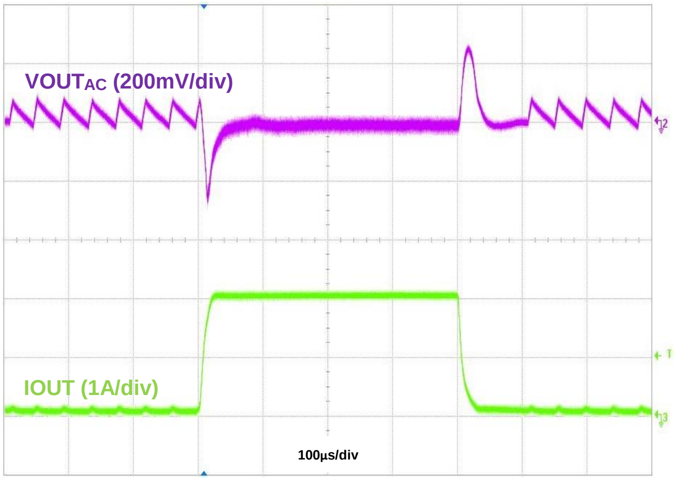

Figure 26. Load Transient, IOUT = 50mA to 2A to 50mA

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Typical Performance Characteristics (AP72250 @T_A = +25°C, VIN = 3.6V, VOUT = 5.2V, MODE = USM, BOM = Table 1, unless otherwise specified.) (continued)

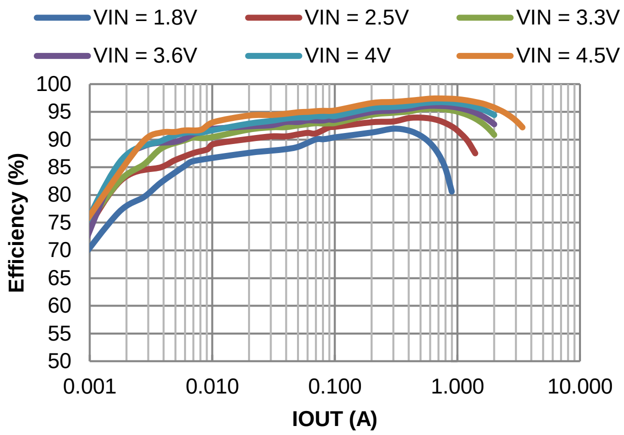

Figure 27. Efficiency vs. Output Current, VOUT = 5.2V

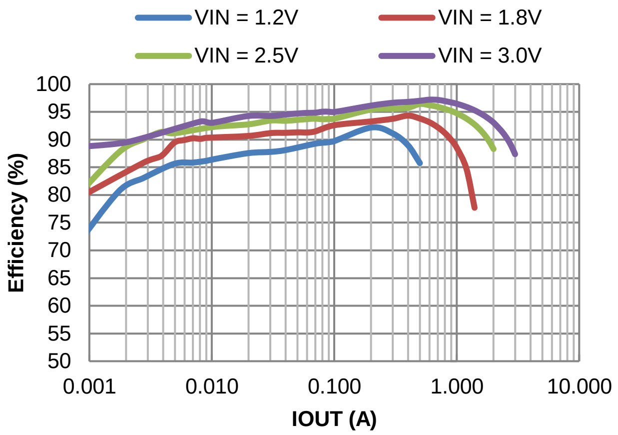

Figure 28. Efficiency vs. Output Current, VOUT = 3.3V

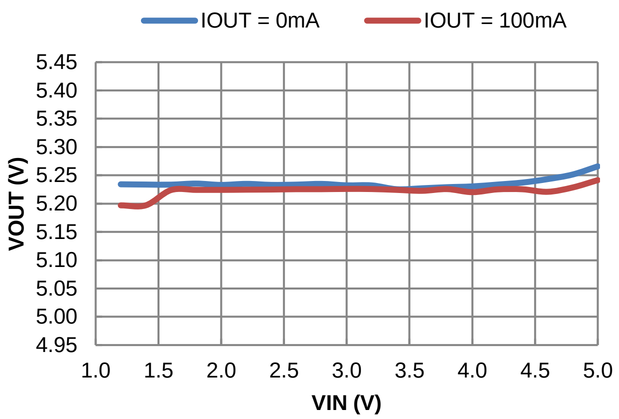

Figure 29. Line Regulation

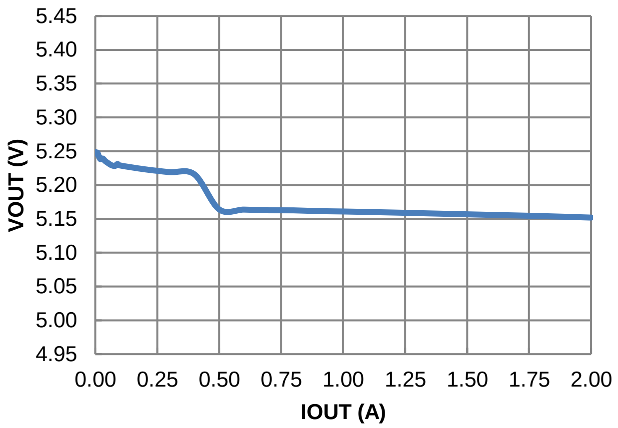

Figure 30. Load Regulation

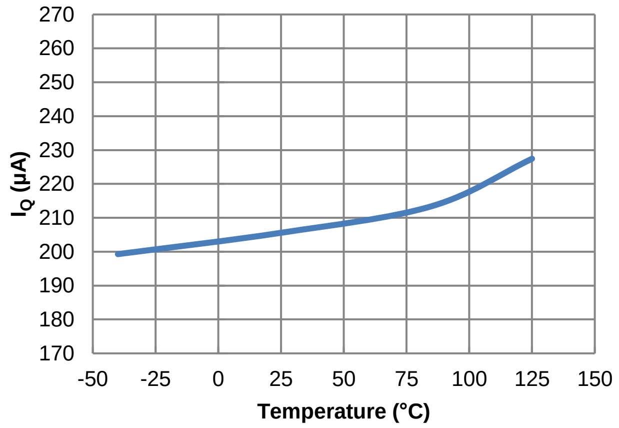

Figure 31. I_Q vs. Temperature, V_{EN} = VIN, V_{MODE} = Floating, R1 = 1.05MΩ, R2 = 200kΩ

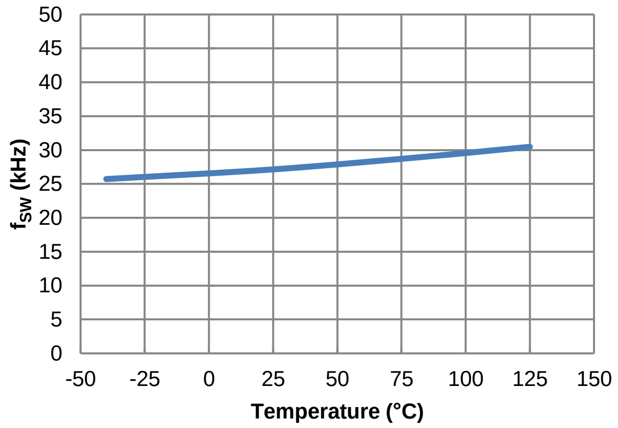

Figure 32. f_{SW} vs. Temperature, IOUT = 0A

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Typical Performance Characteristics (AP72250 @T_A = +25°C, VIN = 3.6V, VOUT = 5.2V, MODE = USM, BOM = Table 1, unless otherwise specified.) (continued)

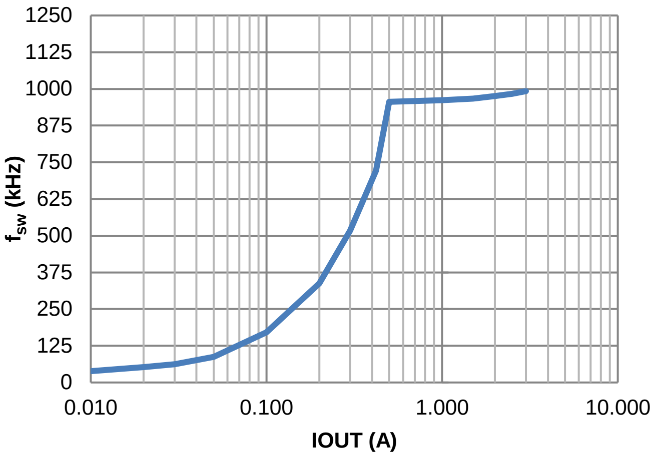

Figure 33. f_{SW} vs. Load

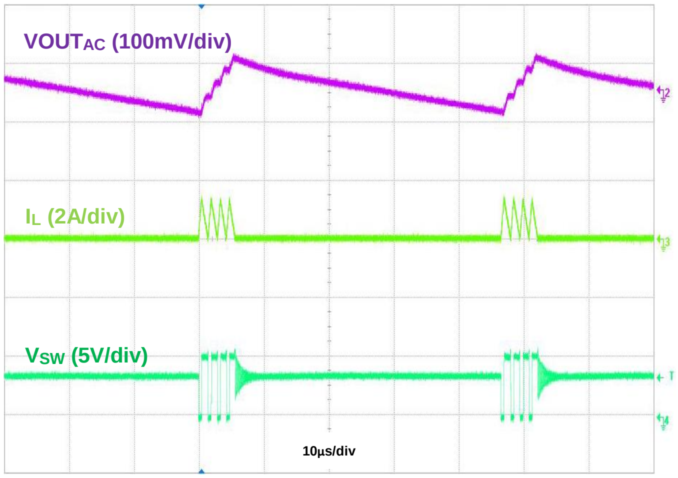

Figure 34. Output Voltage Ripple, VOUT = 5.2V, IOUT = 50mA

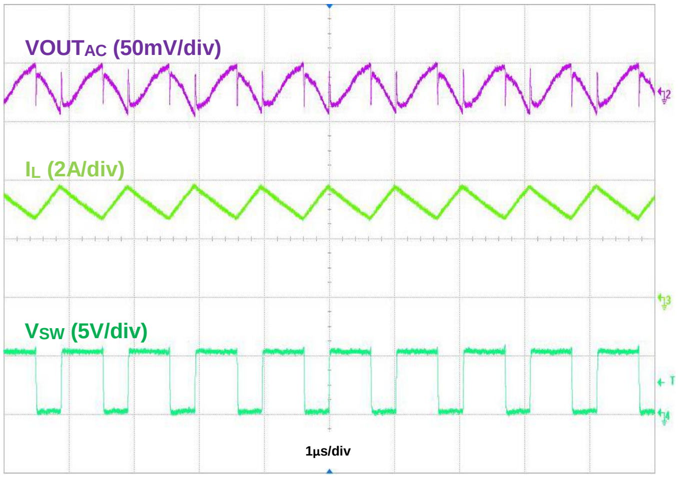

Figure 35. Output Voltage Ripple, VOUT = 5.2V, IOUT = 2A

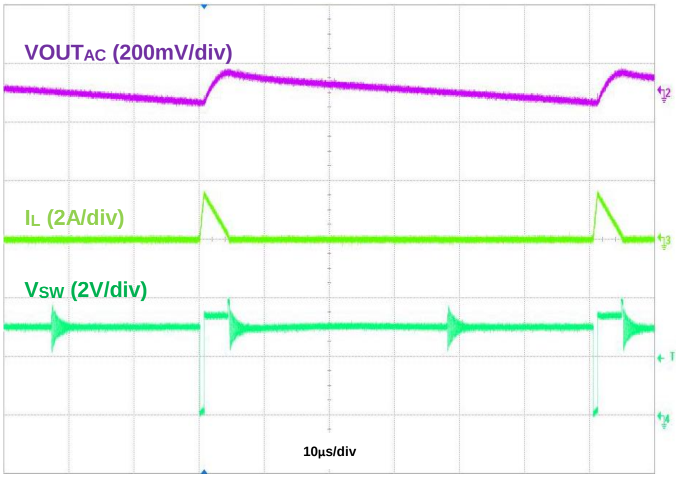

Figure 36. Output Voltage Ripple, VIN = 3V,
VOUT = 3.3V, IOUT = 50mA

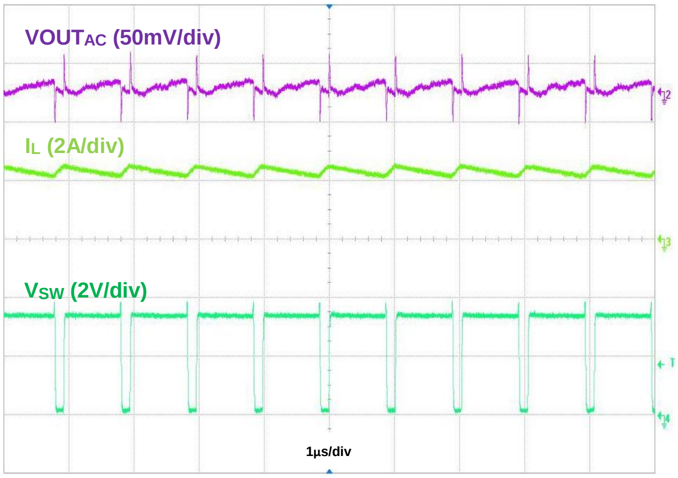

Figure 37. Output Voltage Ripple, VIN = 3V,
VOUT = 3.3V, IOUT = 2A

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Typical Performance Characteristics (AP72250 @T_A = +25°C, VIN = 3.6V, VOUT = 5.2V, MODE = USM, BOM = Table 1, unless otherwise specified.) (continued)

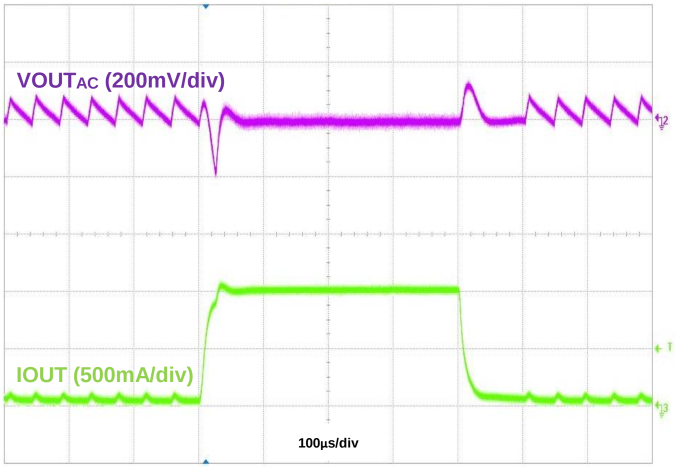

Figure 38. Load Transient, IOUT = 50mA to 1A to 50mA

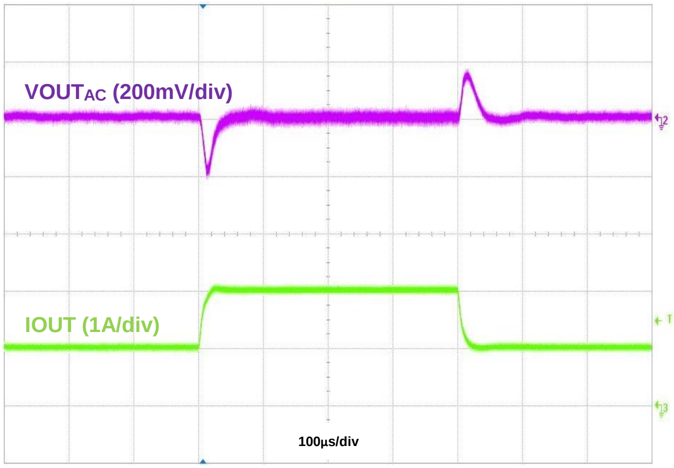

Figure 39. Load Transient, IOUT = 1A to 2A to 1A

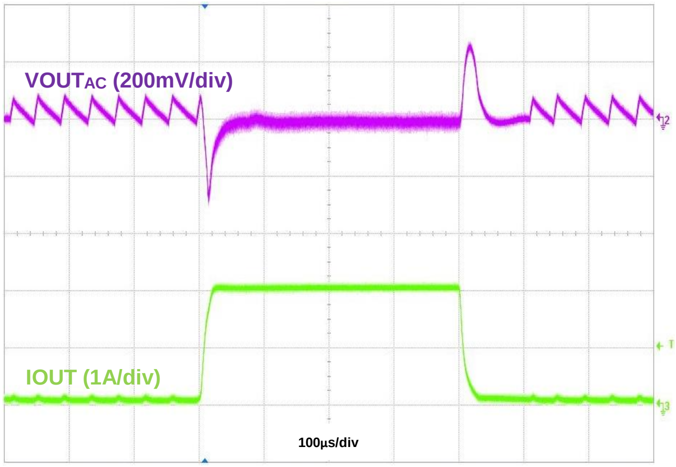

Figure 40. Load Transient, IOUT = 50mA to 2A to 50mA

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Typical Performance Characteristics (AP72250 @T_A = +25°C, VIN = 3.6V, VOUT = 5.2V, MODE = PWM, BOM = Table 1, unless otherwise specified.) (continued)

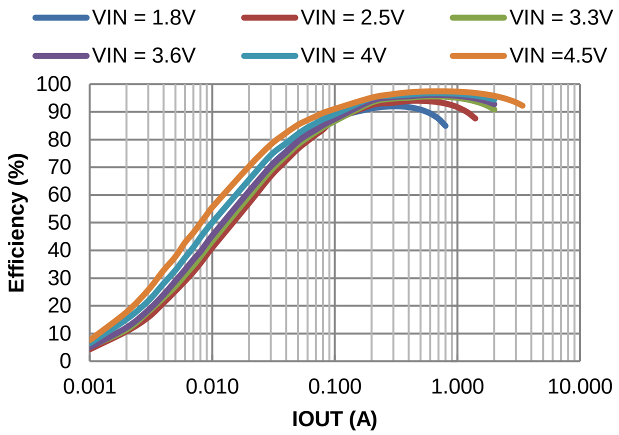

Figure 41. Efficiency vs. Output Current, VOUT = 5.2V

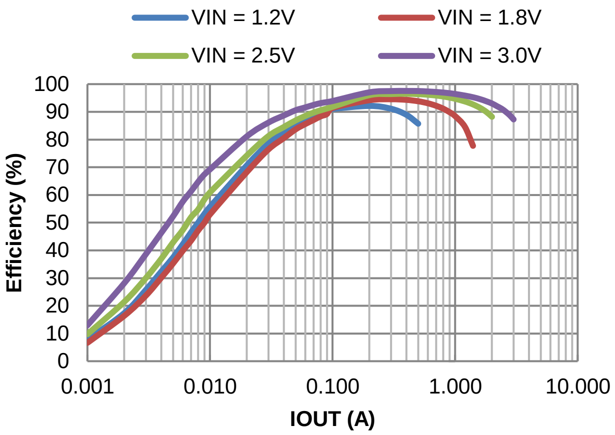

Figure 42. Efficiency vs. Output Current, VOUT = 3.3V

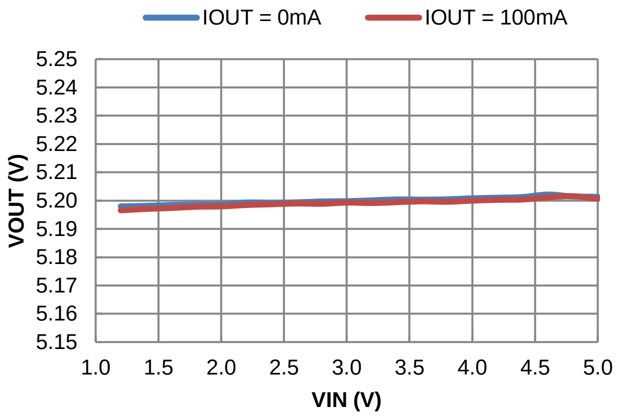

Figure 43. Line Regulation

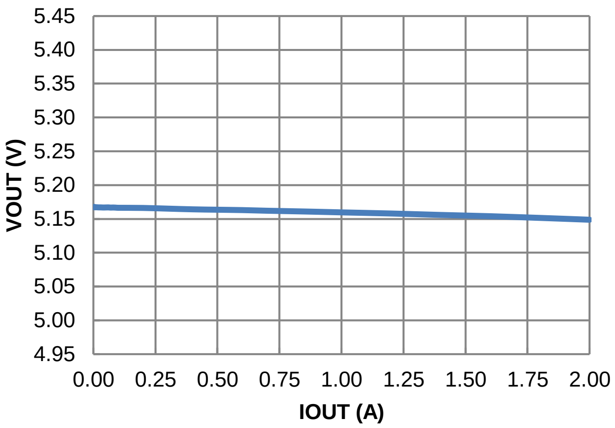

Figure 44. Load Regulation

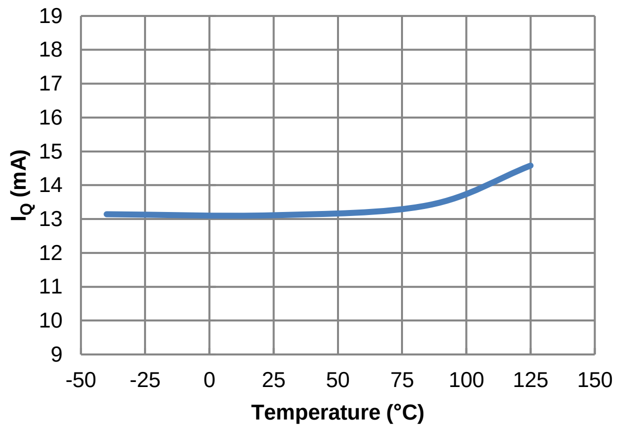

Figure 45. I_Q vs. Temperature, V_{EN} = V_{MODE} = VIN, R1 = 1.05MΩ, R2 = 200kΩ

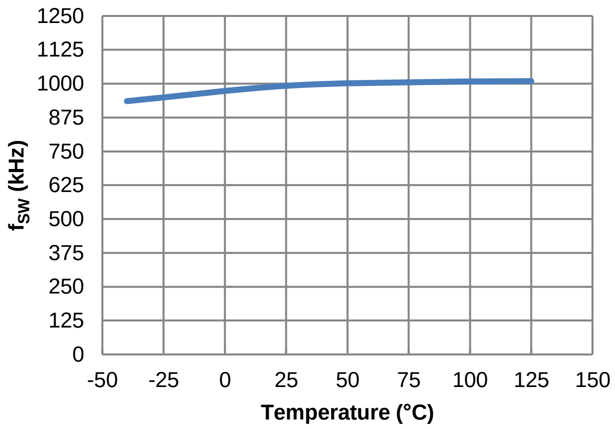

Figure 46. f_{SW} vs. Temperature, IOUT = 0A

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Typical Performance Characteristics (AP72250 @T_A = +25°C, VIN = 3.6V, VOUT = 5.2V, MODE = PWM, BOM = Table 1, unless otherwise specified.) (continued)

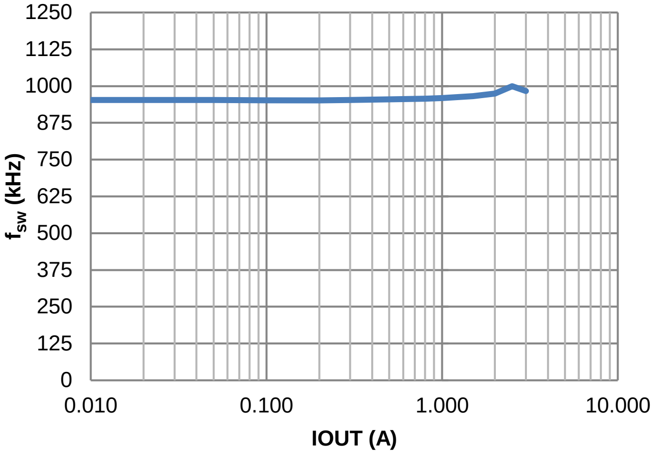

Figure 47. f_{SW} vs. Load

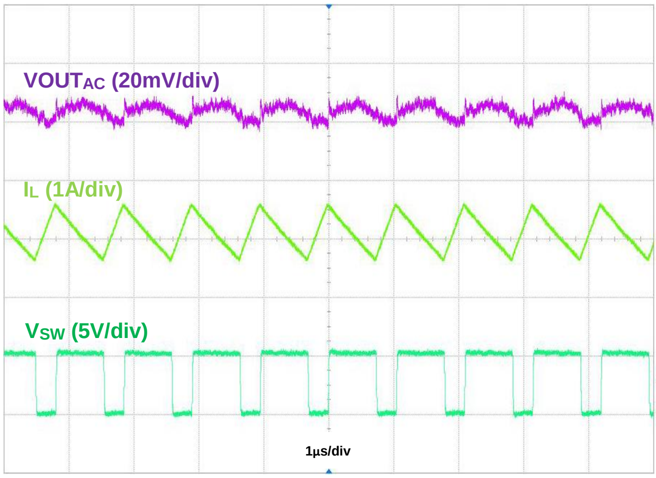

Figure 48. Output Voltage Ripple, VOUT = 5.2V, IOUT = 50mA

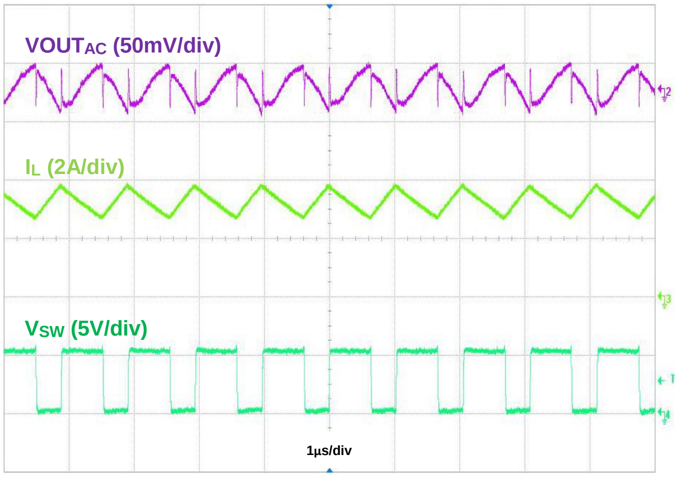

Figure 49. Output Voltage Ripple, VOUT = 5.2V, IOUT = 2A

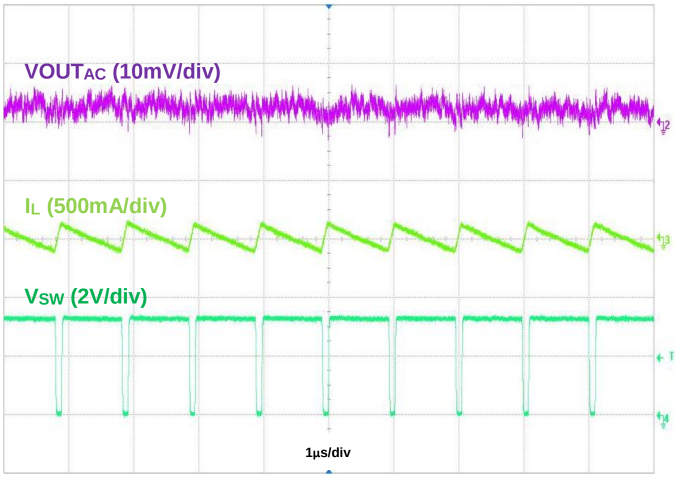

Figure 50. Output Voltage Ripple, VIN = 3V, VOUT = 3.3V, IOUT = 50mA

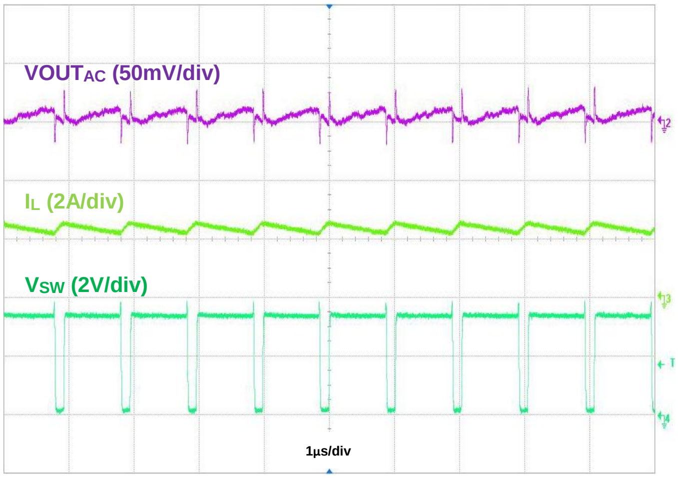

Figure 51. Output Voltage Ripple, VIN = 3V, VOUT = 3.3V, IOUT = 2A

Downloaded from Arrow.com.

Typical Performance Characteristics (AP72250 @T_A = +25°C, VIN = 3.6V, VOUT = 5.2V, MODE = PWM, BOM = Table 1, unless otherwise specified.) (continued)

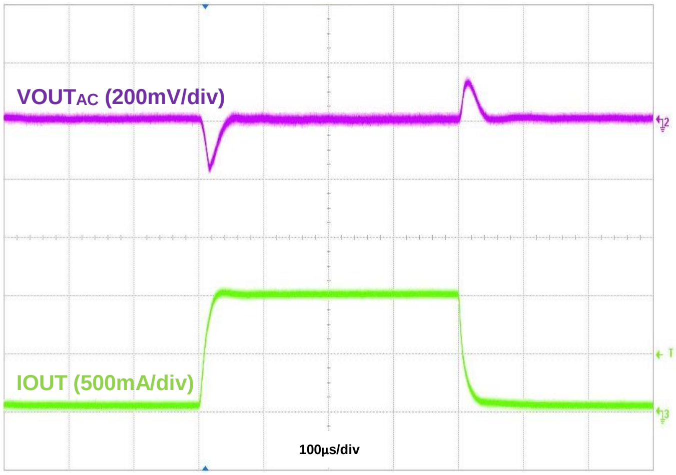

Figure 52. Load Transient, IOUT = 50mA to 1A to 50mA

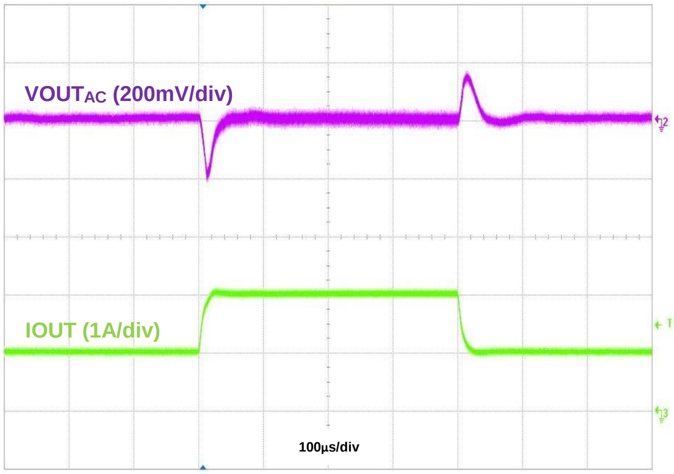

Figure 53. Load Transient, IOUT = 1A to 2A to 1A

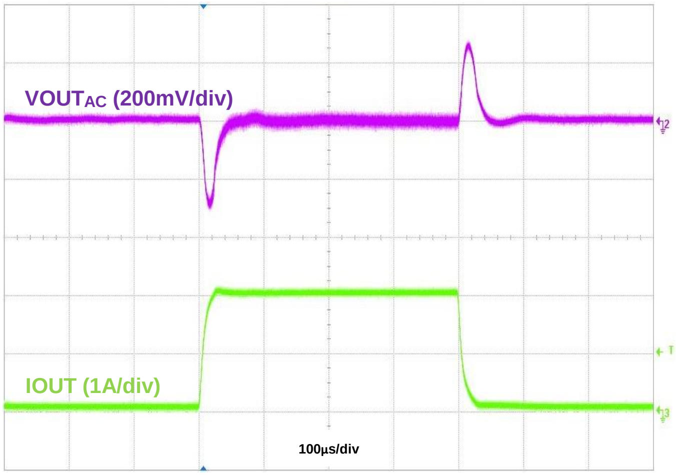

Figure 54. Load Transient, IOUT = 50mA to 2A to 50mA

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Application Information

1 Pulse Width Modulation (PWM) Operation

The AP72250 device is a 0.6V-to-5.5V input, fully integrated synchronous boost converter with 1.0V minimum startup. Refer to the block diagram in Figure 3. The device employs fixed-frequency peak current mode control. The internal clock's rising edge initiates turning on the integrated low-side power MOSFET, Q1, for each cycle. When Q1 is on, the inductor current rises linearly. The current across Q1 is sensed and converted to a voltage with a ratio of R_T via the CSA block. The CSA output is combined with an internal slope compensation, S_E, resulting in V_{SUM}. When V_{SUM} rises higher than the COMP node, the device turns off Q1 and turns on the high-side power MOSFET, Q2. The inductor current decreases when Q2 is on and charges the output capacitor. On the rising edge of next clock cycle, Q2 turns off and Q1 turns on. This sequence repeats every clock cycle.

The error amplifier generates the COMP voltage by comparing the voltage on the FB pin with an internal 0.8V reference. An increase in load current causes the feedback voltage to drop. The error amplifier thus raises the COMP voltage until the average inductor current matches the increased load current. This feedback loop regulates the output voltage. The internal slope compensation circuitry prevents subharmonic oscillation when the duty cycle is greater than 50% for peak current mode control.

When the input voltage is above 90% of the output voltage, the AP72250 rapidly and smoothly transits from boost to pass-through mode by keeping the high-side MOSFET, Q2, on.

The peak current mode control, integrated loop compensation network simplifies the AP72250 footprint as well as minimizing the external component count.

Connecting the MODE pin to VIN sets the AP72250 to operate in Forced PWM Mode regardless of output load.

2 Pulse Frequency Modulation (PFM) and Ultrasonic Mode (USM) Operation

AP72250 enters PFM operation during light load conditions when the MODE pin is tied to GND. In heavy load conditions, the AP72250 operates in PWM mode. As the load current decreases, the internal COMP node voltage also decreases. At a certain limit, if the load current is low enough, the COMP node voltage is clamped and is prevented from decreasing any further. The voltage at which COMP is clamped corresponds to the 1.5A PFM peak inductor current limit. As the load current approaches zero, the AP72250 enters PFM mode to increase the converter power efficiency at light load conditions. When the inductor current decreases to 30mA, zero cross detection circuitry on the high-side power MOSFET, Q2, forces it off. The boost converter does not sink current from the output when the output load is light and while the device is in PFM. Since the AP72250 works in PFM during light load conditions, it can achieve power efficiency of up to 89% at a 5mA load condition.

AP72250 enters USM operation during light load conditions when the MODE pin is left floating. USM is similar to PFM operation but with one key difference. Unlike in PFM, operating in USM limits the switching frequency of the device from falling below 20.5kHz. This prevents the device from switching in the audible frequency range. When the regulator detects that no switching has occurred within the last 37μs, it turns on Q2 for a fixed amount of time (~50ns) to induce a negative inductor current and force switching action on the SW pin.

The quiescent current of AP72250 is 20μA typical under a no-load, non-switching condition.

3 Enable

When the EN voltage falls below its logic low threshold (maximum 0.2V, falling), the internal SS voltage discharges to ground and device operation disables. When disabled, the device shutdown supply current is only 2.5μA. When applying a voltage greater than the EN logic high threshold (minimum 0.90V, rising when VIN > 1.6V), the AP72250 enables all functions and the device initiates the soft-start phase. Alternatively, leave the EN pin floating to allow the AP72250 to soft-start automatically when VIN > 1V. During the soft-start period when VOUT < VIN, the inductor current is regulated at 250mA. Therefore, the load current should not exceed 100mA during startup.

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Application Information (continued)

4 Power-Good (PG) Indicator

The PG pin of AP72250 is an open-drain output that is actively held low during the soft-start period until the output voltage reaches 80% of its target value. When the output voltage is outside of its regulation by +20% or -25%, PG pulls low until the output returns within +15% or -20% of its set value. The PG rising edge transition is delayed by 2ms while its falling edge transition is delayed by 5µs to prevent false triggering. The PG pin is connected to an internal VCC through an internal 5MΩ pull-up resistor.

5 Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to protect the IC from insufficient input voltages. The AP72250 disables if the input voltage falls below 0.57V. In this UVLO event, both the high-side and low-side power MOSFETs turn off and the 200Ω active discharge enables to discharge the output voltage to ground.

6 Overcurrent Protection (OCP) and Short-Circuit Protect (SCP)

The AP72250 has cycle-by-cycle peak current limit protection by sensing the current through the internal low-side power MOSFET, Q1. While Q1 is on, the internal sensing circuitry monitors its conduction current. The overcurrent limit has a corresponding voltage limit, V_{LIMIT}. When the voltage between PGND and SW is lower than V_{LIMIT} due to excessive current through Q1, the OCP triggers, and the controller turns off Q1. During this time, both Q1 and Q2 remain off. A new switching cycle begins only when the voltage between PGND and SW rises above V_{LIMIT}.

If Q1 consistently hits the peak current limit for seven switching cycles and VOUT < VIN, then the boost converter enters short-circuit protection. The high-side power MOSFET switches its body diode connection to VIN to protect the device from having a direct path between VIN and VOUT through the body diode. In the short-circuit condition, the inductor current is regulated at 250mA to prevent excessive power dissipation.

7 Reverse (Negative) Current Protection

During PWM operation, a reverse current comparator on the high-side power MOSFET, Q2, monitors the current entering from VOUT. When this current exceeds 2A (typical), Q2 turns off for the remainder of the switching cycle. This feature protects the boost converter from excessive reverse current if the boost output voltage is held above its target voltage by an external source.

8 Output Active Discharge

AP72250 provides an internal 200Ω resistor for the output active discharge function. The internal resistor discharges the energy stored in the output capacitor to PGND whenever the regulator is disabled or encounters thermal shutdown. The internal discharge resistor disconnects from the output when the regulator is enabled and in normal operating conditions.

9 Thermal Shutdown (TSD)

If the junction temperature of the device reaches the thermal shutdown limit of +150°C, the AP72250 shuts down both its high-side and low-side power MOSFETs and triggers the output active discharge. When the junction temperature reduces to the required level (+130°C typical), the device initiates a normal power-up cycle with soft-start.

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Application Information (continued)

10 Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$\mathbf{T_{RISE} = PD \cdot (\theta_{JA})} \qquad \textbf{Eq. 1}$$

Where:

- PD is the power dissipated by the regulator
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature

The junction temperature, T_J, is given by:

$$\mathbf{T_J = T_A + T_{RISE}} \qquad \textbf{Eq. 2}$$

Where:

- T_A is the ambient temperature of the environment

For the X1-WLB1713-12 package, the θ_{JA} is 90°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of +125°C when considering the thermal design. Figure 55 shows a typical derating curve versus ambient temperature.

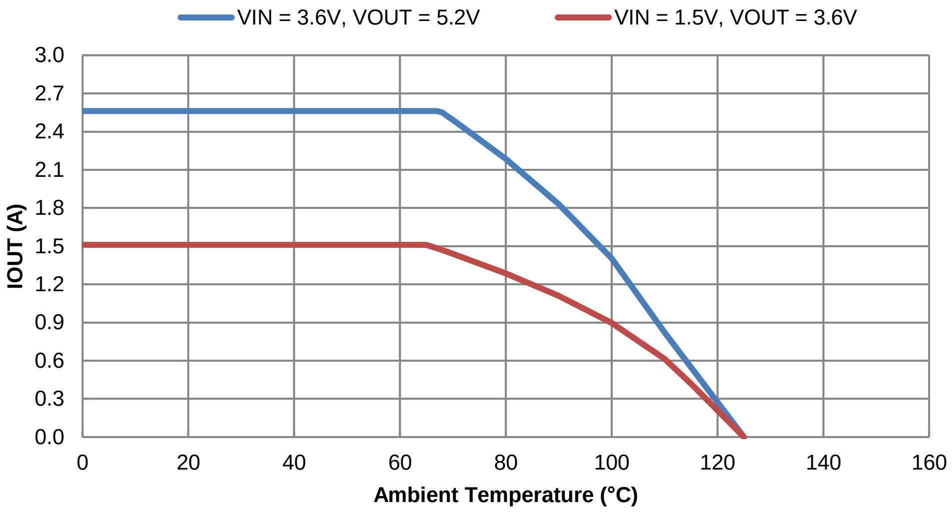

Figure 55. Output Current Derating Curve vs. Ambient Temperature

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Application Information (continued)

11 Setting the Output Voltage

The AP72250 has adjustable output voltages starting from 0.8V using an external resistive divider. The resistor values of the feedback network are selected based on a design trade-off between efficiency and output voltage accuracy. There is less current consumption in the feedback network for high resistor values, which improves efficiency at light loads. However, values too high cause the device to be more susceptible to noise affecting its output voltage accuracy. R2 can be determined by the following equation:

$$\mathbf{R2} = \frac{\mathbf{0.8 \cdot R1}}{\mathbf{VOUT - 0.8V}} \qquad \textbf{Eq. 3}$$

Table 1 shows a list of recommended component selections for common AP72250 output voltages referencing Figure 1.

Table 1. Recommended Component Selections

AP72250					
Output Voltage (V)	**R1 (kΩ)**	**R2 (kΩ)**	**L (µH)**	**C1 (µF)**	**C2 (µF)**
1.8	100.0	80.6	0.47	10	2 x 22
2.5	100.0	32.4	0.68	10	2 x 22
3.3	100.0	31.6	1.00	10	2 x 22
5.0	100.0	19.1	1.00	10	2 x 22
5.2	100.0	18.2	1.00	10	2 x 22

12 Inductor

Calculating the inductor value is a critical factor in designing a boost converter. For most designs, the following equation can be used to calculate the inductor value:

$$\mathbf{L} = \frac{\mathbf{VIN \cdot (VOUT - VIN)}}{\mathbf{VOUT \cdot \Delta I_L \cdot f_{SW}}} \qquad \textbf{Eq. 4}$$

Where:

- ΔI_L is the inductor current ripple
- f_{SW} is the boost converter switching frequency

For AP72250, choose ΔI_L to be 30% to 50% of the peak inductor current of 4.5A.

The inductor peak current is calculated by:

$$\mathbf{I_{L_{PEAK}}} = \mathbf{I_{LOAD}} \cdot \left(\frac{\mathbf{VOUT}}{\mathbf{VIN}}\right) + \frac{\mathbf{\Delta I_L}}{\mathbf{2}} \qquad \textbf{Eq. 5}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal power MOSFETs. Therefore, choosing an inductor with the appropriate saturation current rating is important. For most applications, it is recommended to select an inductor of approximately 1.0µH with a DC current rating of at least 35% higher than the maximum peak current. For highest efficiency, the inductor's DC resistance should be less than 50mΩ. Use a larger inductance for improved efficiency under light load conditions but beware of the "right-half-plane zero" frequency, F_{RHPZ}, which is:

$$\mathbf{F_{RHPZ}} = \frac{\mathbf{VIN^2}}{\mathbf{2 \cdot \pi \cdot IOUT \cdot VOUT \cdot L}} \qquad \textbf{Eq. 6}$$

The right-half-plane zero frequency can cause loop stability so it is ideal to have it be as high as possible. Therefore, for applications using a low VIN and a high VOUT, the recommendation is to decrease the inductance, the output current, or both, to avoid any possible stability issues caused by F_{RHPZ}.

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Application Information (continued)

13 Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. While a 10µF input capacitor is sufficient for most applications, larger values may be used to reduce input ripple without limitations. It is recommended to use at least X5R or X7R ceramic input capacitors.

14 Output Capacitor

The output capacitor must sustain the ripple current produced during the off-time of the switching period. It must have a low ESR to minimize power dissipation due to the RMS output current.

The RMS current rating of the output capacitor is a critical parameter and must be higher than the RMS output current. As a rule of thumb, select an output capacitor with a RMS current rating greater than 2.5A.

Due to large dI/dt through the output capacitor, electrolytic, or ceramic capacitors with low ESR should be used. If using a tantalum capacitor, it must be surge protected or else capacitor failure could occur. For most applications, a total capacitance of 2 x 22µF using ceramic capacitors is sufficient.

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady-state and enters maximum duty cycle to supply more current to the load. However, the inductor limits the change in increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady-state and sets the on-time to minimum to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

The ESR of the output capacitor dominates the output voltage ripple. The amount of output voltage ripple can be calculated by:

$$\mathbf{VOUT_{Ripple} = I_{L_{PEAK}} \cdot (ESR)} \qquad \textbf{Eq. 7}$$

Where:

- ESR is the equivalent series resistance of the output capacitor

An output capacitor with large capacitance and low ESR is the best option. For most applications, using 2 x 22µF to 5 x 22µF, X5R or X7R ceramic capacitors are sufficient.

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Layout

PCB Layout

1. The AP72250 works at 4.7A peak load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and PGND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as closely across VOUT and PGND as possible.
5. Connect the Analog Ground (GND) to a large, low-noise ground plane at the top or at an intermediate layer of the PCB and away from the switching current path of PGND.
6. Place the feedback components as close to FB as possible.
7. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
8. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
9. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
10. See Figure 56 for more details.

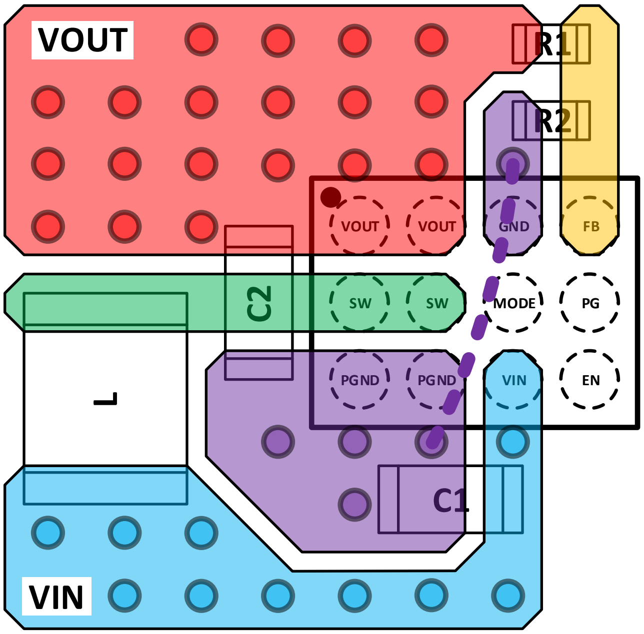

Figure 56. Recommended PCB Layout

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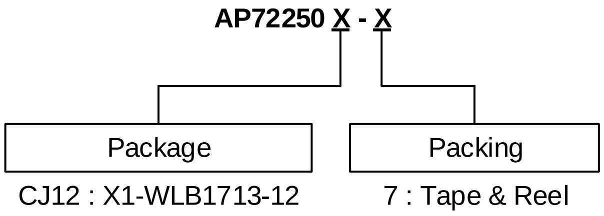
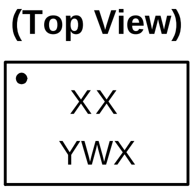
Ordering Information



Part Number	Package	Package Code	Packing	
			Qty.	Carrier
AP72250CJ12-7	X1-WLB1713-12	CJ12	3,000	7” Tape and Reel

Marking Information

X1-WLB1713-12



XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~ z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
AP72250CJ12-7	X1-WLB1713-12	F5

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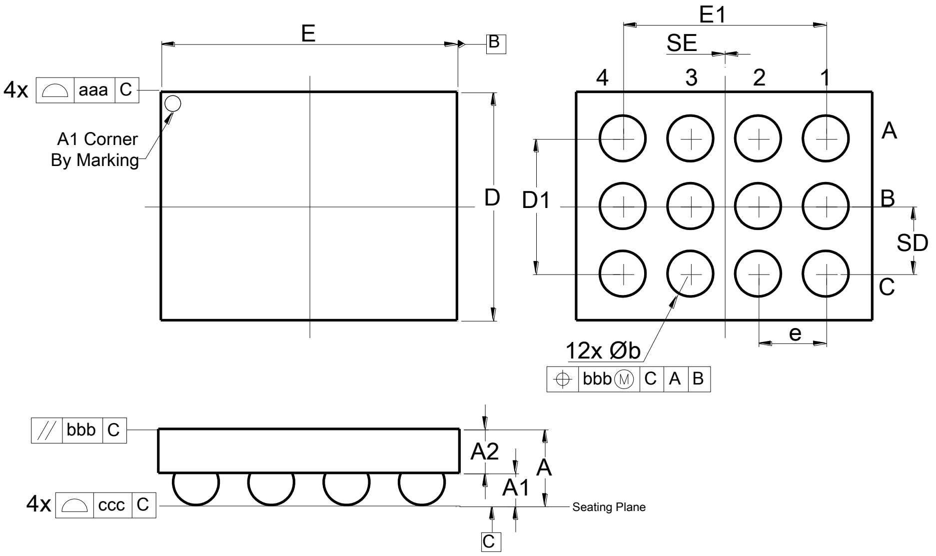
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-WLB1713-12

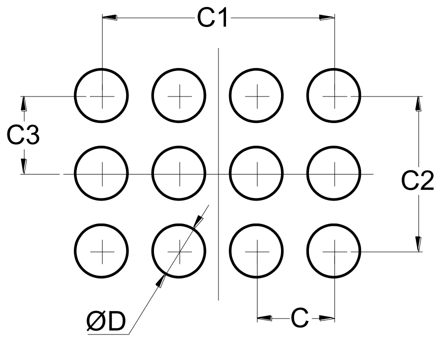


X1-WLB1713-12			
Dim	**Min**	**Max**	**Typ**
A	0.400	0.500	0.450
A1	0.170	0.210	0.190
A2	0.210	0.310	0.260
b	0.240	0.300	0.270
D	1.325	1.375	1.350
D1	0.750	0.850	0.800
E	1.725	1.775	1.750
E1	1.150	1.250	1.200
e	0.400 BSC		
SD	0.400 BSC		
SE	0.000 BSC		
aaa	0.10		
bbb	0.10		
ccc	0.05		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-WLB1713-12



Dimensions	Value (in mm)
C	0.400
C1	1.200
C2	0.800
C3	0.400
D	0.270

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: SnAgCu Balls, Solderable per MIL-STD-202, Method 208 ⓔ1
- Weight: 0.002 grams (Approximate)

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