Features

- ➔ Operation power supply voltage from 2.3V to 5.5V
- ➔ 16-bit I/O pins which can be programmed as Input or Output
- ➔ 5V tolerant I/Os
- ➔ Polarity inversion register
- ➔ Active LOW interrupt output
- ➔ Low current consumption
- ➔ 0Hz to 400KHz clock frequency
- ➔ Noise filter on SCL/SDA inputs
- ➔ Power-on reset
- ➔ ESD protection (4KV HBM and 1KV CDM)
- ➔ Latch-up tested (exceeds 100mA)
- ➔ Offered in two different packages: TSSOP-24 and TQFN 4x4-24

Description

The PI4IOE5V9555 is an I^2C-bus I/O expander that provides 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I^2C-bus/SMBus applications. It includes the features such as higher driving capability, 5V tolerance, lower power supply, individual I/O configuration, and smaller packaging. It provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PI4IOE5V9555 consists of two 8-bit configuration registers to configure the I/Os as either inputs or outputs, and two 8-bit polarity registers to change the polarity of the input port register data. The data for each input or output is kept in the corresponding Input port or Output port register. All registers can be read by the system master.

The PI4IOE5V9555 open-drain interrupt output is activated and indicate to the system when any input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three input pins (A0, A1, A2) can select I^2C-bus address of PI4IOE5V9555 from the eight preset address. It allows up to eight PI4IOE5V9555 to share the same I^2C-bus/SMBus and provide maximum 128 I/Os.

Pin Configuration

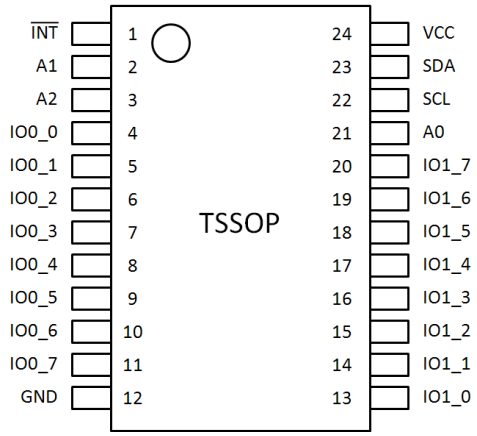


Figure 1: TSSOP-24 (Top View)

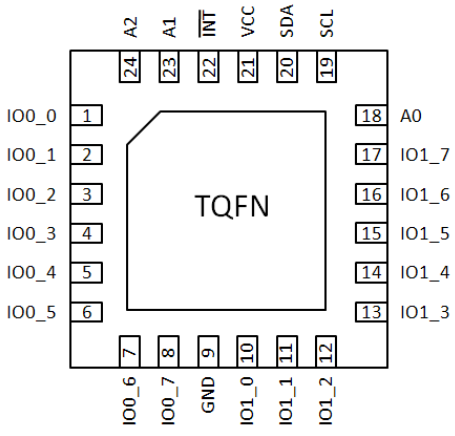


Figure 2: TQFN 4x4-24 (Top View)

Pin Description

Table 1: Pin Description

Pin		Name	Type	Description
TSSOP24	TQFN24			
1	22	$\overline{INT}$	O	Interrupt input (open-drain)
2	23	A1	I	Address input 1
3	24	A2	I	Address input 2
4	1	IO0_0	I/O	Port 0 input/output 0
5	2	IO0_1	I/O	Port 0 input/output 1
6	3	IO0_2	I/O	Port 0 input/output 2
7	4	IO0_3	I/O	Port 0 input/output 3
8	5	IO0_4	I/O	Port 0 input/output 4
9	6	IO0_5	I/O	Port 0 input/output 5
10	7	IO0_6	I/O	Port 0 input/output 6
11	8	IO0_7	I/O	Port 0 input/output 7
12	9	GND	G	Ground
13	10	IO1_0	I/O	Port 1 input/output 0
14	11	IO1_1	I/O	Port 1 input/output 1
15	12	IO1_2	I/O	Port 1 input/output 2
16	13	IO1_3	I/O	Port 1 input/output 3
17	14	IO1_4	I/O	Port 1 input/output 4
18	15	IO1_5	I/O	Port 1 input/output 5
19	16	IO1_6	I/O	Port 1 input/output 6
20	17	IO1_7	I/O	Port 1 input/output 7
21	18	A0	I	Address input 0
22	19	SCL	I	Serial clock line input
23	20	SDA	I	Serial data line open-drain
24	21	VCC	P	Supply voltage

* I = Input; O = Output; P = Power; G = Ground

Maximum Ratings

Power supply	-0.5V to +6.0V
Voltage on an I/O pin	GND-0.5V to +6.0V
Input current	±20mA
Output current on an I/O pin	±50mA
Supply current	160mA
Ground supply current	200mA
Total power dissipation	200mW
Operation temperature	-40~85℃
Storage temperature	-65~150℃
Maximum Junction temperature ,T j(max)	125℃

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Static characteristics

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb= -40 ℃ to +85 ℃; unless otherwise specified.

Table 2: Static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
VCC	Supply voltage		2.3	-	5.5	V
I_{CC}	Supply current	Operating mode; VCC = 5.5 V; no load; f_{SCL}= 100 kHz	-	135	200	µA
I_{stb}	Standby current	Standby mode; VCC = 5.5 V; no load; V_I = GND; f_{SCL}= 0 kHz; I/O = inputs	-	1.1	1.5	mA
		Standby mode; VCC = 5.5 V; no load; V_I = VCC; f_{SCL}= 0 kHz; I/O = inputs	-	0.25	1	µA
V_{POR}	Power-on reset voltage[1]		-	1.16	1.41	V
Input SCL, input/output SDA						
V_{IL}	Low level input voltage		-0.5	-	+0.3VCC	V
V_{IH}	High level input voltage		0.7VCC	-	5.5	V
I_{OL}	Low level output current	V_{OL}=0.4V	3	-	-	mA
I_L	Leakage current	V_I=VCC=GND	-1	-	1	µA
C_i	Input capacitance	V_I =GND	-	6	10	pF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I/Os						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_{OL}	Low level output current	VCC = 2.3 V to 5.5 V; V_{OL} = 0.5 V[2]	8	-	20	mA
		VCC = 2.3 V to 5.5 V; V_{OL} = 0.7 V[2]	10	-	24	mA
V_{OH}	High level output voltage	I_{OH}=-8mA;VCC=2.3V[3]	1.8	-	-	V
		I_{OH}=-10mA;VCC=2.3V[3]	1.7	-	-	V
		I_{OH}=-8mA;VCC=3.0V[3]	2.6	-	-	V
		I_{OH}=-10mA;VCC=3.0V[3]	2.5	-	-	V
		I_{OH}=-8mA;VCC=4.75V[3]	4.1	-	-	V
		I_{OH}=-10mA;VCC=4.75V[3]	4.0	-	-	V
I_{LIH}	High level input leakage current	VCC=5.5V; V_I=VCC	-	-	1	µA
I_{LIL}	Low level input leakage current	VCC=5.5V; V_I=GND	-	-	-100	µA
C_i	Input capacitance		-	3.7	10	pF
C_o	Output capacitance		-	3.7	10	pF
Interrupt $\overline{INT}$						
I_{OL}	Low level output current	V_{OL}=0.4V	3	-	-	mA
Select inputs A0,A1,A2						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_L	Input leakage current		-1		1	µA

Note:
[1]: VCC must be lowered to 0.2 V for at least 20 us in order to reset part.
[2]: Each I/O must be externally limited to a maximum of 25 mA and each octal (IO0_0 to IO0_7 and IO1_0 to IO1_7) must be limited to a maximum current of 100 mA for a device total of 200 mA.
[3]: The total current sourced by all I/Os must be limited to 160 mA.

Dynamic Characteristics

Table 3: Dynamic characteristics

Symbol	Parameter	Test Conditions	Standard mode I^2C		Fast mode I^2C		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{VD;ACK}$[1]	data valid acknowledge time		-	3.45	-	0.9	µs
$t_{HD;DAT}$[2]	data hold time		0	-	0	-	ns
$t_{VD;DAT}$	data valid time		-	3.45	-	0.9	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals		-	300	-	300	ns
t_r	rise time of both SDA and SCL signals		-	1000	-	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
Port timing							
$t_{v(Q)}$	Data output valid time[3]		-	200	-	200	ns
$t_{su(D)}$	Data input set-up time		150	-	150	-	ns
$T_{h(D)}$	Data input hold time		1	-	1	-	µs
Interrupt timing							
$t_{v(INT)}$	Valid time on pin $\overline{INT}$		-	4	-	4	µs
$T_{rst(INT)}$	Reset time on pin $\overline{INT}$		-	4	-	4	µs

Note:
[1]: $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
[2]: $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
[3]: $t_{v(Q)}$measured from 0.7VCC on SCL to 50% I/O output.

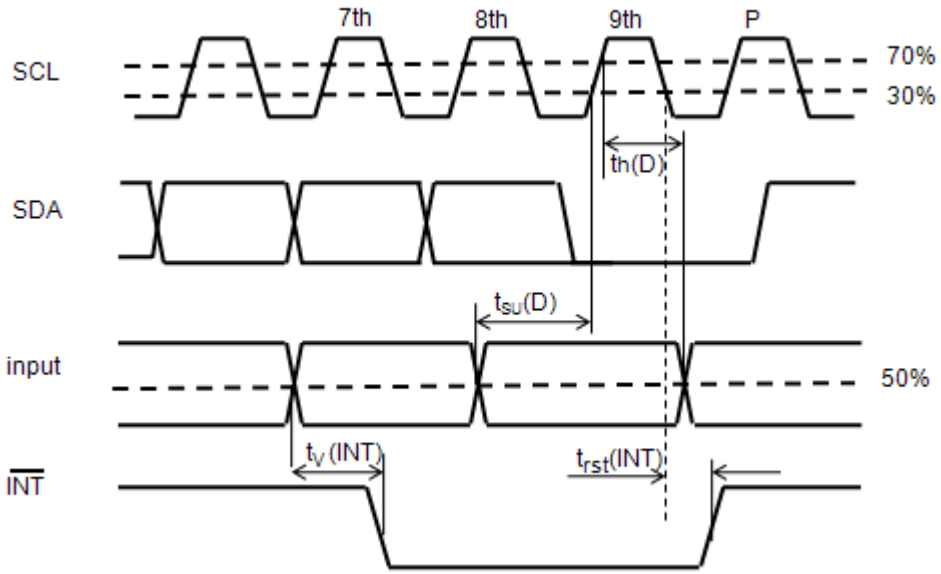
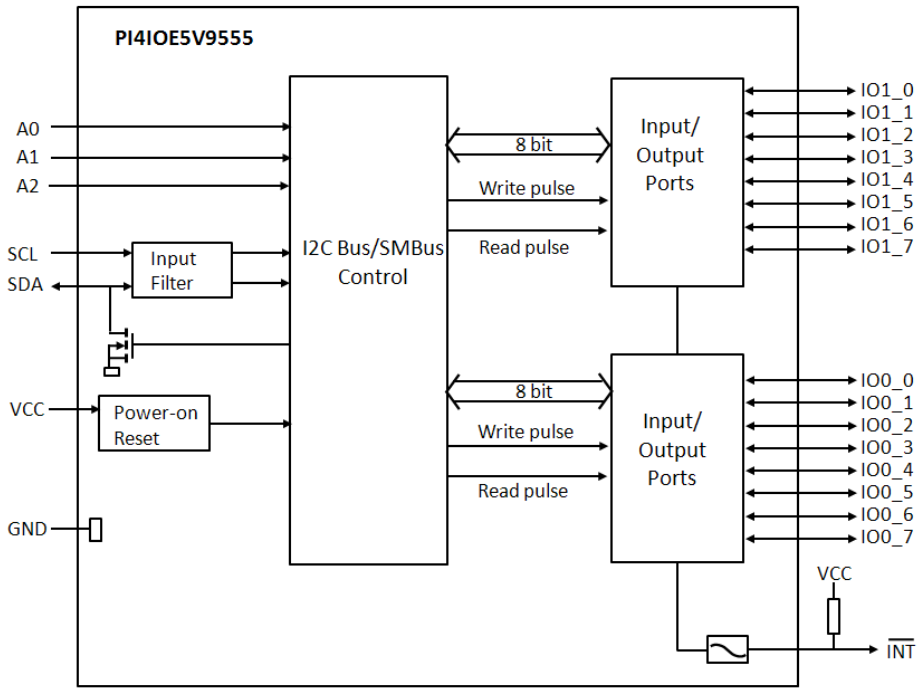


Figure 3: timing parameters for INT signal

PI4IOE5V9555 Block Diagram

Figure 4: Block diagram



Note: All I/Os are set to inputs at reset.

Details Description

a. Device address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	0	1	0	0	A2	A1	A0	R/W

Note: Read "1", Write "0"

b. Registers

i. Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 4: Command byte

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity inversion port 0
5	Polarity inversion port 1
6	Configuration port 0
7	Configuration port 1

ii. Register 0 and 1: input port registers

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

Table 5: Input port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 6: Input port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

iii. Register 2 and 3:Output port registers

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 7: Output port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 8: Output port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

iv. Register 4 and 5: Polarity inversion registers

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 9: Polarity Inversion port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 10: Polarity Inversion port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

v. Register 6 and 7: Configuration registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high value resistor tied to VCC at each pin. At reset, the IOs are configured as inputs with a pull-up to VCC.

Table 11: Configuration port 0 register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 12: Configuration port 1 register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

c. Power-on reset

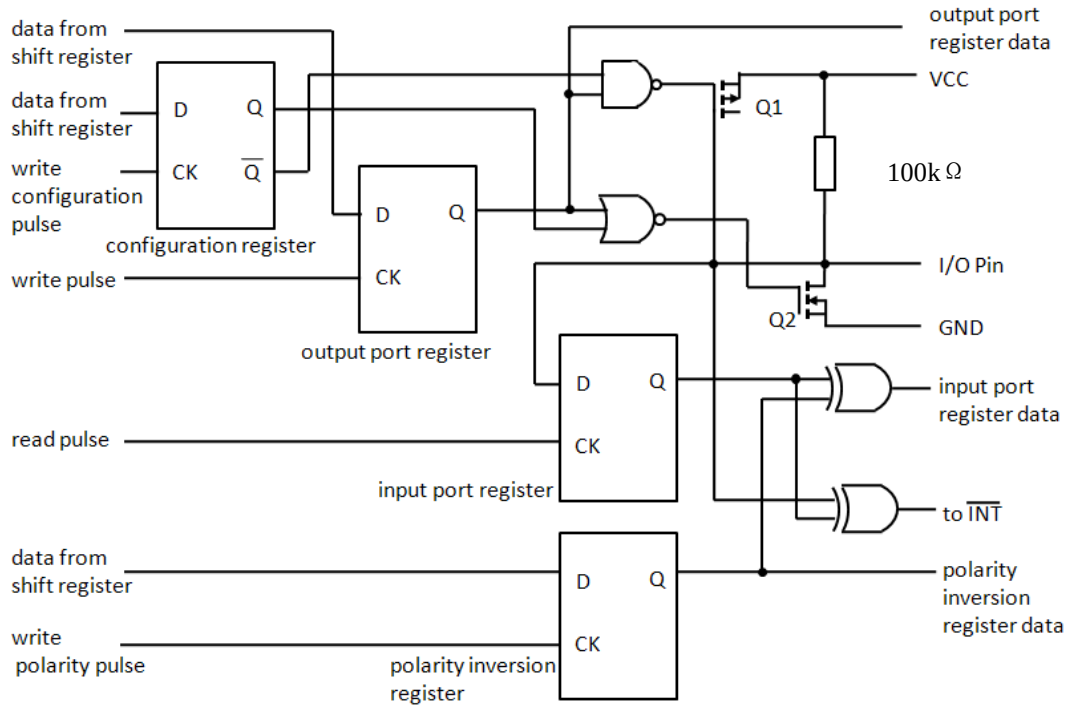
When power is applied to VCC, an internal power-on reset holds the PI4IOE5V9555 in a reset condition until VCC has reached V_{POR}. At that point, the reset condition is released and thePI4IOE5V9555 registers and SMBus state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above V_{POR}. However, when it is required to reset the part by lowering the power supply, it is necessary to lower it below 0.2 V.

d. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up to VCC. The input voltage may be raised above VCC to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either VCC or GND.

Figure 5: Simplified schematic of I/Os



After power-on reset, all registers return to default values.

e. Bus Transaction

i. Writing to the port registers

Data is transmitted to the PI4IOE5V9555 by sending the device address and setting the least significant bit to a logic 0. The command byte is sent after the address and determines which register will receive the data following the command byte.
The eight registers within the PI4IOE5V9555 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair. For example, if the first byte is sent to Output Port 1 (register 3), the next byte will be stored in Output Port 0 (register 2).There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

Figure 6: Write to output registers

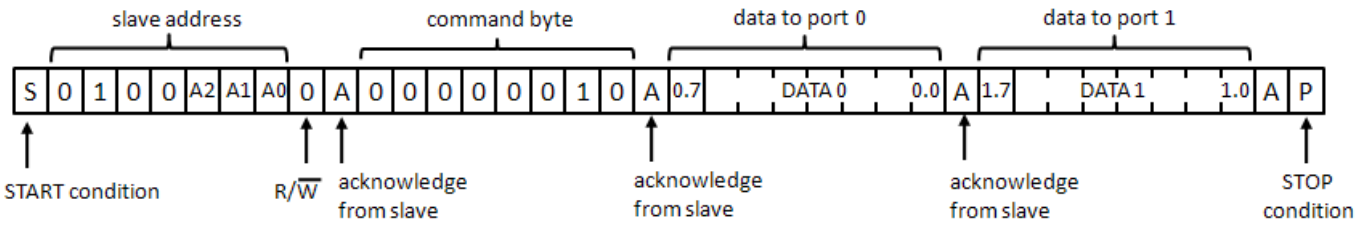
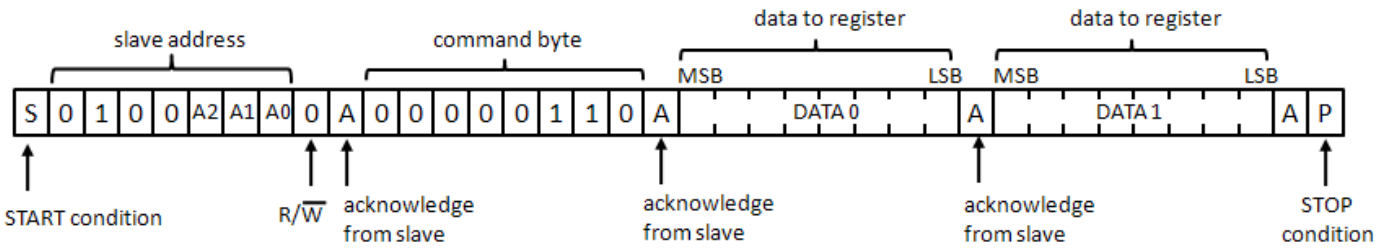


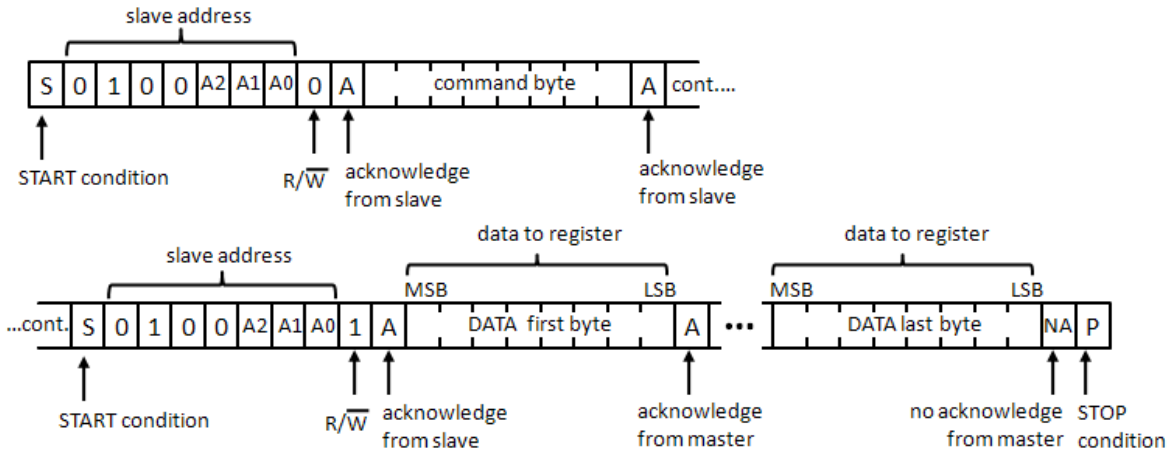
Figure 7: Write to configuration registers



ii. Reading the port registers

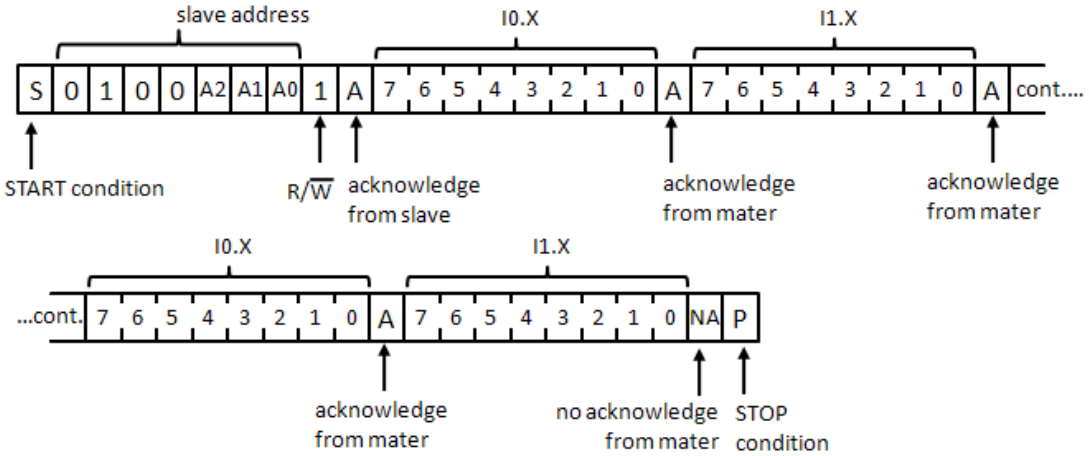
In order to read data from the PI4IOE5V9555, the bus master must first send the PI4IOE5V9555address with the least significant bit set to a logic 0. The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PI4IOE5V9555. Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.

Figure 8: Read from registers



Note: Transfer can be stopped at any time by a STOP condition.

Figure 9: Read Input port register



Note: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

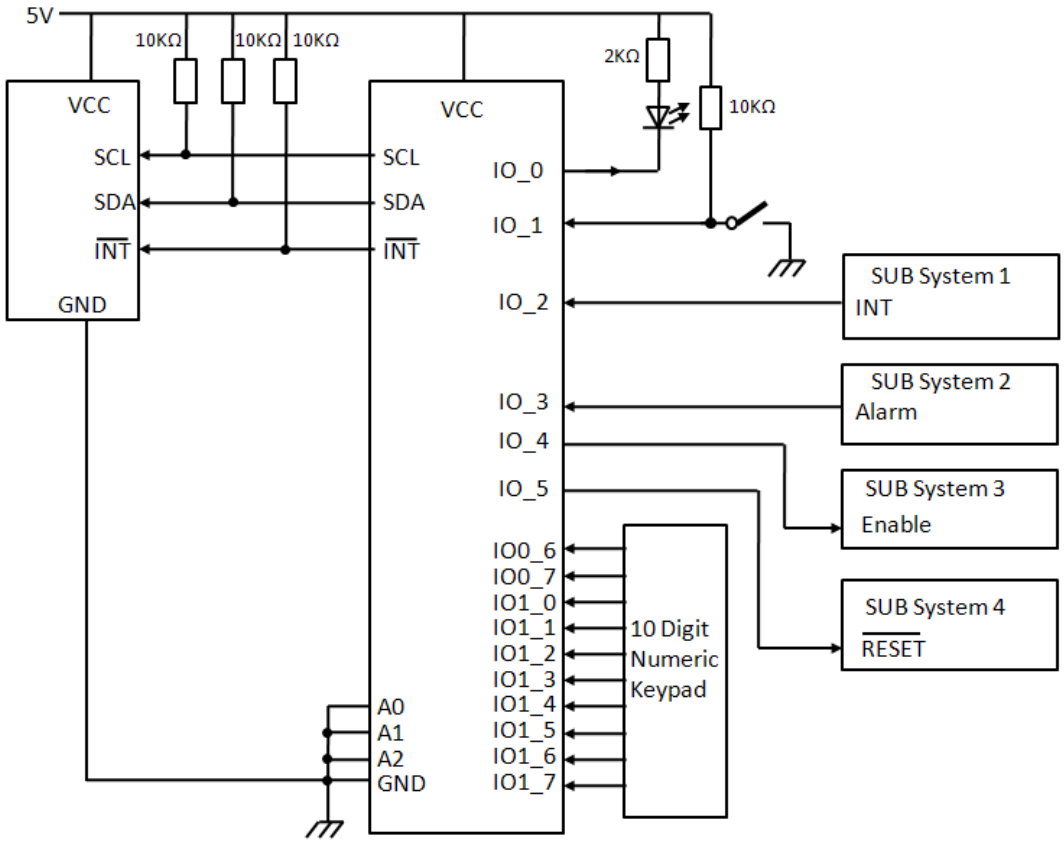
iii. Interrupt output

The open-drain interrupt output is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read. A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Note: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

Application design-in information

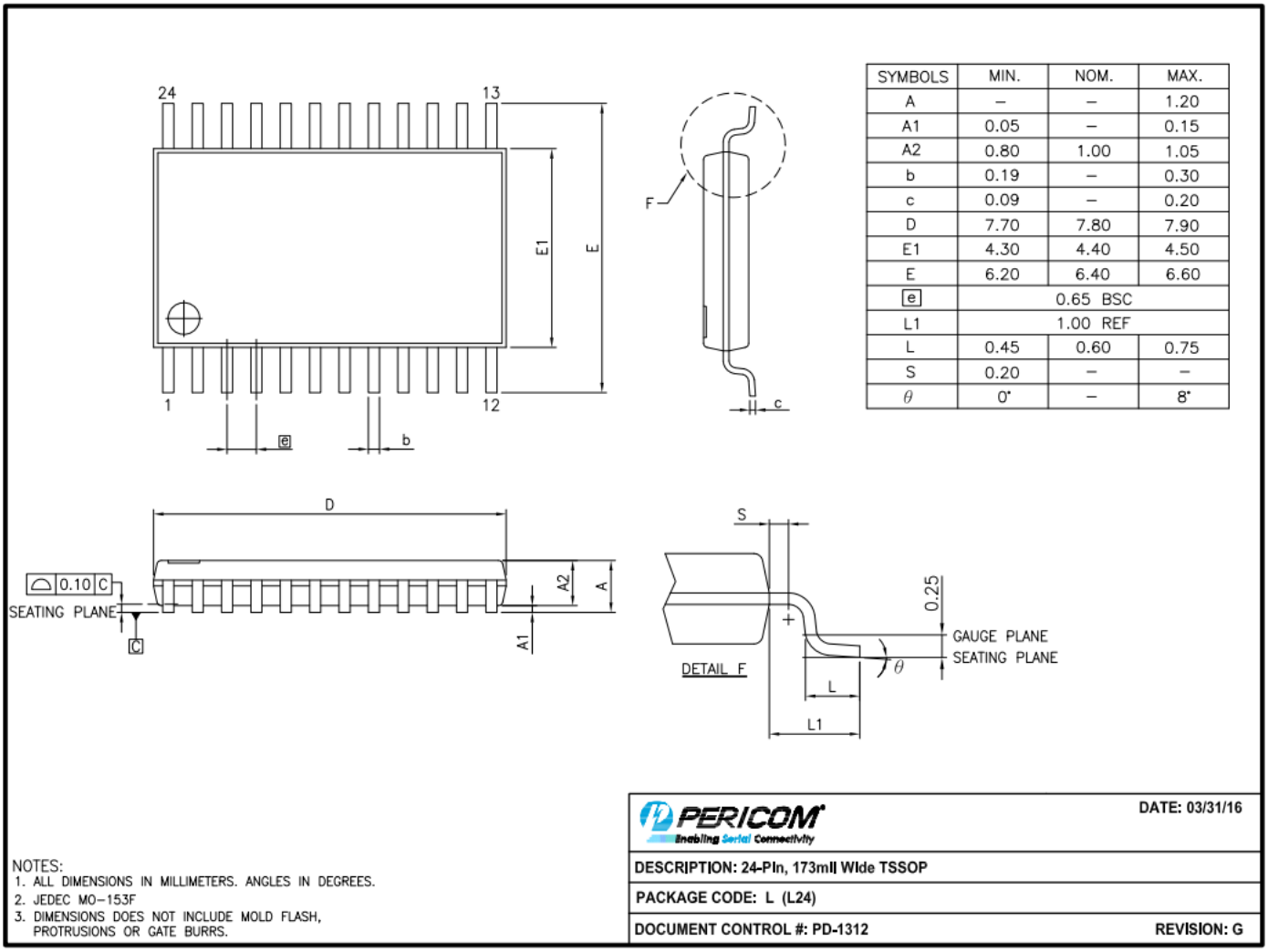
Figure 10: Typical application



Device address configured as 0100 000xb for this example.
IO0_0, IO0_4, IO0_5 configured as outputs.
IO0_1, IO0_2, IO0_3 configured as inputs.
IO0_6, IO0_7, and IO1_0 to IO1_7 configured as inputs.

Mechanical Information

TSSOP-24(L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

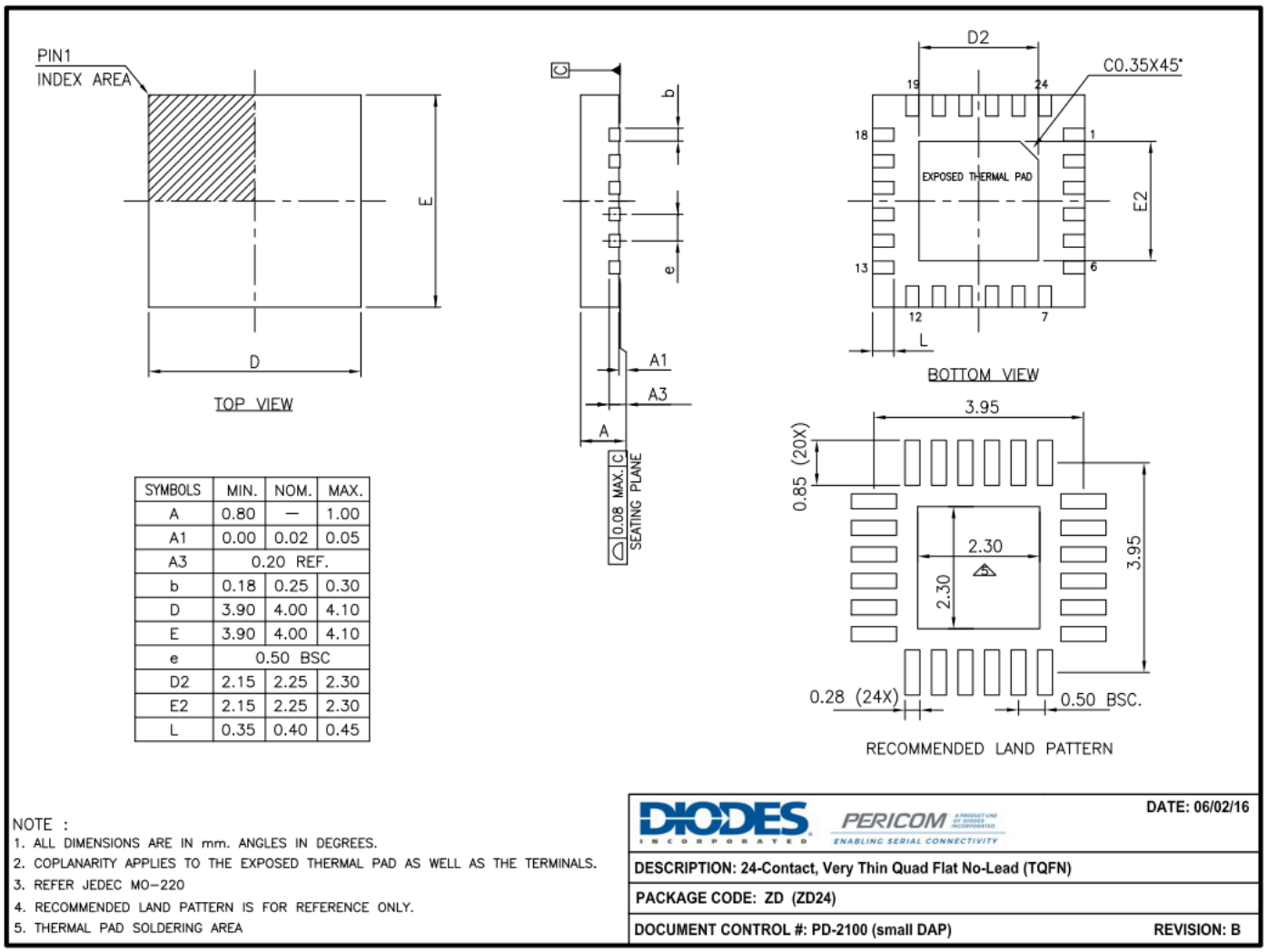
DATE: 03/31/16

DESCRIPTION: 24-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L24)

DOCUMENT CONTROL #: PD-1312 REVISION: G

TQFN 4x4-24(ZD)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	—	1.00
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e		0.50 BSC	
D2	2.15	2.25	2.30
E2	2.15	2.25	2.30
L	0.35	0.40	0.45

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

DATE: 06/02/16

DESCRIPTION: 24-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD (ZD24)

DOCUMENT CONTROL #: PD-2100 (small DAP) REVISION: B

Ordering Information

Part No.	Package Code	Package
PI4IOE5V9555LE	L	24-pin,173mil Wide (TSSOP)
PI4IOE5V9555LEX	L	24-pin,173mil Wide (TSSOP), Tape & Reel
PI4IOE5V9555ZDEX	ZD	24-contact, Very Thin Quad Flat No-Lead (TQFN), Tape & Reel

Note:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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