TDSW0602T

Document Category: Product Specification

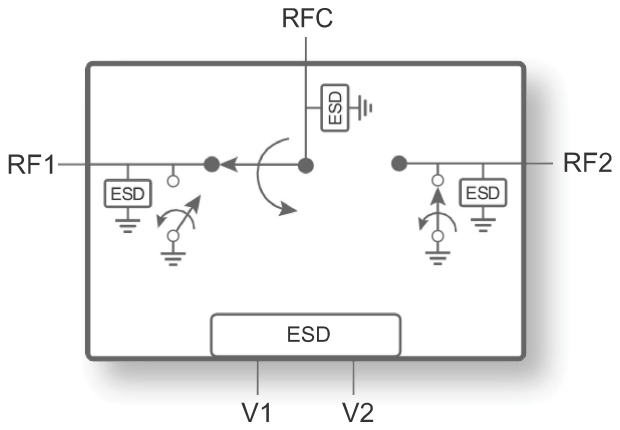
TELEDYNE e2v HIREL ELECTRONICS Everywhereyoulook™

UltraCMOS® SPDT RF Switch, 9 kHz–60 GHz

Features

- Wideband support up to 60 GHz
- Low insertion loss
  - 1.3 dB @ 26.5 GHz
  - 1.7 dB @ 45 GHz
  - 1.9 dB @ 50 GHz
  - 2.7 dB @ 60 GHz
- Fast switching time of 8 ns
- High port to port isolation
  - 41 dB @ 26.5 GHz
  - 38 dB @ 45 GHz
  - 37 dB @ 50 GHz
  - 36 dB @ 60 GHz
- –55°C to +125°C operating temperature range
- High linearity: IIP3 of 48 dBm

Figure 1 • *TDSW0602T Functional Diagram*



Applications

- Harsh industrial applications
- Applications that require extended temperature support in the range of –55°C to +125°C
- Wafer lot accept testing performed per MIL-PRF-38534 Class K

Product Description

The TDSW0602T is a HaRP™ technology-enhanced reflective SPDT RF switch die that supports a wide frequency range from 9 kHz to 60 GHz. It delivers low insertion loss, fast switching time and high isolation in the operating temperature of –55°C to +125°C. It is ideal for applications that require extended temperature support within this range, such as harsh industrial applications. At 50 GHz, the TDSW0602T exhibits 1.9 dB insertion loss and 37 dB isolation. No blocking capacitors are required if dc voltage is not present on the RF ports.

The TDSW0602T is manufactured on UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology.

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Peregrine's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in Table 1 may cause permanent damage. Operation should be restricted to the limits in Table 2. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 1.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for TDSW0602T*

Parameter/Condition	Min	Max	Unit
Control voltage (V1, V2)	–3.6	3.6	V
RF input power (RFC–RFX, 50Ω)		Fig. 2	dBm
Maximum junction temperature		+150	°C
Storage temperature range	–65	+150	°C
ESD voltage HBM(*) All pins RF pins to GND		 600 1000	 V V
Note: * Human body model (MIL-STD 883 Method 3015).			

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Recommended Operating Conditions

Table 2 lists the recommended operating conditions for TDSW0602T. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Recommended Operating Condition for TDSW0602T*

Parameter	Min	Typ	Max	Unit
Control high (V1, V2)	2.7	3.0	3.3	V
Control low (V1, V2)	–3.3	–3.0	–2.7	V
Control current		390		nA
RF input power, CW (RFC–RFX)(1)			Fig. 2	dBm
RF input power, pulsed (RFC–RFX)(2)			Fig. 2	dBm
Operating temperature range	–55	+25	+125	°C

Notes:
1) 100% duty cycle, all bands, 50Ω.
2) Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

Electrical Specifications

Table 3 provides the TDSW0602T key electrical specifications @ +25°C, V1 = +3.0V, V2 = –3.0V or V1 = –3.0V, V2 = +3.0V ($Z_S = Z_L = 50\Omega$), unless otherwise specified.

Table 3 • *TDSW0602T Electrical Specifications*

Parameter	Path	Condition	Min	Typ	Max	Unit
Operation frequency			9 kHz		60 GHz	As shown
Insertion loss	RFC–RFX	100 MHz 100 MHz–26.5 GHz 26.5–45 GHz 45–50 GHz 50–60 GHz		0.9 1.3 1.7 1.9 2.7	1.1 1.6 2.0 2.3 3.8	dB dB dB dB dB
Isolation	All paths	100 MHz 100 MHz–26.5 GHz 26.5–45 GHz 45–50 GHz 50–60 GHz	74 38 33 32 29	80 41 38 37 36		dB dB dB dB dB
Return loss (active port)	RFC-RFX	100 MHz 100 MHz–26.5 GHz 26.5–45 GHz 45–50 GHz 50–60 GHz		21 17 18 15 13		dB dB dB dB dB

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Table 3 • *TDSW0602T Electrical Specifications (Cont.)*

Parameter	Path	Condition	Min	Typ	Max	Unit
Return loss (RFC port)	RFC–RFX	100 MHz 100 MHz–26.5 GHz 26.5–45 GHz 45–50 GHz 50–60 GHz		21 20 18 16 14		dB dB dB dB dB
2nd harmonic, 2fo	RFC–RFX	+25 dBm output power, 1 GHz +25 dBm output power, 2 GHz +25 dBm output power, 6.5 GHz +25 dBm output power, 13.4 GHz		73 77 89 92		dBc dBc dBc dBc
Input 1dB compression point(1)				Fig. 2		dBm
Input IP2		1 GHz 2 GHz 6.5 GHz 13.4 GHz		93 98 109 112		dBm dBm dBm dBm
Input IP3		1 GHz 2 GHz 6 GHz 13.4 GHz		49 48 46 46		dBm dBm dBm dBm
Video feed through(2)		DC measurement		30		mV_{PP}
RF T_{RISE} /T_{FALL}		10%/90% RF		3		ns
Settling time		50% CTRL to 0.05 dB final value		48	60	ns
Switching time		50% CTRL to 90% or 10% RF		8	12	ns

Notes:
1) The input 1dB compression point is a linearity figure of merit. Refer to Table 2 for the RF input power (50Ω).
2) Measured with a 3.5 ns rise time, –3.0/+3.0V pulse and 100 MHz bandwidth.

Control Logic

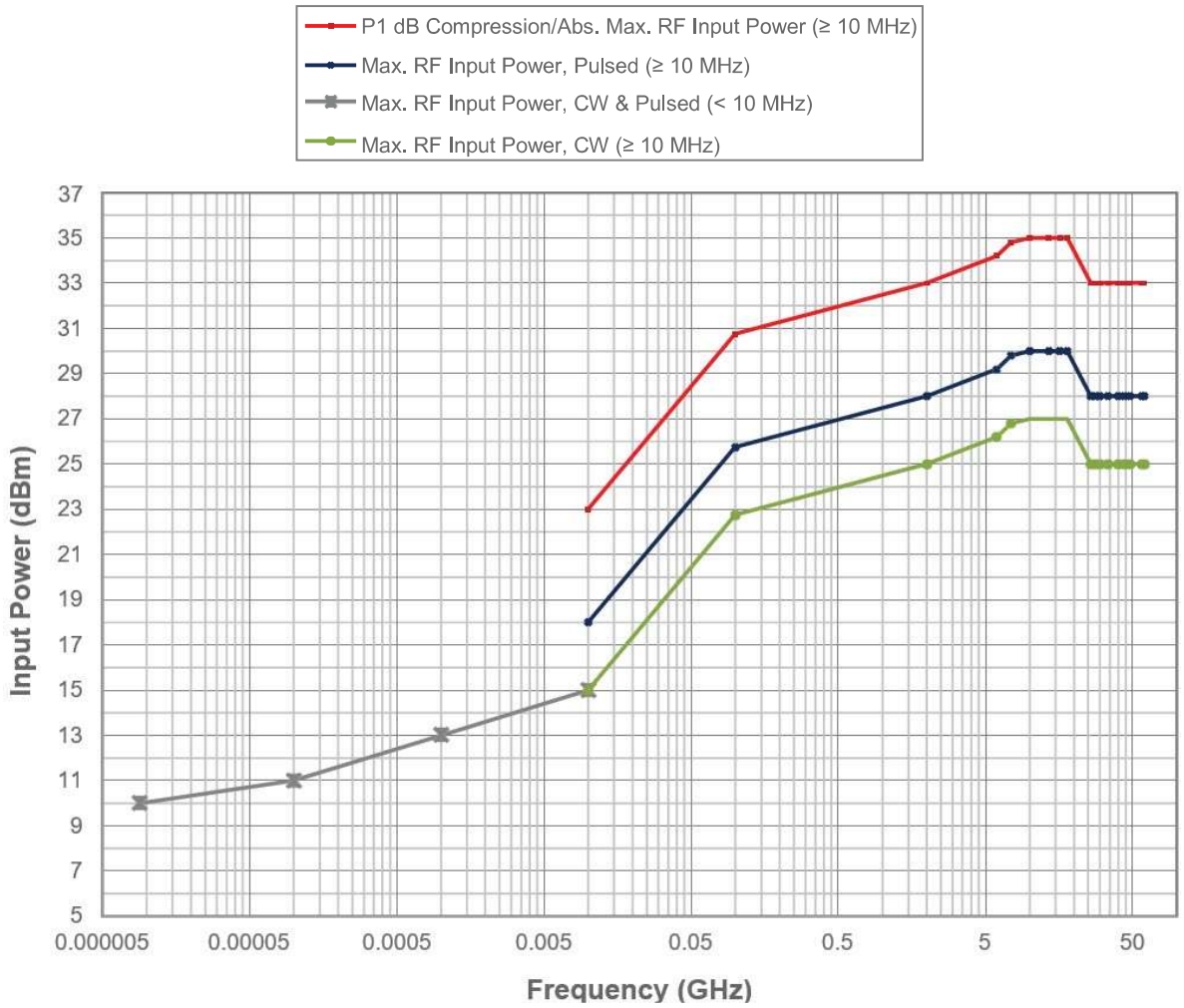
Table 4 provides the control logic truth table for the TDSW0602T. States 2 and 3 are used in normal switching operations.

Table 4 • *Truth Table for TDSW0602T*

V1	V2	RF1	RF2	State
–3.0V	–3.0V	OFF	OFF	1
–3.0V	+3.0V	OFF	ON	2
+3.0V	–3.0V	ON	OFF	3
+3.0V	+3.0V	ON	ON	4

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Figure 2 • ***Power De-rating Curve, 9 kHz–60 GHz, –55°C to +125°C Ambient, 50Ω***



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Typical Performance Data

Figure 3–Figure 12 show the typical performance data @ 25°C, V1 = +3.0V, V2 = –3.0 or V1 = –3.0V, V2 = +3.0V (Z_S = Z_L = 50Ω), unless otherwise specified.

Figure 3 • *Insertion Loss vs Temperature (RFC–RFX)*

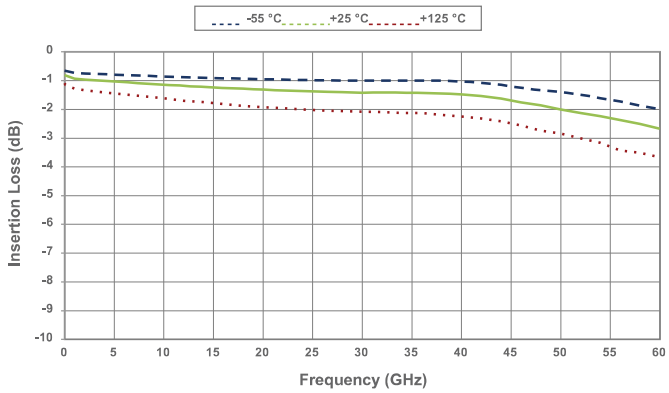


Figure 4 • *RFC Port Return Loss vs Temperature*

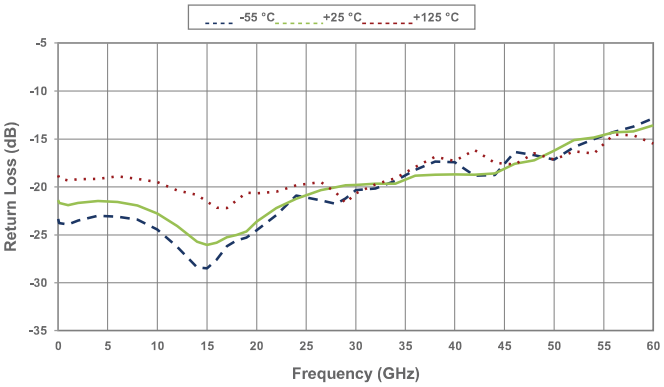


Figure 5 • *Active Port Return Loss vs Temperature*

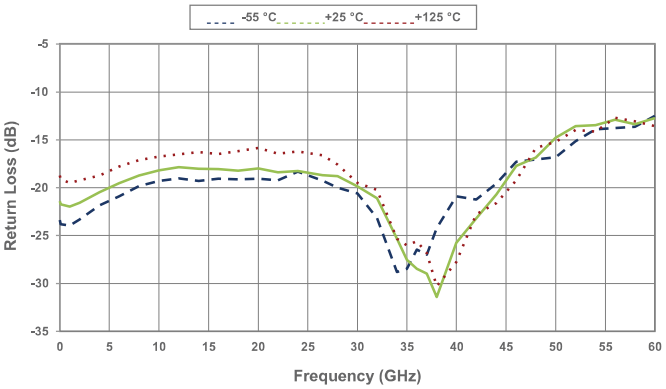


Figure 6 • *Insertion Loss vs V1/V2 (RFC–RFX)*

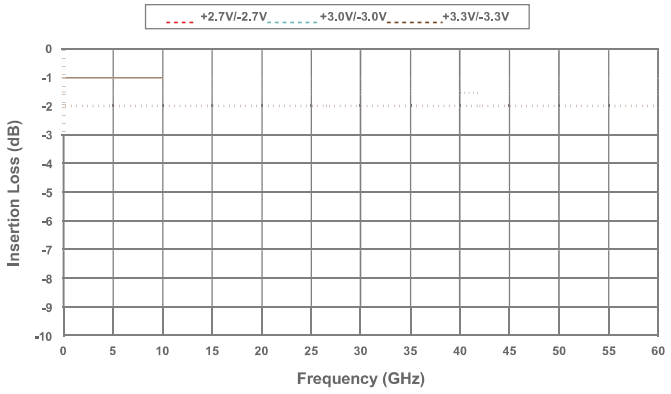


Figure 7 • *RFC Port Return Loss vs V1/V2*

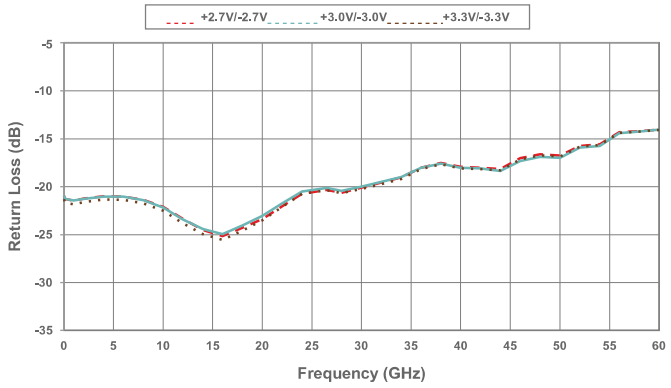
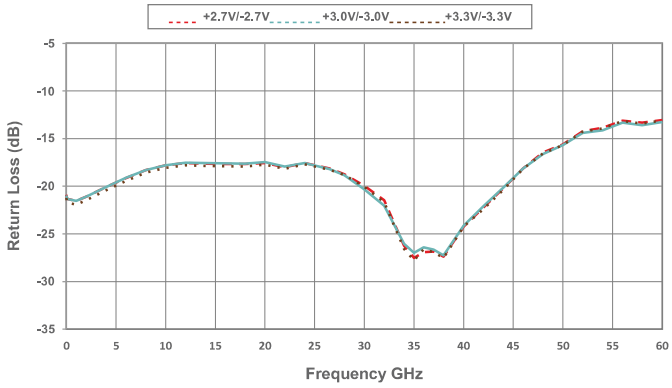


Figure 8 • *Active Port Return Loss vs V1/V2*



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Figure 9 • *Isolation vs Temperature (RFX–RFX)*

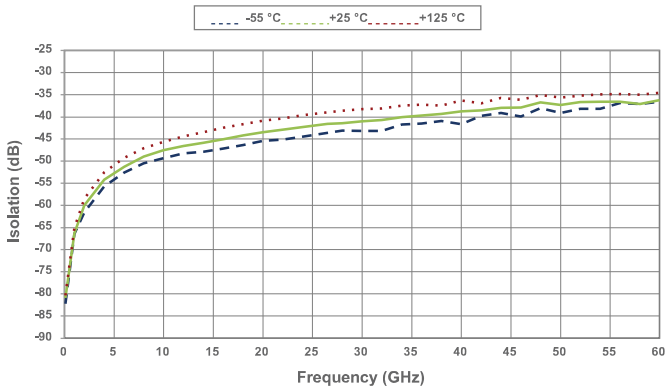


Figure 10 • *Isolation vs Temperature (RFC–RFX)*

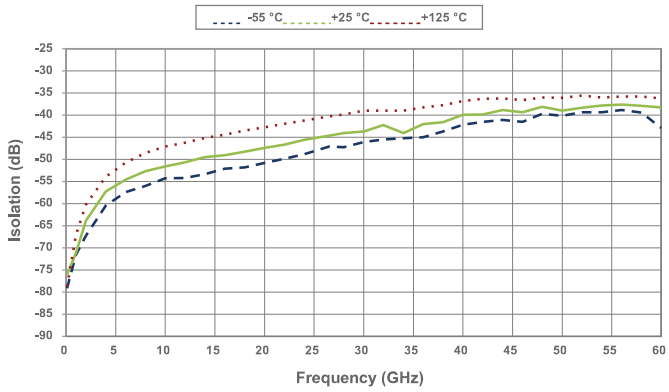


Figure 11 • *Isolation vs V1/V2 (RFX–RFX)*

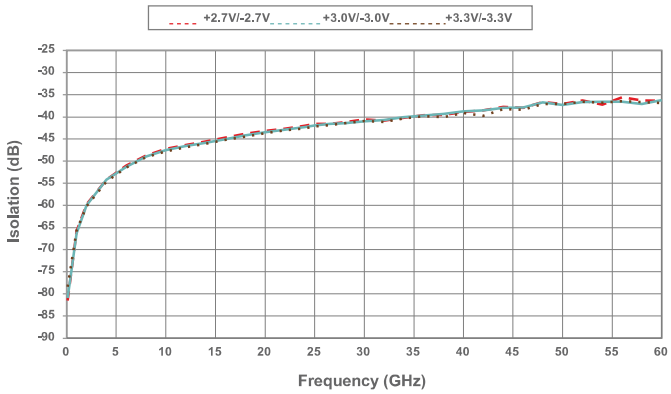
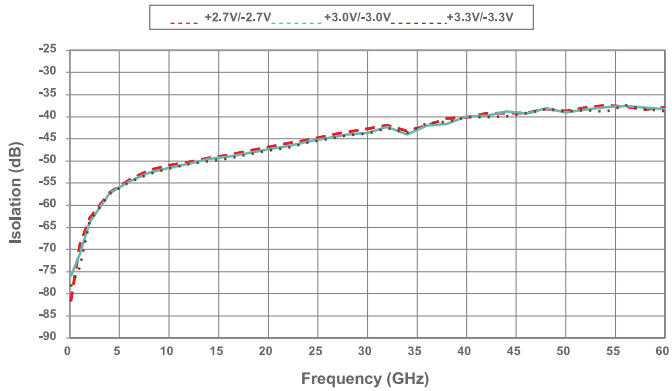


Figure 12 • *Isolation vs V1/V2 (RFC–RFX)*



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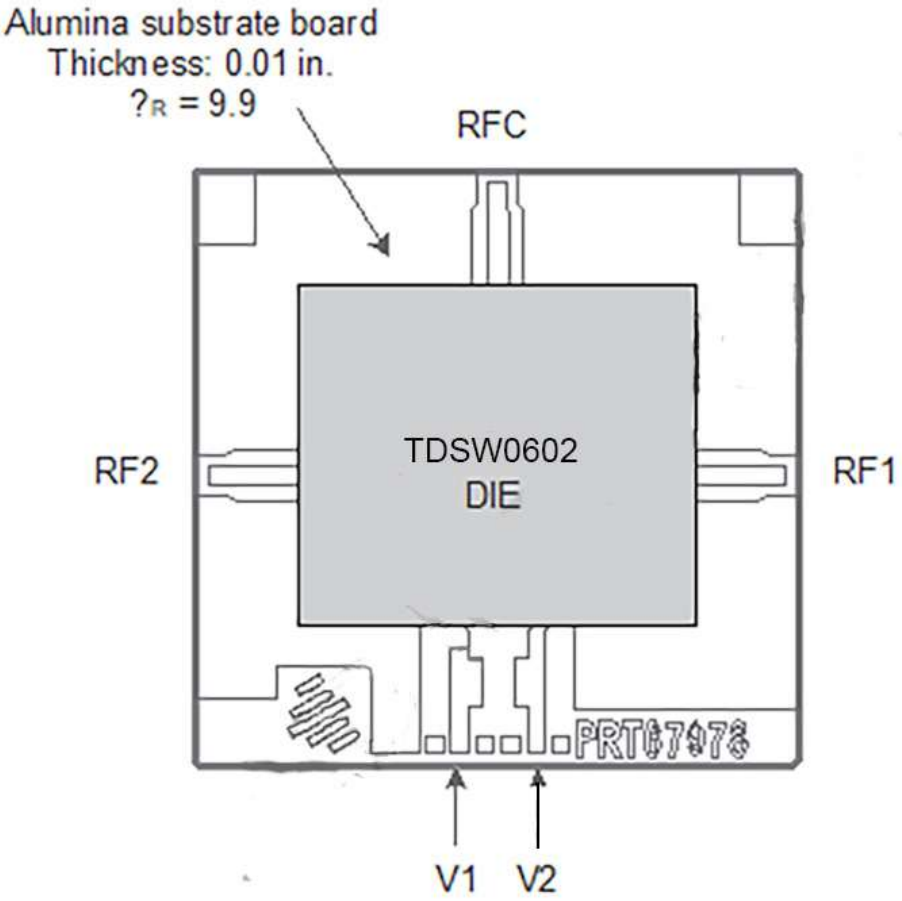
Evaluation Setup

The TDSW0602T s-parameter data and input 1dB compression point up to 60 GHz (Table 3 and Figure 3–Figure 12) were taken using either co-planar waveguide with ground (CPWG) or grounded co-planar waveguide (GCPW) on an alumina substrate and RF probes.

The TDSW0602T 2nd harmonic, input 1dB compression point below 18 GHz, input IP3 measurements, settling time and switching time (Table 3) were taken on a PCB using 2.92 mm connectors.

Bypass capacitors are not required.

Figure 13 • *Alumina Substrate Board for TDSW0602T*



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Pin Configuration

This section provides pin information for the TDSW0602T. Figure 14 shows the pin configuration of this device. Table 5 provides a description for each pin.

Figure 14 • *Pin Configuration (Bumps Up) for TDSW0602T*

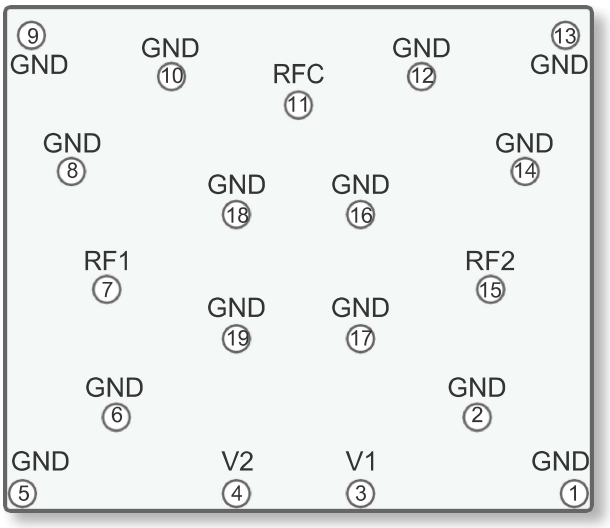


Table 5 • *Pin Descriptions for TDSW0602T*

Pin No.	Pin Name	Description
1, 2, 5, 6, 8–10, 12–14, 16–19	GND	Ground
3	V1	Control input 1
4	V2	Control input 2
7	RF1	RF port 1
11	RFC	RF common port
15	RF2	RF port 2

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Die Mechanical Specifications

This section provides the die mechanical specifications for the TDSW0602T.

Table 6 • *Mechanical Specifications for TDSW0602T*

Parameter	Min	Typ	Max	Unit	Test Condition
Die size, singulated (x, y)	2485 × 2139	2495 × 2149	2505 × 2159	µm	Including excess silicon, maximum tolerance = ±10 µm
Wafer thickness	180	200	220	µm	
Bump pitch	500			µm	
Bump height	59.5	70	80.5	µm	
Bump diameter		91		µm	
UBM diameter	71	75	79	µm	

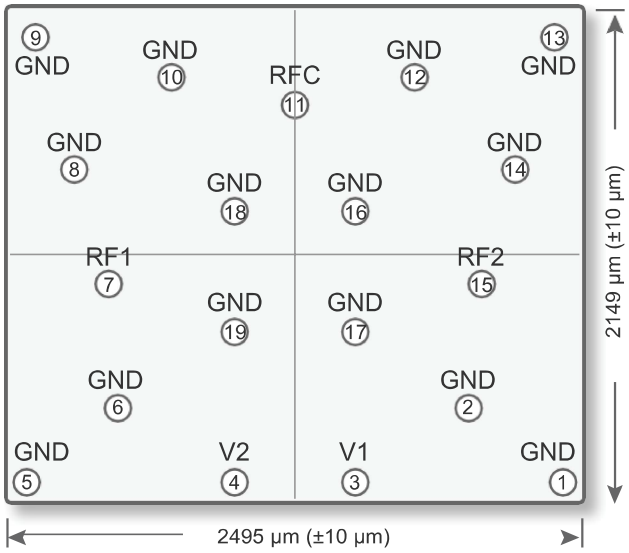
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Table 7 • ***Pin Coordinates for TDSW0602T***(*)

Pin #	Pin Name	Pin Center (µm)	
		X	Y
1	GND	1128.5	–958.5
2	GND	731.5	–646.5
3	V1	253.5	–958.5
4	V2	–253.5	–958.5
5	GND	–1128.5	–958.5
6	GND	–731.5	–646.5
7	RF1	–785.5	–121.5
8	GND	–931.5	363.5
9	GND	–1091.5	913.5
10	GND	–503.5	753.5
11	RFC	0	629
12	GND	503.5	753.5
13	GND	1091.5	913.5
14	GND	931.5	363.5
15	RF2	785.5	–121.5
16	GND	253.5	183.5
17	GND	253.5	–326.5
18	GND	–253.5	183.5
19	GND	–253.5	–326.5

Note: * All pin locations originate from the die center and refer to the center of the pin.

Figure 15 • ***Pin Layout for TDSW0602T***(1)(2)



Notes:

1) Drawings are not drawn to scale.
2) Singulated die size shown, bump side up.

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Ordering Information

Table 8 lists the available ordering code for the TDSW0602T as well as shipping method.

Table 8 • *Order Code for TDSW0602T*

Order Code	Description	Packaging	Shipping Method
TDSW0602T–99	TDSW0602 SPDT RF switch	Flip Chip Die / Waffle Pack	Waffle Pack
TDSW0602T–00	TDSW0602T SPDT RF switch EVK	Evaluation Kit	Unit
TDSW0602T–88[1]	TDSW0602T Commercial Level EM Die	Flip-chip Die/Tape and Reel	Tape and Reel

Notes:
1.The TDSW0602T-88 die are ES (engineering sample) units intended as initial evaluation devices for customers of the TDSW0602T-99 flight die. TheTDSW0602T-88 ESdie provide the same electrical functionality and performance as the TDSW0602T-99flight die, but is processed to a non-compliant flow (e.g. no QCI coverage or element evaluation data). These die are obtained from non-qualified wafers so are not suitable forqualification, production, radiation testing or flight use.

Document Categories

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