

N-channel 900 V, 0.91 Ω typ., 6 A MDmesh™ K5 Power MOSFET in an I²PAK package

Datasheet - production data

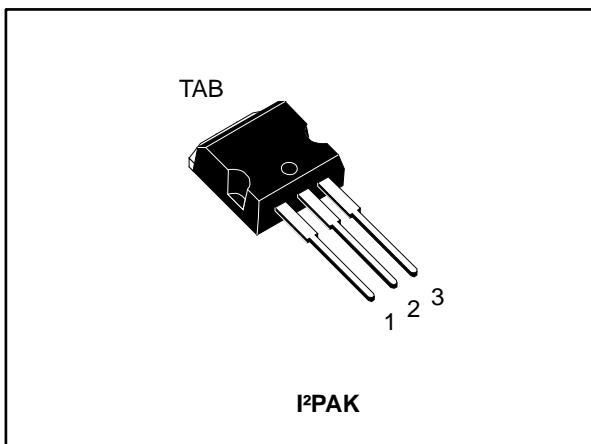
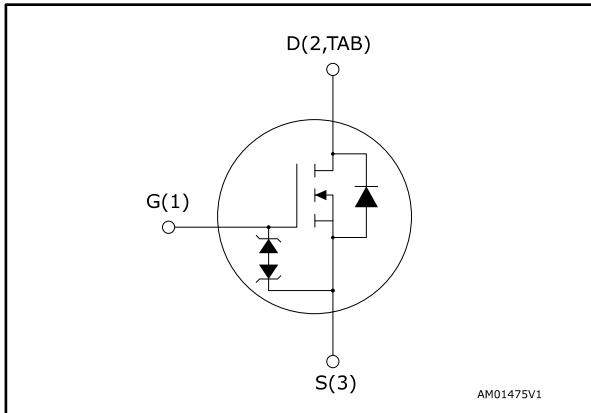


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STI6N90K5	900 V	1.10 Ω	6 A

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STI6N90K5	6N90K5	I ² PAK	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	6	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	4	A
$I_D^{(1)}$	Drain current (pulsed)	24	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_j	Operating junction temperature range	- 55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:

(1)Pulse width limited by safe operating area

(2) $I_{SD} \leq 6$ A, $di/dt \leq 100$ A/ μs ; V_{DS} peak $< V_{(BR)DSS}$, $V_{DD} = 450$ V.(3) $V_{DS} \leq 720$ V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.14	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C}/\text{W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50$ V)	210	mJ

2 Electrical characteristics

$T_C = 25^\circ\text{C}$ unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_D = 1 \text{ mA}$	900			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0 \text{ V}$, $V_{\text{DS}} = 900 \text{ V}$			1	μA
		$V_{\text{GS}} = 0 \text{ V}$, $V_{\text{DS}} = 900 \text{ V}$ $T_C = 125^\circ\text{C}$ ⁽¹⁾			50	μA
I_{GSS}	Gate body leakage current	$V_{\text{DS}} = 0 \text{ V}$, $V_{\text{GS}} = \pm 20 \text{ V}$			± 10	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DD}} = V_{\text{GS}}$, $I_D = 100 \mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10 \text{ V}$, $I_D = 3 \text{ A}$		0.91	1.10	Ω

Notes:

⁽¹⁾ Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100 \text{ V}$, $f = 1 \text{ MHz}$, $V_{\text{GS}} = 0 \text{ V}$	-	342	-	pF
C_{oss}	Output capacitance		-	31	-	pF
C_{rss}	Reverse transfer capacitance		-	1.2	-	pF
$C_{\text{o(tr)}}^{(1)}$	Equivalent capacitance time related	$V_{\text{DS}} = 0 \text{ to } 720 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$	-	55	-	pF
$C_{\text{o(er)}}^{(2)}$	Equivalent capacitance energy related		-	20	-	pF
R_g	Intrinsic gate resistance	$f = 1 \text{ MHz}$, $I_D = 0 \text{ A}$	-	6.4	-	Ω
Q_g	Total gate charge	$V_{\text{DD}} = 720 \text{ V}$, $I_D = 6 \text{ A}$ $V_{\text{GS}} = 10 \text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	11	-	nC
Q_{gs}	Gate-source charge		-	2.5	-	nC
Q_{gd}	Gate-drain charge		-	7	-	nC

Notes:

⁽¹⁾ $C_{\text{o(tr)}}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁽²⁾ $C_{\text{o(er)}}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450 \text{ V}$, $I_D = 3 \text{ A}$, $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see <i>Figure 14: "Test circuit for resistive load switching times"</i> and <i>Figure 19: "Switching time waveform"</i>)	-	12.4	-	ns
t_r	Rise time		-	12.2	-	ns
$t_{d(off)}$	Turn-off delay time		-	30.4	-	ns
t_f	Fall time		-	15.5	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 6 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i>)	-	342		ns
Q_{rr}	Reverrse recovery charge		-	3.13		μC
I_{RRM}	Reverse recovery current		-	18.3		A
t_{rr}	Reverse recovery time		-	536		ns
Q_{rr}	Reverse recovery charge	$I_{SD} = 6 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i>)	-	4.42		μC
I_{RRM}	Reverse recovery current		-	16.5		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1

Electrical characteristics (curves)

Figure 2: Safe operating area

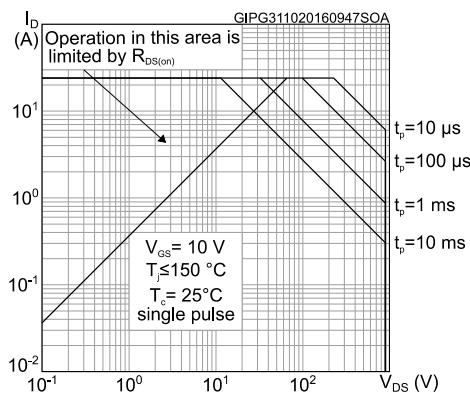


Figure 3: Thermal impedance

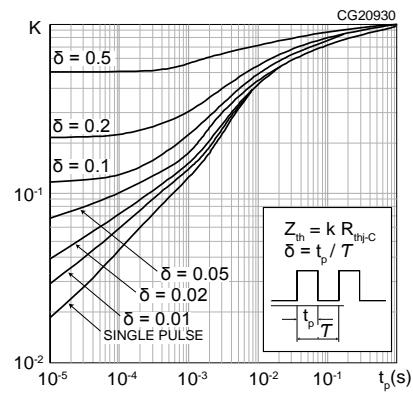


Figure 4: Output characteristics

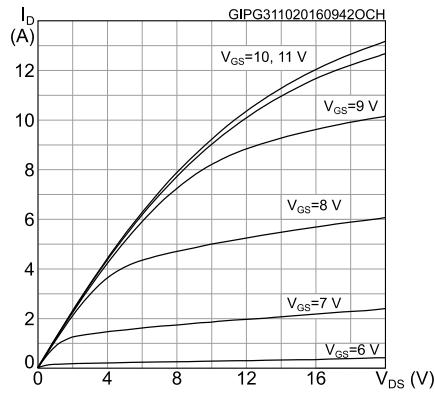


Figure 5: Transfer characteristics

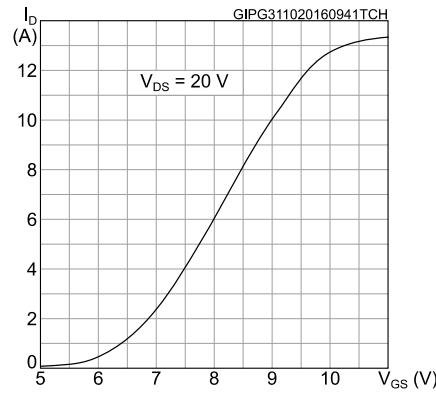


Figure 6: Gate charge vs gate-source voltage

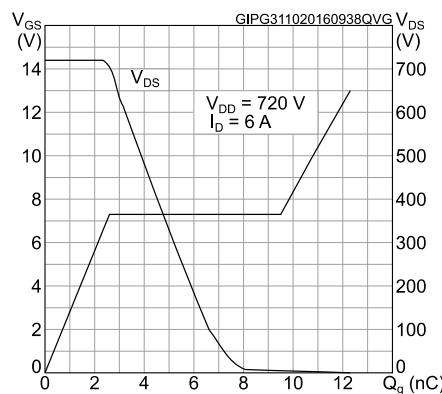


Figure 7: Static drain-source on-resistance

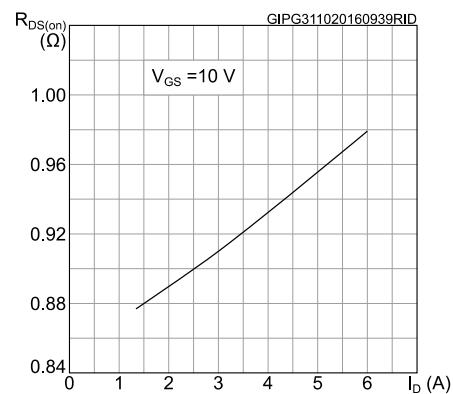


Figure 8: Capacitance variations

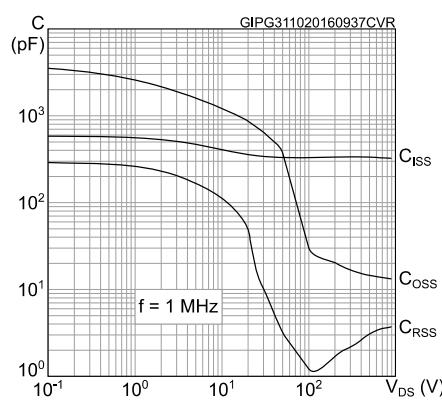


Figure 9: Normalized gate threshold voltage vs temperature

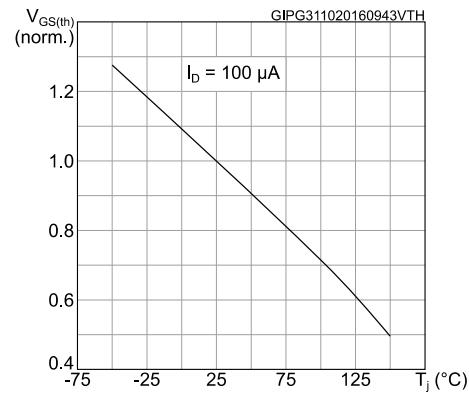


Figure 10: Normalized on-resistance vs temperature

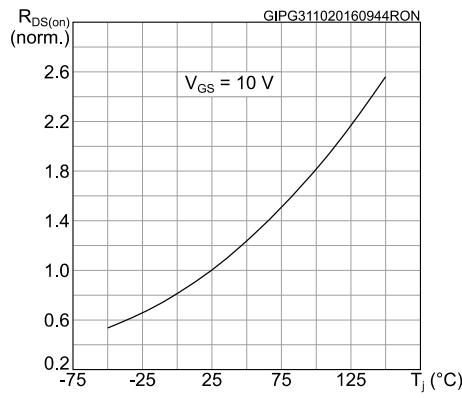


Figure 11: Normalized V_(BR)DSS vs temperature

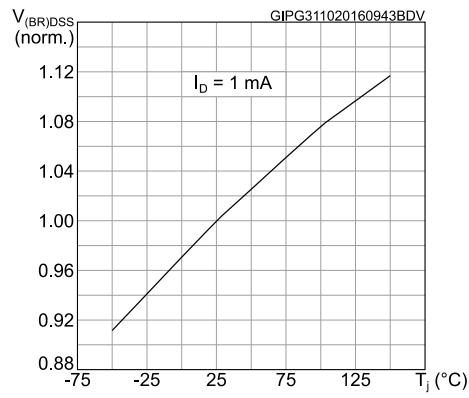


Figure 12: Maximum avalanche energy vs starting T_j

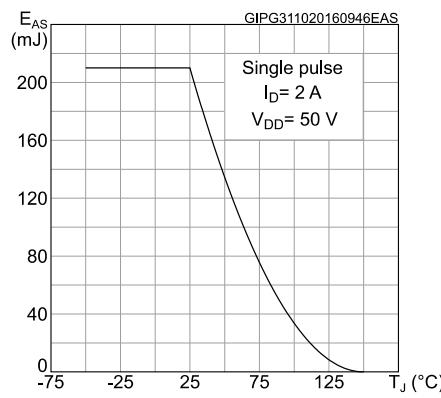
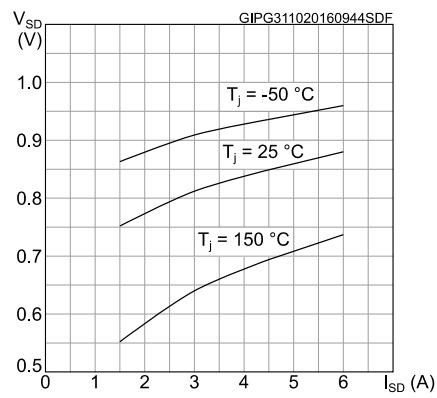


Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Test circuit for resistive load switching times

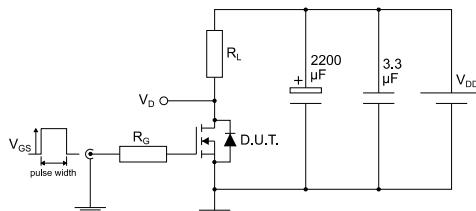


Figure 15: Test circuit for gate charge behavior

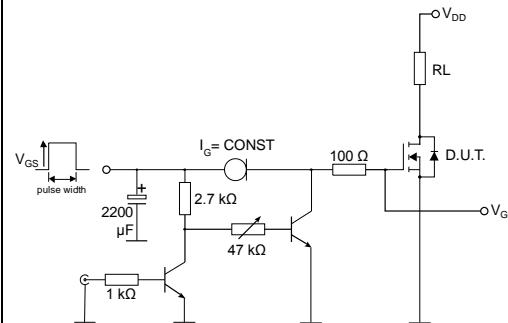


Figure 16: Test circuit for inductive load switching and diode recovery times

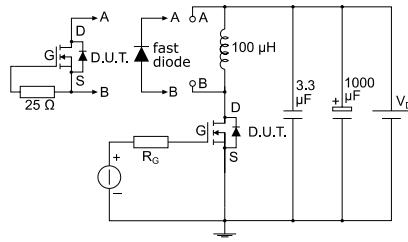


Figure 17: Unclamped inductive load test circuit

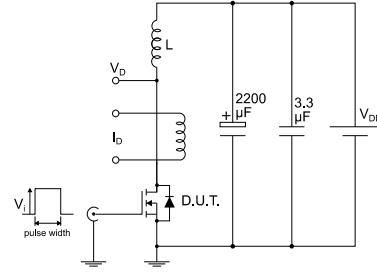


Figure 18: Unclamped inductive waveform

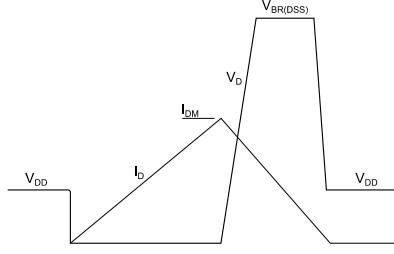
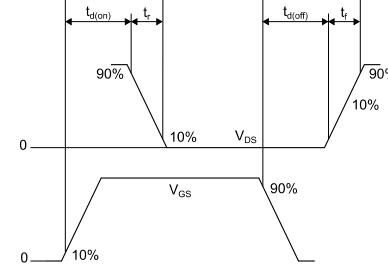


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 I²PAK package information

Figure 20: I²PAK package outline

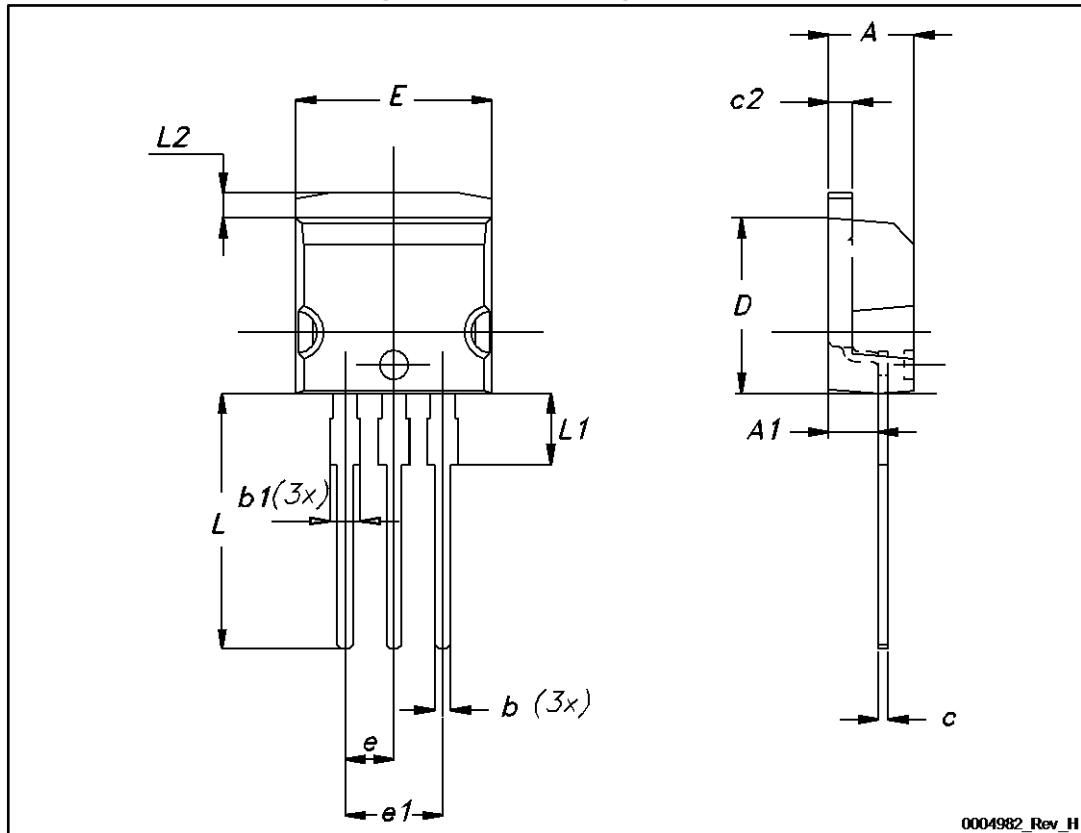


Table 10: I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	—	4.60
A1	2.40	—	2.72
b	0.61	—	0.88
b1	1.14	—	1.70
c	0.49	—	0.70
c2	1.23	—	1.32
D	8.95	—	9.35
e	2.40	—	2.70
e1	4.95	—	5.15
E	10	—	10.40
L	13	—	14
L1	3.50	—	3.93
L2	1.27	—	1.40

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
02-Nov-2016	1	First release.

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