# NTD5865NL

## MOSFET – Power, N-Channel
### 60 V, 46 A, 16 mΩ

**ON Semiconductor®**

**http://onsemi.com**

| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---|---|---|
| 60 V | 16 mΩ @ 10 V | 46 A |
| | 19 mΩ @ 4.5 V | |

**Features**

- Low Gate Charge
- Fast Switching
- High Current Capability
- 100% Avalanche Tested
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

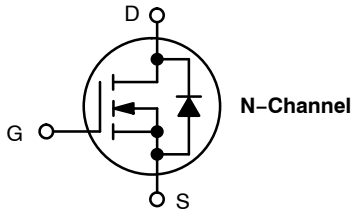
| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 60 | V |
| Gate−to−Source Voltage − Continuous | | | $V_{GS}$ | ±20 | V |
| Gate−to−Source Voltage − Non−Repetitive ($t_p$ < 10 μs) | | | $V_{GS}$ | ±30 | V |
| Continuous Drain Current ($R_{\theta JC}$) | Steady State | $T_C$ = 25°C | $I_D$ | 46 | A |
| | | $T_C$ = 100°C | | 33 | |
| Power Dissipation ($R_{\theta JC}$) | | $T_C$ = 25°C | $P_D$ | 71 | W |
| Pulsed Drain Current | $t_p$ = 10 μs | | $I_{DM}$ | 203 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{stg}$ | −55 to 175 | °C |
| Source Current (Body Diode) | | | $I_S$ | 46 | A |
| Single Pulse Drain−to−Source Avalanche Energy | (L = 0.1 mH) | | $E_{AS}$ | 36 | mJ |
| | | | $I_{AS}$ | 27 | A |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

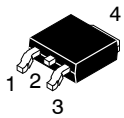
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL RESISTANCE MAXIMUM RATINGS**

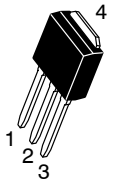
| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Case (Drain) | $R_{\theta JC}$ | 2.1 | °C/W |
| Junction−to−Ambient − Steady State (Note 1) | $R_{\theta JA}$ | 49 | |

1. Surface−mounted on FR4 board using a 650 mm², 2 oz. Cu pad.



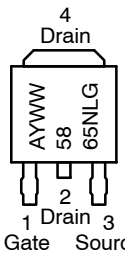



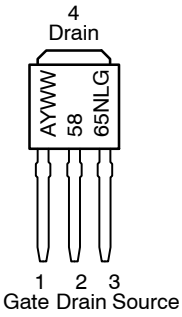

**DPAK**
**CASE 369AA**
**(Surface Mount)**
**STYLE 2**




**IPAK**
**CASE 369D**
**(Straight Lead)**
**STYLE 2**

**MARKING DIAGRAMS & PIN ASSIGNMENT**




A = Assembly Location*
Y = Year
WW = Work Week
5865NL = Device Code
G = Pb−Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 5 of this data sheet.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 60 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | | 55 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 60 V | $T_J$ = 25°C | | | 1.0 | μA |
| | | | $T_J$ = 150°C | | | 100 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | 1.0 | | 2.0 | V |
| Negative Threshold Temperature Co-efficient | $V_{GS(TH)}/T_J$ | | | | 5.6 | | mV/°C |
| Drain−to−Source on Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 20 A | | | 13 | 16 | mΩ |
| Drain−to−Source on Resistance | $R_{DS(on)}$ | $V_{GS}$ = 4.5 V, $I_D$ = 20 A | | | 16 | 19 | mΩ |
| Forward Transconductance | gFS | $V_{DS}$ = 15 V, $I_D$ = 20 A | | | 15 | | S |
| **CHARGES, CAPACITANCES AND GATE RESISTANCES** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = 25 V | | | 1400 | | pF |
| Output Capacitance | $C_{oss}$ | | | | 137 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | | 95 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 48 V, $I_D$ = 40 A | | | 29 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 1.1 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 4 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 8 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 48 V, $I_D$ = 40 A | | | 15 | | nC |
| Gate Resistance | $R_G$ | | | | 1.3 | | Ω |
| **SWITCHING CHARACTERISTICS** (Note 3) | | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 10 V, $V_{DD}$ = 48 V, $I_D$ = 40 A, $R_G$ = 2.5 Ω | | | 8.4 | | ns |
| Rise Time | $t_r$ | | | | 12.4 | | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 26 | | |
| Fall Time | $t_f$ | | | | 4.4 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 40 A | $T_J$ = 25°C | | 0.95 | 1.2 | V |
| | | | $T_J$ = 125°C | | 0.85 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, dIs/dt = 100 A/μs, $I_S$ = 40 A | | | 20 | | ns |
| Charge Time | ta | | | | 13 | | |
| Discharge Time | tb | | | | 7 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 13 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.



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## TYPICAL CHARACTERISTICS

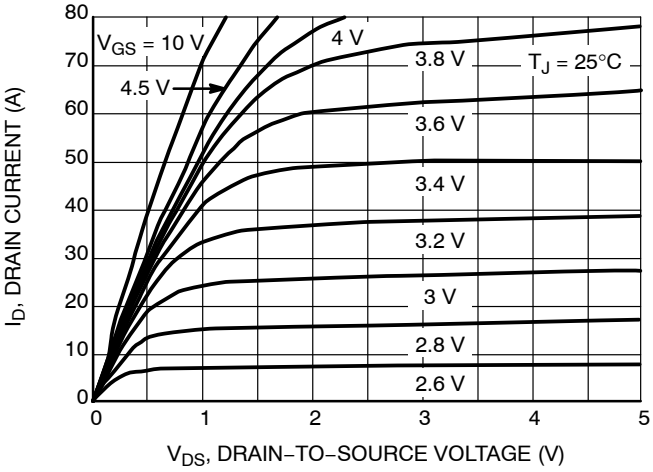


**Figure 1. On−Region Characteristics**

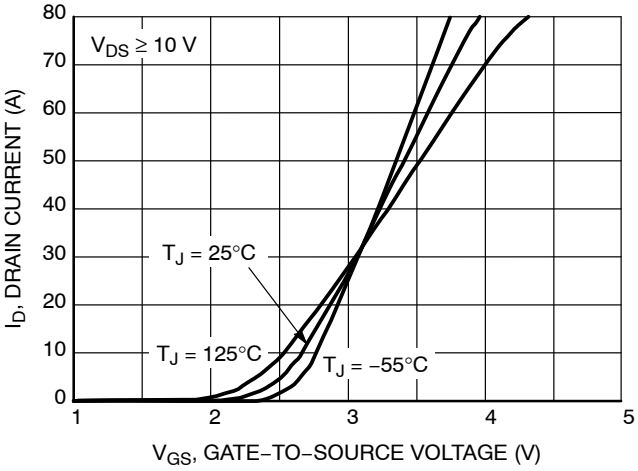


**Figure 2. Transfer Characteristics**

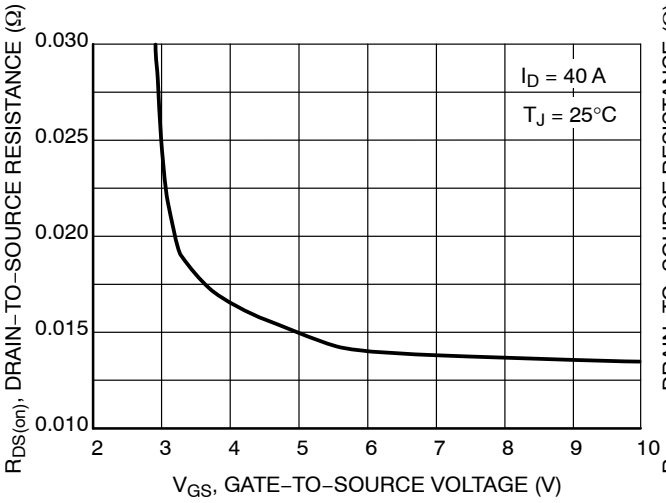


**Figure 3. On−Resistance vs. Gate Voltage**

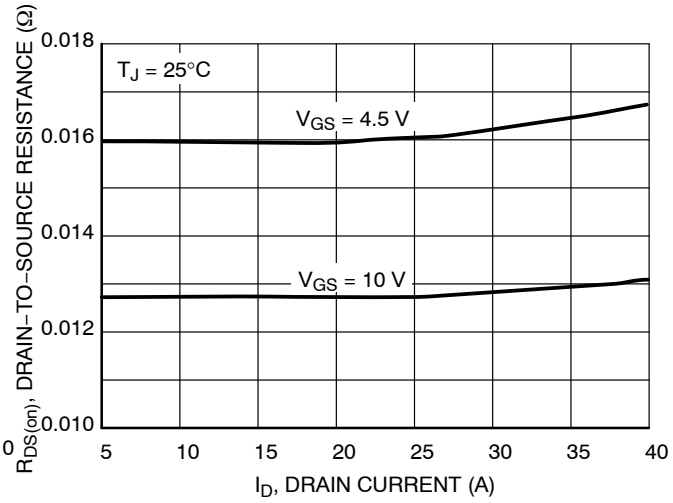


**Figure 4. On−Resistance vs. Drain Current**

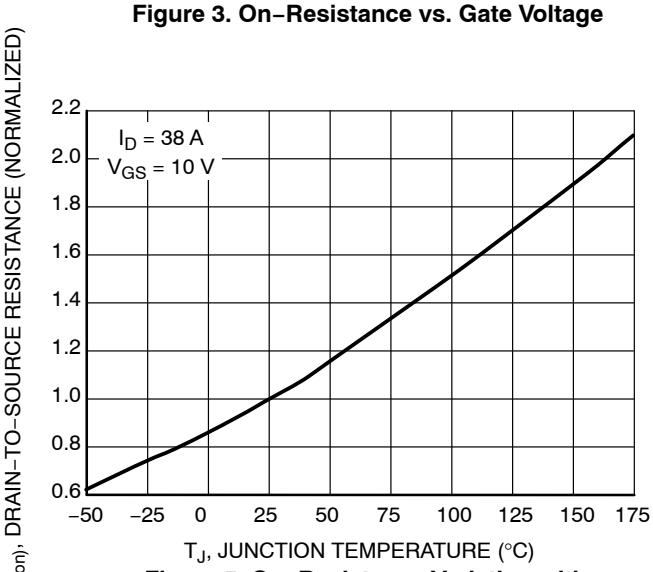


**Figure 5. On−Resistance Variation with Temperature**

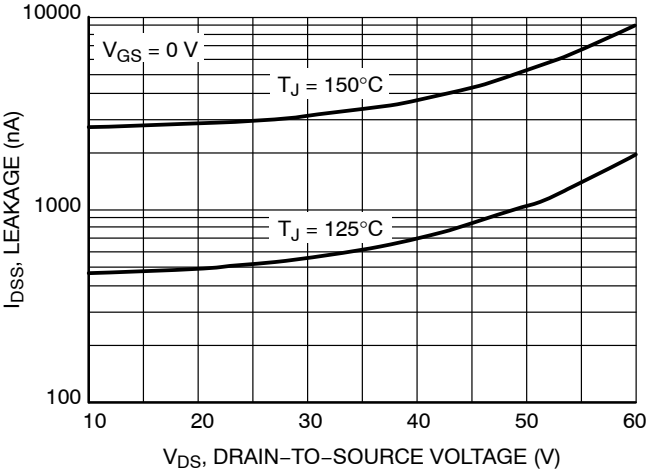


**Figure 6. Drain−to−Source Leakage Current vs. Voltage**



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## TYPICAL CHARACTERISTICS

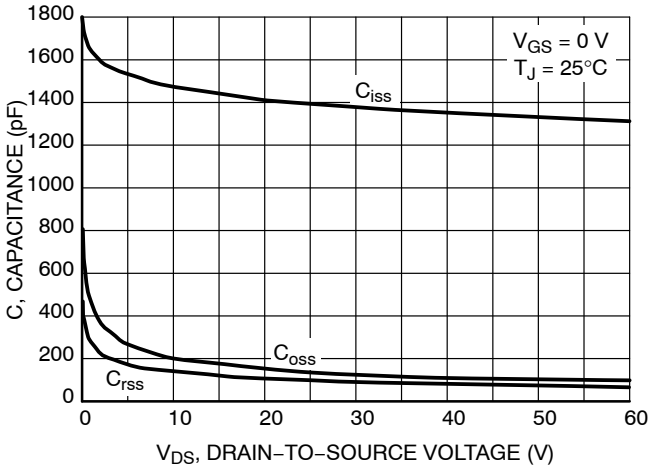


**Figure 7. Capacitance Variation**

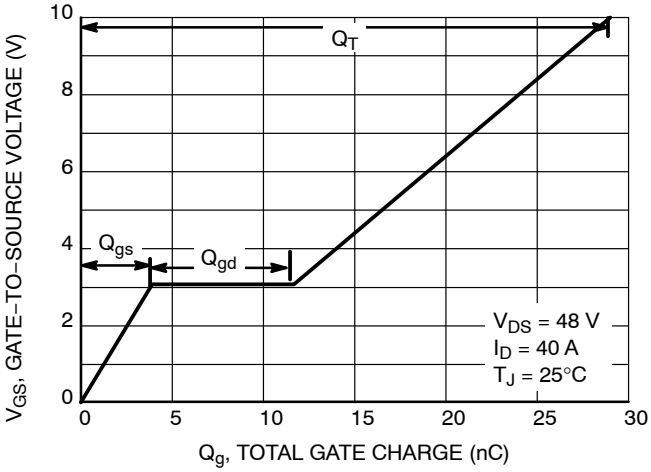


**Figure 8. Gate−to−Source vs. Total Charge**

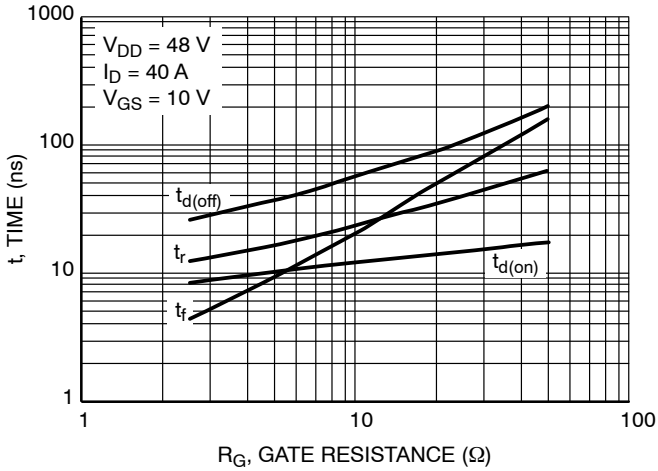


**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

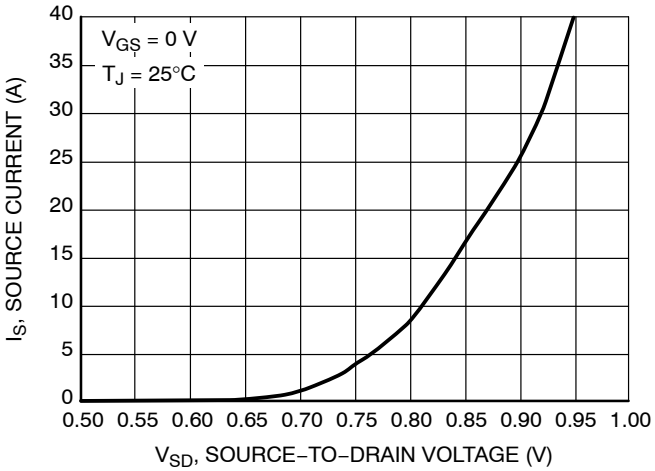


**Figure 10. Diode Forward Voltage vs. Current**

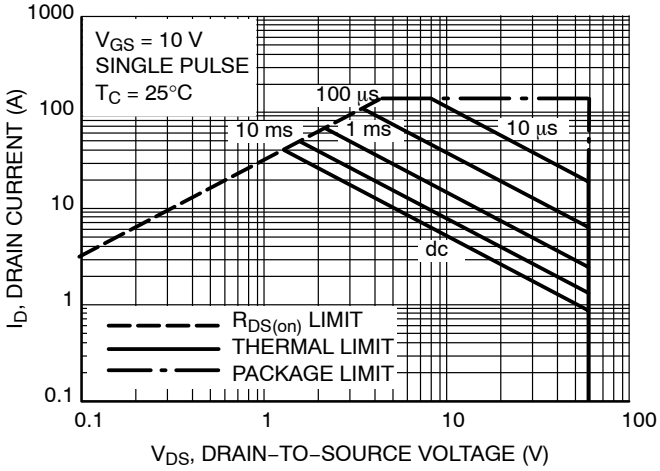


**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



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## TYPICAL CHARACTERISTICS

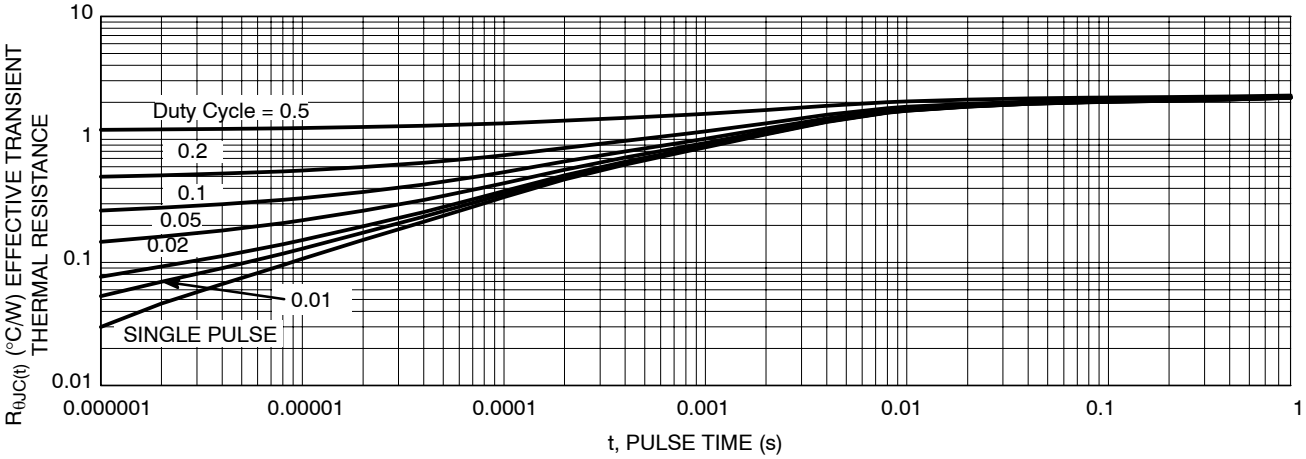


**Figure 12. Thermal Response**

### ORDERING INFORMATION

| Order Number | Package | Shipping† |
|---|---|---|
| NTD5865NL−1G | IPAK (Straight Lead)<br>(Pb−Free) | 75 Units / Rail |
| NTD5865NLT4G | DPAK<br>(Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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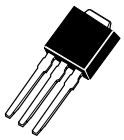
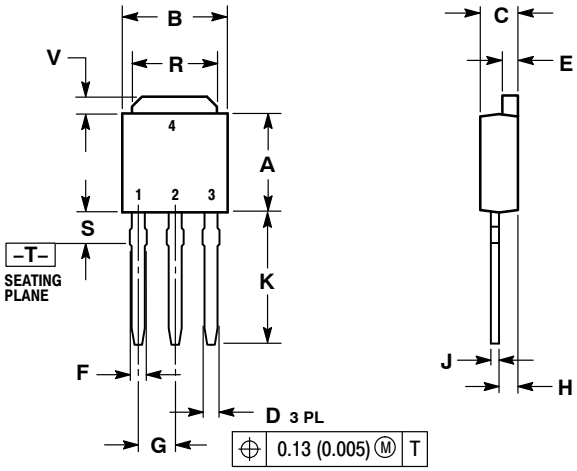


SCALE 1:1

**DPAK INSERTION MOUNT**
CASE 369
ISSUE O

DATE 02 JAN 2000




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.250 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.033 | 0.040 | 0.84 | 1.01 |
| F | 0.037 | 0.047 | 0.94 | 1.19 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.175 | 0.215 | 4.45 | 5.46 |
| S | 0.050 | 0.090 | 1.27 | 2.28 |
| V | 0.030 | 0.050 | 0.77 | 1.27 |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

| | | |
|---|---|---|
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| DESCRIPTION: | DPAK INSERTION MOUNT | PAGE 1 OF 1 |

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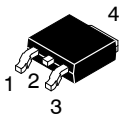


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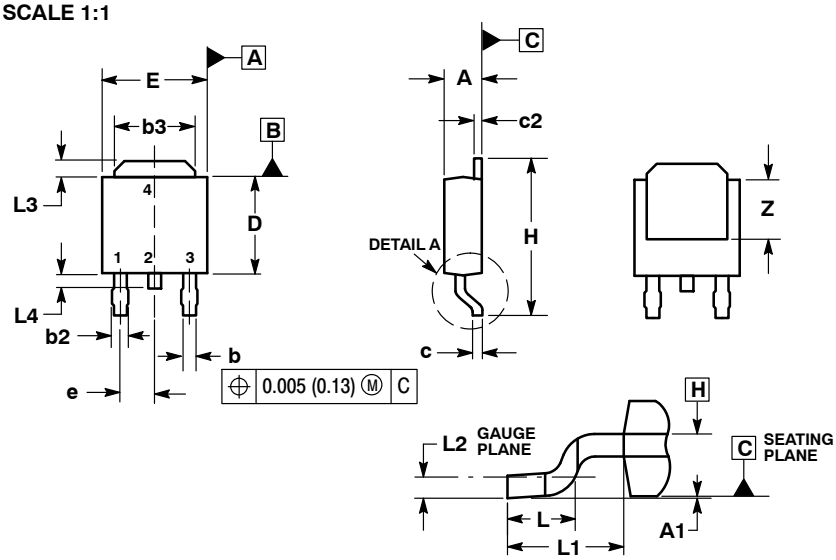
## DPAK (SINGLE GUAGE)
CASE 369AA
ISSUE B

DATE 03 JUN 2010




**DETAIL A**
ROTATED 90° CW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

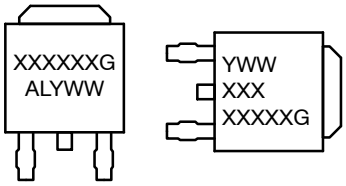
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## GENERIC MARKING DIAGRAM*

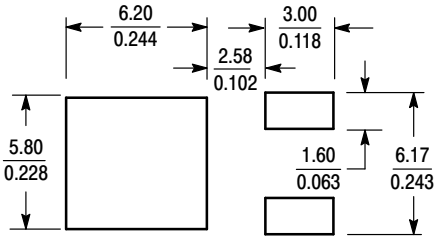



IC Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

## SOLDERING FOOTPRINT*




SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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|---|---|---|
| DESCRIPTION: | DPAK (SINGLE GAUGE) | PAGE 1 OF 1 |

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