RoHS

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Vishay Siliconix

P-Channel 20 V (D-S) MOSFET

PowerPAK® 0806 Single

Bottom View

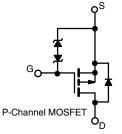
PRODUCT SUMMARY						
V _{DS} (V)	-20					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5 \text{ V}$	1.25					
$R_{DS(on)}$ max. (Ω) at V_{GS} = -2.5 V	1.7					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.8 \text{ V}$	2.7					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.5 \text{ V}$	4.4					
Q _g typ. (nC)	0.64					
I _D (A)	-0.5 ^{a, f}					
Configuration	Single					

FEATURES

- TrenchFET® Gen III p-channel power MOSFET
- Ultra small 0.8 mm x 0.6 mm outline
- Ultra thin 0.4 mm max. height
- Typical ESD protection 1500 V (HBM)
- -1.5 V rated R_{DS(on)}
- 100% R_q tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- · Load switch
- · High speed switching
- Power management in battery-operated, mobile and wearable devices



ORDERING INFORMATION	
Package	PowerPAK 0806
Lead (Pb)-free and halogen-free	SiUD403ED-T1-GE3

The lead finish is NiPdAu and classed as E4 finish

Top View

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage		V_{DS}	-20	V		
Gate-source voltage		V_{GS}	± 8	V		
	T _A = 25 °C		-0.5 ^{a, f}			
Continuous drain surrent (T. 150 °C)	T _A = 70 °C	1 , [-0.5 ^{a, f}			
Continuous drain current (T _J = 150 °C)	T _A =25 °C	l _D	-0.4 ^b			
	T _A = 70 °C	1	-0.32 b	Α		
Pulsed drain current (t = 100 μs)		I _{DM}	-0.8			
	T _A = 25 °C		-0.5 ^{a, f}			
Continuous source-drain diode current	T _A = 70 °C	l _S	-0.37 b	\neg		
	T _A = 25 °C		1.25 ^a			
Maximum power dissipation	T _A = 70 °C	1 5	0.8 ^a	w		
	T _A = 25 °C	P _D	0.37 b	VV		
	T _A = 70 °C		0.24 ^b			
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C		
Soldering recommendations (peak temperature) c			260			

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^{a, d}	+ < 5.0	В	80	100	°C/W	
Maximum junction-to-ambient b, e	t ≤ 5 s	R _{thJA}	265	335	J 6/44	

Notes

- Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s Refer to IPC / JEDEC® (J-STD-020), no manual or hand soldering Maximum under steady state conditions is 135 °C/W

- Maximum under steady state conditions is 400 °C/W
- Package limited

Document Number: 70731



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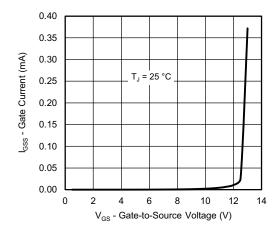
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static					•		
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-20	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	J 050 A	-	-12.4	-	m\//°C	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	1.6	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.4	-	-0.9	V	
Gate-source leakage		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$	-	-	± 0.5	μA	
	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$	-	-	± 7		
Zana mata walta sa duaka awanat		V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1		
Zero gate voltage drain current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	μA	
On-state drain current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = 0 \text{ V}$	-0.5	-	-	Α	
		$V_{GS} = -4.5 \text{ V}, I_D = -0.3 \text{ A}$	-	1.01	1.25		
Data and a state with a second	5	$V_{GS} = -2.5 \text{ V}, I_D = -0.1 \text{ A}$	-	1.4	1.7		
Drain-source on-state resistance a	R _{DS(on)}	V _{GS} = -1.8 V, I _D = -0.1 A	-	2.1	2.7	Ω	
		V _{GS} = -1.5 V, I _D = -0.05 A	-	2.8	4.4	1	
Forward transconductance a	9 _{fs}	$V_{DS} = -10 \text{ V}, I_D = -0.3 \text{ A}$	-	0.6	-	S	
Dynamic ^b					•		
Input capacitance	C _{iss}		-	31	-	pF	
Output capacitance	C _{oss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	8.1	-		
Reverse transfer capacitance	C _{rss}		-	7	-		
Table de de co	Qg	$V_{DS} = -10 \text{ V}, V_{GS} = -8 \text{ V}, I_{D} = -0.3 \text{ A}$	- 1.1		1.7		
Total gate charge		$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -0.3 \text{ A}$	-	0.64	1	0	
Gate-source charge	Q_{gs}	V 40VV 45VI 00A	-	0.13	-	nC	
Gate-drain charge	Q_{gd}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -0.3 \text{ A}$	_	0.1	-	1	
Gate resistance	R_g	f = xx MHz	15	74	150	Ω	
Turn-on delay time	t _{d(on)}		-	7	15		
Rise time	t _r	$V_{DD} = -10 \text{ V}, R_L = 33.3 \Omega, I_D \cong -0.3 \text{ A},$	_	21	40	ns	
Turn-off delay time	t _{d(off)}	$V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	-	11	20		
Fall time	t _f		-	11	20		
Turn-on delay time	t _{d(on)}		-	2	5		
Rise time	t _r	$V_{DD} = -10 \text{ V}, R_L = 33.3 \Omega, I_D \cong -0.3 \text{ A},$	-	18	40		
Turn-off delay time	t _{d(off)}	V_{GEN} = -8 V, R_g = 1 Ω	-	10	20		
Fall time	t _f		-	10	20		
Drain-Source Body Diode Characteristi	cs						
Continuous source-drain diode current	Is	T _A = 25 °C	-	-	-0.5 ^c	^	
Pulse diode forward current	I _{SM}		-	-	-0.8	A	
Body diode voltage	V _{SD}	$I_S = -0.3 \text{ A}, V_{GS} = 0 \text{ V}$	-	-0.9	-1.2	V	
Body diode reverse recovery time	t _{rr}		-	15	30	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = -0.3 A, di/dt = 100 A/μs,	-	7.5	15	nC	
Reverse recovery fall time	t _a	T _J = 25 °C	-	10.5	-		
Reverse recovery rise time	t _b		-	4.5	-	ns	

Notes

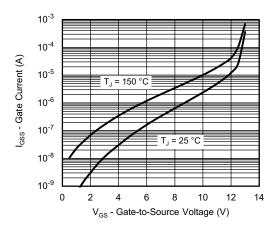
- a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing
- c. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

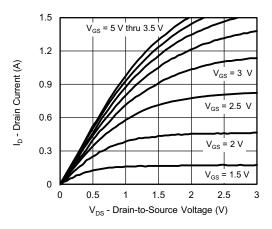




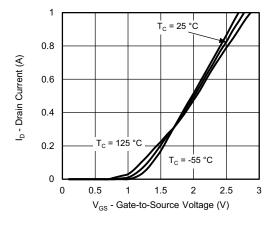
Gate Current vs. Gate-Source Voltage



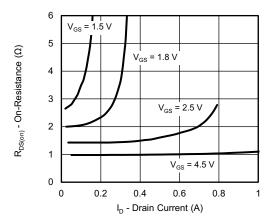
Gate Current vs. Gate-Source Voltage



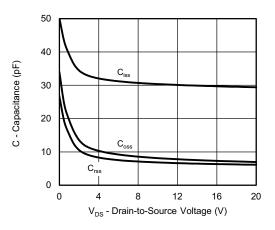
Output Characteristics



Transfer Characteristics

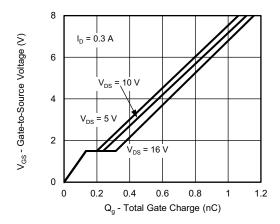


On-Resistance vs. Drain Current and Gate Voltage

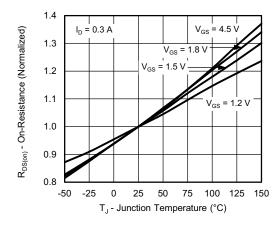


Capacitance

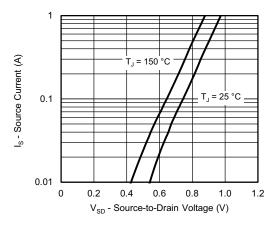




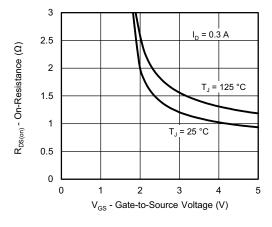
Gate Charge



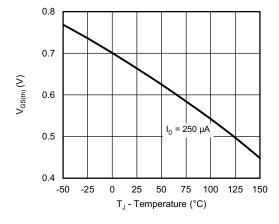
On-Resistance vs. Junction Temperature



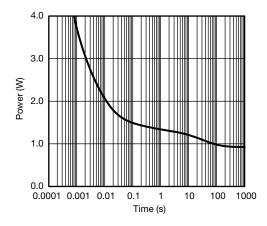
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

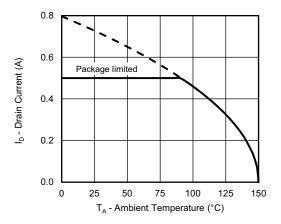


Threshold Voltage

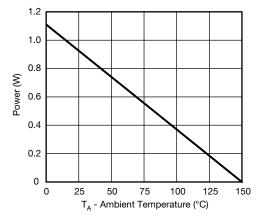


Single Pulse Power, Junction-to-Ambient

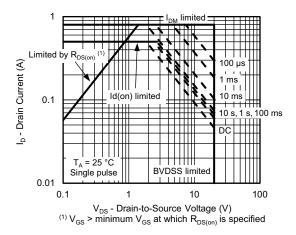




Current Derating a



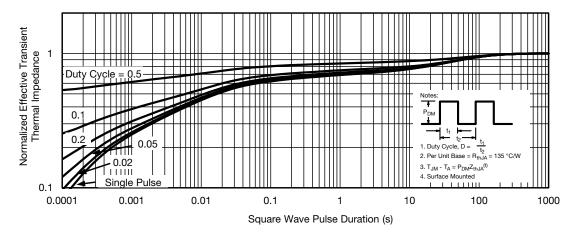
Power, Junction-to-Ambient



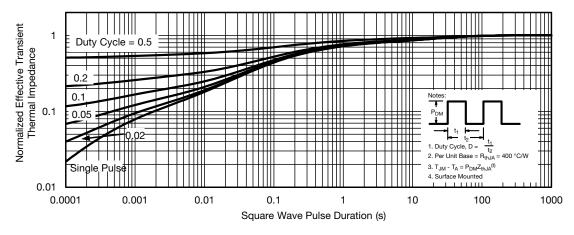
Safe Operating Area, Junction-to-Ambient

a. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with maximum copper)

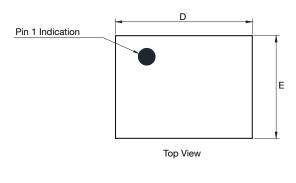


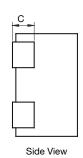
Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with minimum copper)

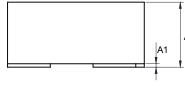
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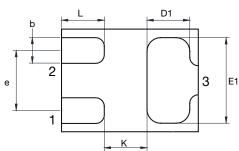
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Case Outline for PowerPAK 0.8 mm x 0.6 mm









Bottom View

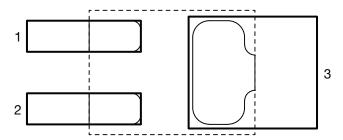
	MILLIMETERS				INCHES	
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
Α	0.350	0.380	0.400	0.0138	0.0150	0.0157
A1	0	-	0.020	0	-	0.0008
b	0.120	0.150	0.180	0.0047	0.0059	0.0071
С	0.119	0.127	0.135	0.0047	0.0050	0.0053
D	0.750	0.800	0.850	0.0295	0.0315	0.0335
D1	0.200	0.250	0.300	0.0078	0.0098	0.0118
E	0.550	0.600	0.650	0.0217	0.0236	0.0256
E1	0.450	0.500	0.550	0.0177	0.0197	0.0217
е	0.300	0.350	0.400	0.0118	0.0138	0.0158
K	0.150	0.250	0.350	0.0058	0.0098	0.0138
L	0.200	0.250	0.300	0.0078	0.0098	0.0118

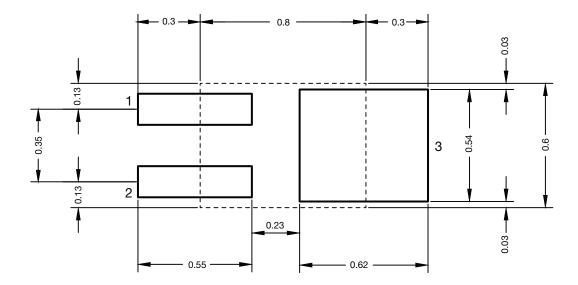
ECN: C13-1574-Rev. A, 23-Dec-13

DWG: 6020



Recommended Land Pattern PowerPAK® 0806









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