# Microtronix

# Firefly II Module

## USER MANUAL

**Revision 1.2.1**

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This datasheet provides information regarding the Firefly II module. The following table shows the document revision history.

| Document Revision History | |
|---|---|
| **Date** | **Description** |
| January 2006 | Initial Release – Version 1.0 |
| July 2008 | Add mechanical information – Version 1.2 |
| August 2013 | Update mechanical drawing – Version 1.2.1 |

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## Typographic Conventions

| | |
|---|---|
| **Path/Filename** | A path/filename |
| `[SOPC Builder]$ <cmd>` | A command that should be run from within the Cygwin Environment. |
| `…sdk/<path>` | A file that is relative to the sdk directory. |
| `Code` | Sample code. |
| ↵ | Indicates that there is no break between the current line and the next line. |

## Table of Contents

## Features

- Altera EP2C20, EP2C35 or EP2C50 484-pin Cyclone II FPGA
- Altera EPCS16 Serial Configuration Device
- 16, 32 or 64MB PC133 SDRAM
- 8, 16, 32 or 64MB Flash
- 4-wire RS-232 Transceiver
- 24MHz oscillator
- 95 User I/O pins
- User accessible PLL (2 input pins, 2 output pins)
- JTAG port
- Optional Active Serial programming port (reduces I/O to 88)
- Supports Nios II soft core processor and uClinux operating system
- Supports self-reconfiguration of FPGA from logic in FPGA

## General Description

The Firefly II Module is intended to provide a drop-in uClinux system for embedded systems. It provides a Cyclone II FPGA for a Nios II soft-core processor as well as enough SDRAM and Flash to run the uClinux operating system. A large I/O count allows the module to be used in many diverse applications. Communication and programming is provided through Altera's standard utilities.

### *Reference Design*

The Microtronix Firefly II Module ships with a reference design that connects all of the devices on the module. It is a Nios II based system that boots uClinux from the flash. Communication is provided through the JTAG port and can be initiated using Altera's nios2-terminal utility.

## Board Components

This section describes the various components and sub-circuits of the Microtronix Firefly II Module. For each component or circuit, this section explains: basic function, performance limits and I/O requirements. Figure 1 shows the location of all the Firefly II components mentioned in this section.

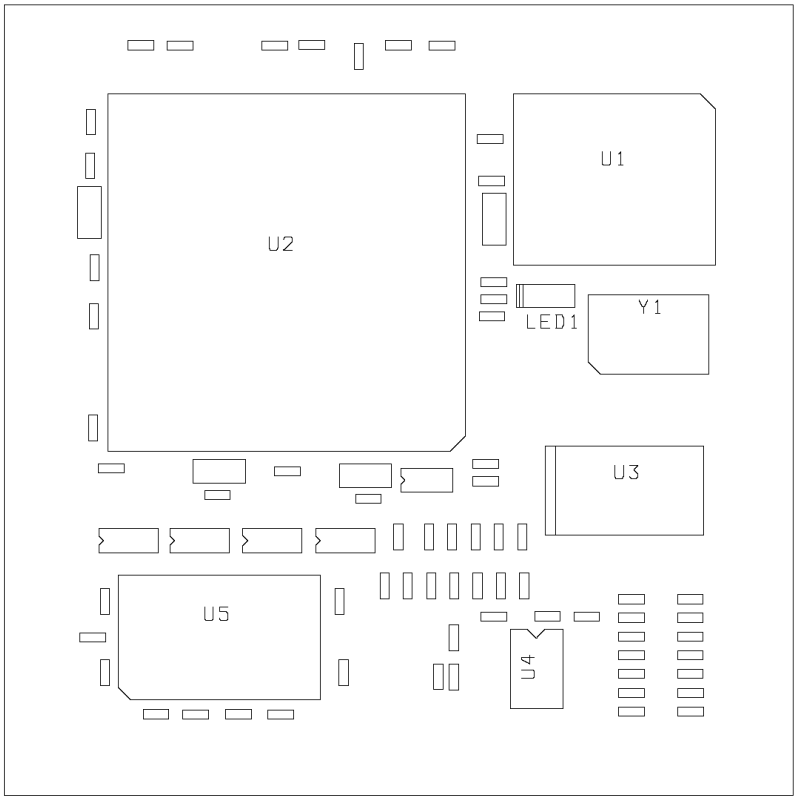


**Figure 1: Firefly II Components**

### *Cyclone FPGA*

**U2** is an Altera Cyclone II FPGA. EP2C20F484C8N, EP2C35F484C8N, or EP2C50F484C8N FPGA device in a 484 pin FineLine BGA® package. Table 1 lists the Cyclone II device features.

**Table 1: Cyclone II Device Features**

| | EP2C20 | EP2C35 | EP2C50 |
|---|---|---|---|
| LEs | 18,752 | 33,216 | 50,528 |
| M4K RAM Blocks | 52 | 105 | 129 |
| Total RAM Bits | 239,616 | 483,840 | 594,432 |
| Embedded multipliers | 26 | 35 | 86 |

The Cyclone II is configured on power-up by the EPCS16 serial configuration device (U3). It can also be configured through the JTAG port using Altera's FPGA programming tool.

See the Altera Cyclone II literature page for Cyclone II related documentation at http://www.altera.com/literature/lit-cyc2.jsp.

### *Serial Configuration Device*

**U3** is an Altera EPCS16 Serial Configuration Device. This device is a serial flash device with additional state machine logic for handshaking with the Active Serial Programming feature of the Cyclone FPGA. After a Power-On or Board Reset event, the Cyclone II FPGA and Serial Configuration Device work together to load a design from the flash memory of the configuration device into Cyclone II FPGA SRAM cells. Once configuration is complete, the new core starts running.

Detailed information about the configuration device, as well as design file sizes, can be found in Table 2 below.

**Table 2: Serial Configuration Device**

| | |
|---|---|
| Max Serial Clock Frequency | 20MHz |
| Power On Reset Time | 100ms |
| Compression Performance | 35-60% |
| Flash Memory Size (bits) | 16,777,216 |
| Max Uncompressed Design Size (2C20) (bits) | 3,892,496 |
| Min area left for general use (2C20) (bits) | 12,884,720 |
| Max Uncompressed Design Size (2C35) | 6,848,608 |
| Min area left for general use (2C35) | 9,928,608 |
| Max Uncompressed Design Size (2C50) | 9,951,104 |
| Min area left for general use (2C50) | 6,826,112 |

The minimum area left for general use in the flash memory of the configuration device can be used by software running on a soft core processor in the Cyclone II FPGA (such as an Altera Nios II) to store configuration information, programs, other compressed core designs, etc.

The Serial Configuration Device also supports compression of the designs being held within it. The compression is enabled from the Quartus II design tool when compiling a logic design. The Active Serial Programming Device will send a compressed data bit stream to the Cyclone II FPGA, which will decompress the data locally in real time and use the uncompressed data to program its SRAM-based logic cells.

See the Altera configuration literature page for EPCS related documentation at http://www.altera.com/literature/lit-config.jsp.

### *Flash*

**U1** is an 8, 16, 32 or 64MB Spansion CFI-compatible flash. The flash sits on its own 16-bit dedicated bus. The flash device can be programmed directly by hardware and software on the Cyclone II or indirectly through the JTAG port using Altera's flash programming utilities. For more information see the S29GLxxxM (8MB) or S29GLxxxN (16, 32, 64MB) datasheet.

### *SDRAM*

**U5** is a 16, 32 or 64 MB Micron SDRAM chip (4, 8 or 16M x 32-bit) chip with a 7ns access time (PC133 compatible SDR SDRAM). The SDRAM exists as a 32-bit wide device on its own dedicated bus. The SDRAM clock input is connected to FPGA PLL3 output pin D5. The 24MHz oscillator drives this PLL. For more information see the ISSI IS42S32160C-6BLI (64MB) or the Micron MT48LC4M32B2 (16MB), MT48LC8M32B2 (32MB) or MT48LC16M32S2 (64MB) datasheets.

### *RS-232*

**U4** is a Texas Instruments MAX3232 4-wire UART transceiver (2 input, 2 output), capable of 250 Kbps transfer rate (max). For more information see the MAX3232 datasheet.

### *Clock*

**Y1** is a 24MHz oscillator. It is connected to the Cyclone II PLL3 through pin A12. The external output of this PLL is pin D5. It is connected to the clock input of the SDRAM device.

### *Module Connector*

Around the bottom of the module is a double row of 0.1" (2.54mm) pitch pins. The recommended connectors for mating with the Firefly II are Samtec's SSW series. Four dual-row 36-pin sockets are required (SSW-118-21-G-D).

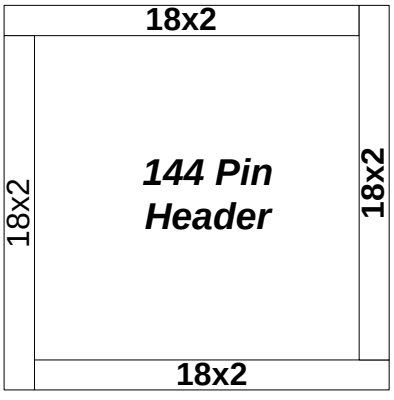


**Figure 2: Firefly II Connector**

### *Module I/O Connector Pinnings*

The module's general-purpose I/O pins are divided into four groups. On the schematic these groups are labeled EPM_A, EPM_B, EPM_C and EPM_D. Two of these groups (EPM_A and EPM_B) are powered from a set of three power pins (module pins B3, B4, A11) allowing these I/Os to operate at voltages other than 3.3V if desired. Additionally, EPM_A and EPM_B signals are routed in pairs to allow for differential signaling (see Appendix B). For Cyclone II supported I/O standards, see the Cyclone II documentation at http://www.altera.com/literature/lit-cyc2.jsp.

For full pin listings, see Appendices A and B.

### *Module Board Mechanical Diagram*

A mechanical drawing of the board is shown below.

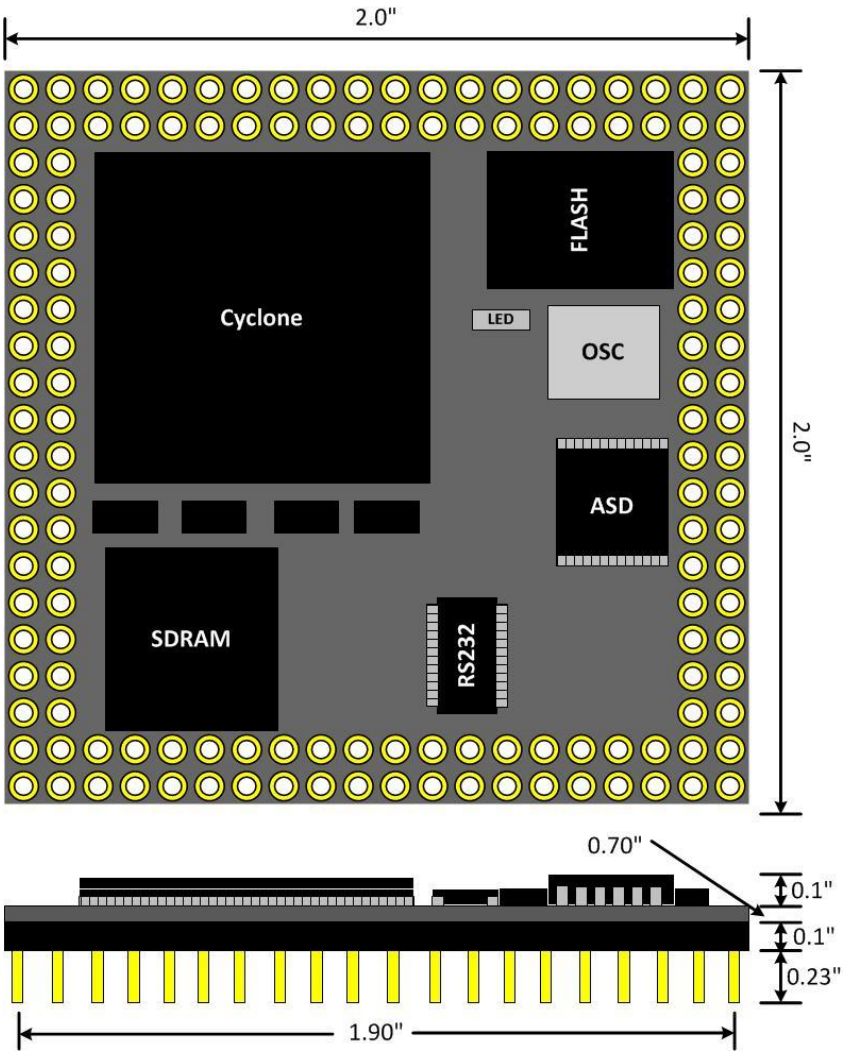


**Figure 3: Firefly II Mechanical Drawing**

## SOPC Builder Components

This section describes how to interface to the various components and sub-circuits of the Microtronix Firefly II using Altera SOPC Builder 5.0.

### *Serial Configuration Device*

The minimum area left for general use in the flash memory of the configuration device can be used by software running on a soft core processor in the Cyclone II FPGA (such as an Altera Nios II) to store configuration information, programs, other compressed core designs, etc. If an Altera Nios II based system is running on the FPGA, the EPCS Serial Flash Controller SOPC component, along with software routines provided by the HAL can be used to access the portions of EPCS flash memory that are not being used to hold the core design.

The Serial Configuration Device also supports compression of the designs being held within it. The compression is enabled from the Quartus II design tool when compiling a logic design. The Active Serial Programming Device will send a compressed data bit stream to the Cyclone II FPGA, which will decompress the data locally in real time and use the uncompressed data to program its SRAM-based logic cells.

See the Altera configuration literature page for EPCS related documentation at http://www.altera.com/literature/lit-config.jsp.

### *Flash*

Interfacing the FLASH with a SOPC based system can be easily accomplished using the “Flash Memory (Common Flash Interface)” SOPC component available that comes with Altera’s Nios II distribution. For proper operation, use the following parameters with the SOPC component: data width 16 bits, setup 35ns, wait 110ns, hold 45ns. The address width depends on the flash size: 23 bits for 16MB, 24 bits for 32MB and 25 bits for 64MB. This component also requires it’s own “Avalon Tri-State Bridge” to connect to the CPU. See n2cpu_nii51013.pdf in the Nios II documents subdirectory for further details.

### *SDRAM*

Interfacing the SDRAM with a SOPC based system can be easily accomplished using the Altera SDRAM SOPC component (see n2cpu_nii51005.pdf in the Nios II documents subdirectory for further details). The SDRAM chip used on the module requires slight changes from a pre-defined chip in the SDRAM SOPC component. First, choose “single Micron MT48LC4M32B2-7 chip” from the “Presets:” list. Next, adjust the row and column values based on the size of SDRAM on the module: for 16MB, no change is necessary; for 32 MB, enter 9

into the Column box; for 64MB, enter 13 into the Row box and 9 into the Column box.

Along with the SOPC builder component, the SDRAM requires a clock signal. This signal should be provided by a PLL megafunction in Quartus II. Pin A12 should be used as the input clock (24MHz on-module oscillator) and pin D5 should be used as the output to the SDRAM. The frequency of the output should match the frequency of the SOPC Builder system.

### *RS-232*

**U4** in Figure 1 is a Maxim Semiconductor MAX3232 4-wire UART transceiver (2 input, 2 output), capable of 115,200 baud transfer rate (max).

## External Support Circuitry

This section describes the support circuitry required by the Firefly II Module.

### *Power Supply*

Two different voltages are required to power the Firefly II Module. Peripherals and Cyclone II I/O require 3.3V while the Cyclone II core requires 1.2V.

Due to the nature of FPGA technology, their power requirements vary greatly depending on how they are configured. Fortunately, Altera provides a tool for estimating Cyclone II power requirements. It can be found on the Altera web site at http://www.altera.com/support/devices/estimator/pow-powerplay.html.

Power calculations for the 3.3V supply must take into account the power requirements of the Firefly II on-board peripherals (SDRAM, Flash, etc). The maximum current requirement for all 3.3V devices (excluding the Cyclone II) is 500mA.

The Firefly II is targeted at Nios II based FPGA designs. For such applications, the recommended power supplies are shown in . These values are sufficient to power Nios II based Firefly II designs.

**Table 3: Recommended Supply Current, Nios II Based Application**

| Voltage | Current |
|---|---|
| 3.3V | 1 A |
| 1.2V | 2 A |

The Firefly II Module allows for a separate VCCIO power supply for I/O banks IO_A and IO_B. Requirements for this supply can be estimated using the Altera power utility indicated above. If a separate I/O voltage is not required, VCCIO can be powered from the 3.3V VCC source.

A number of companies provide resources specifically targeted at designing power supplies for Altera FPGAs. Two such companies are Linear Technologies (http://www.linear.com/designtools/Altera.jsp) and Texas Instruments (http://www.ti.com/alterafpga).

### *JTAG*

A 10-pin, dual-row, 0.1” (2.54mm) pitch header is required for JTAG programming and communication. Figure 4 shows the connections required to support Altera JTAG programming hardware.

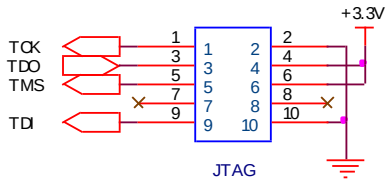


**Figure 4: JTAG Circuitry**

### *Active Serial (Optional)*

A Firefly II assembly option allows for direct access to the EPCS16 serial configuration device. A 10-pin, dual-row, 0.1" (2.54mm) pitch header is required for programming this device. Figure 5 shows the connections required to support Altera active serial programming hardware.

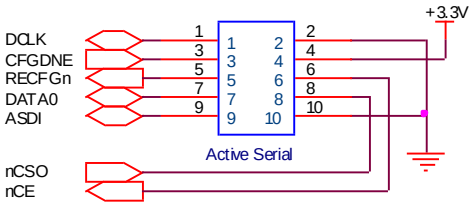


**Figure 5: Active Serial Circuitry**

## Appendix A: Firefly II Module Pins

This section describes all of the pins on the Firefly II module. It also includes pin diagrams for the two module variations affecting the pin functions.

**Table 4: Pin Descriptions**

| Name | Description |
|---|---|
| IO_A[29..0] | General-Purpose I/O powered by VCCIO |
| IO_B[15..0] | General-Purpose I/O powered by VCCIO |
| IO_C[27..0] | General-Purpose I/O powered by VCC (3.3V) |
| IO_D[20..0] | General-Purpose I/O powered by VCC (3.3V) |
| RXD, RTS | RS-232 input to FPGA |
| TXD, CTS | RS-232 output from FPGA |
| CLK_IN+, CLK_IN- | External clock input to FPGA PLL4 |
| CLK_OUT+, CLK_OUT- | Output from FPGA PLL4 |
| TDI, TDO, TMS, TCK | JTAG port for FPGA configuration |
| ASDI, DATA0, RECFGn, CFGDNE, DCLK, nCSO, nCE | Active Serial port for directly programming Serial Configuration Device.<br>Assembly option, replaces IO_C[27..21] |
| VCC | 3.3V, on-board peripheral and I/O power |
| VCORE | 1.2V, FPGA core power |
| VCCIO | I/O power for IO_A and IO_B |
| GND | Ground |

**Table 5: Pin Numbers**

| Pin # | Pin |
|---|---|
| C1 | IO_A0 |
| D1 | IO_A1 |
| E1 | IO_A2 |
| F1 | IO_A3 |
| G1 | IO_A4 |
| K1 | IO_A5 |
| L1 | IO_A6 |
| N1 | IO_A7 |
| P1 | IO_A8 |
| T1 | IO_A9 |
| U1 | IO_A10 |
| V1 | IO_A11 |
| X1 | IO_A12 |
| A2 | IO_A13 |
| B2 | IO_A14 |
| C2 | IO_A15 |
| D2 | IO_A16 |
| F2 | IO_A17 |
| G2 | IO_A18 |
| H2 | IO_A19 |
| K2 | IO_A20 |
| L2 | IO_A21 |
| N2 | IO_A22 |
| P2 | IO_A23 |
| R2 | IO_A24 |
| T2 | IO_A25 |
| U2 | IO_A26 |
| W2 | IO_A27 |
| X2 | IO_A28 |
| Y2 | IO_A29 |
| A9 | IO_B0 |
| A10 | IO_B1 |

| Pin # | Pin |
|---|---|
| A12 | IO_B2 |
| A13 | IO_B3 |
| A15 | IO_B4 |
| A16 | IO_B5 |
| A17 | IO_B6 |
| B8 | IO_B7 |
| B9 | IO_B8 |
| B10 | IO_B9 |
| B12 | IO_B10 |
| B13 | IO_B11 |
| B14 | IO_B12 |
| B15 | IO_B13 |
| B16 | IO_B14 |
| B18 | IO_B15 |
| A19 | IO_C0 |
| B19 | IO_C1 |
| C19 | IO_C2 |
| E19 | IO_C3 |
| F19 | IO_C4 |
| G19 | IO_C5 |
| H19 | IO_C6 |
| K19 | IO_C7 |
| M19 | IO_C8 |
| N19 | IO_C9 |
| P19 | IO_C10 |
| B20 | IO_C11 |
| D20 | IO_C12 |
| E20 | IO_C13 |
| F20 | IO_C14 |
| H20 | IO_C15 |
| K20 | IO_C16 |
| M20 | IO_C17 |
| N20 | IO_C18 |
| R20 | IO_C19 |
| T20 | IO_C20 |
| V19 | IO_C21 / nCSO |
| W19 | IO_C22 / nCE |
| U20 | IO_C23 / ASDI |
| V20 | IO_C24 / DATA0 |
| W20 | IO_C25 / RECFGn |
| X20 | IO_C26 / CFGDNE |
| Y20 | IO_C27 / DCLK |
| Y4 | IO_D0 |
| Y5 | IO_D1 |
| Y6 | IO_D2 |
| Y8 | IO_D3 |
| Y9 | IO_D4 |
| Y11 | IO_D5 |
| Y12 | IO_D6 |
| Y14 | IO_D7 |
| Y15 | IO_D8 |
| Y16 | IO_D9 |
| X3 | IO_D10 |
| X5 | IO_D11 |
| X6 | IO_D12 |
| X7 | IO_D13 |
| X8 | IO_D14 |
| X9 | IO_D15 |
| X11 | IO_D16 |
| X12 | IO_D17 |
| X13 | IO_D18 |
| X14 | IO_D19 |
| X15 | IO_D20 |

| Pin # | Pin |
|---|---|
| Y18 | RXD |
| X17 | RTS |
| Y17 | TXD |
| X18 | CTS |
| A7 | CLK_IN+ |
| B7 | CLK_IN- |
| A6 | CLK_OUT+ |
| B6 | CLK_OUT- |
| A18, C20, L20, M1, W1, X19, Y3, Y10 | VCC |
| R19, T19 | VCORE |
| A10, B3, B4 | VCCIO |
| A8, A14, A20, B1, B5, B11, B17, D19, E2, G20, H1, L19, M2, P20, R1, U19, V2, X4, X10, X16, Y1, Y7, Y13, Y19 | GND |

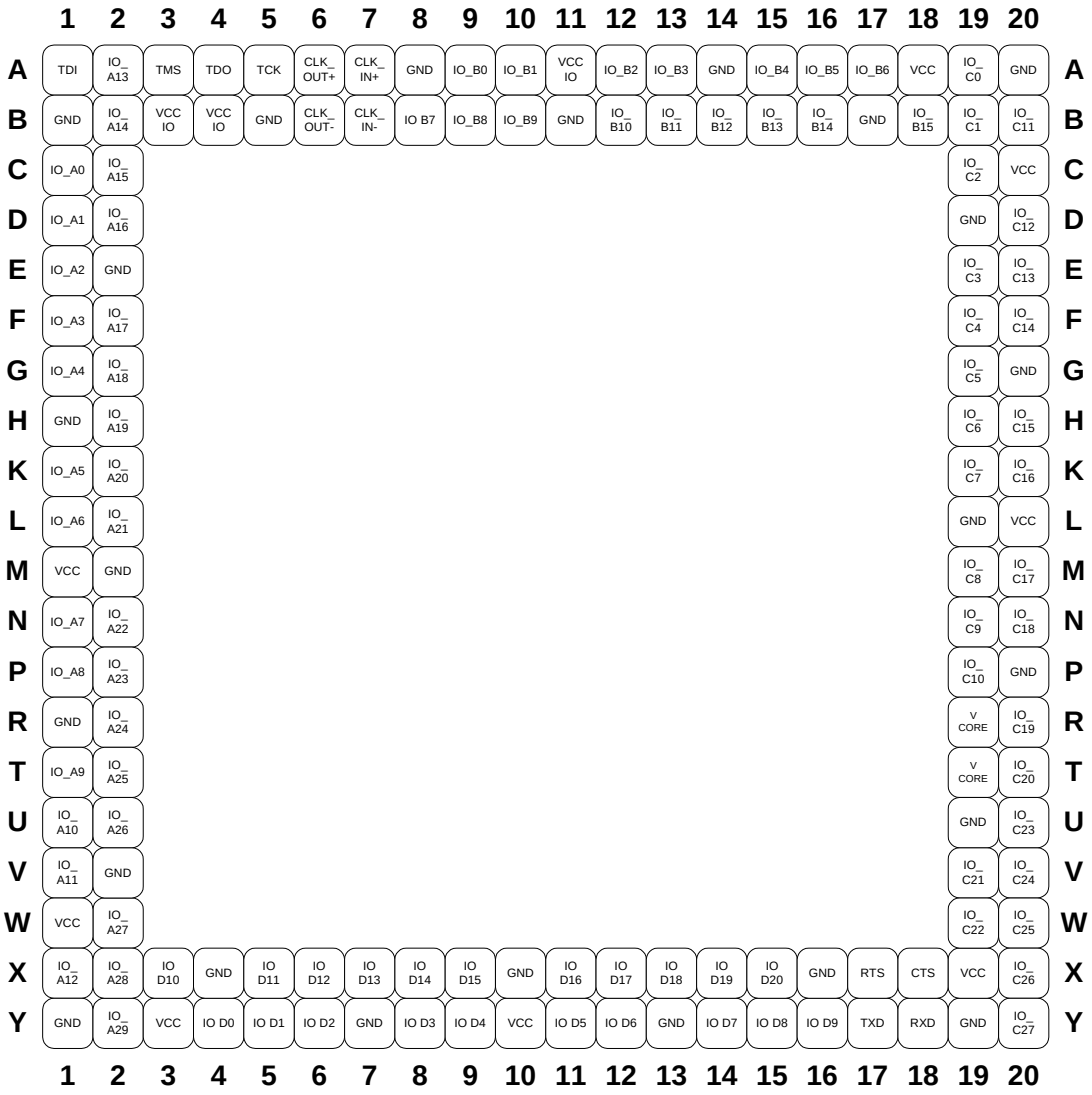


**Figure 6: Pin Diagram (Default Configuration)**

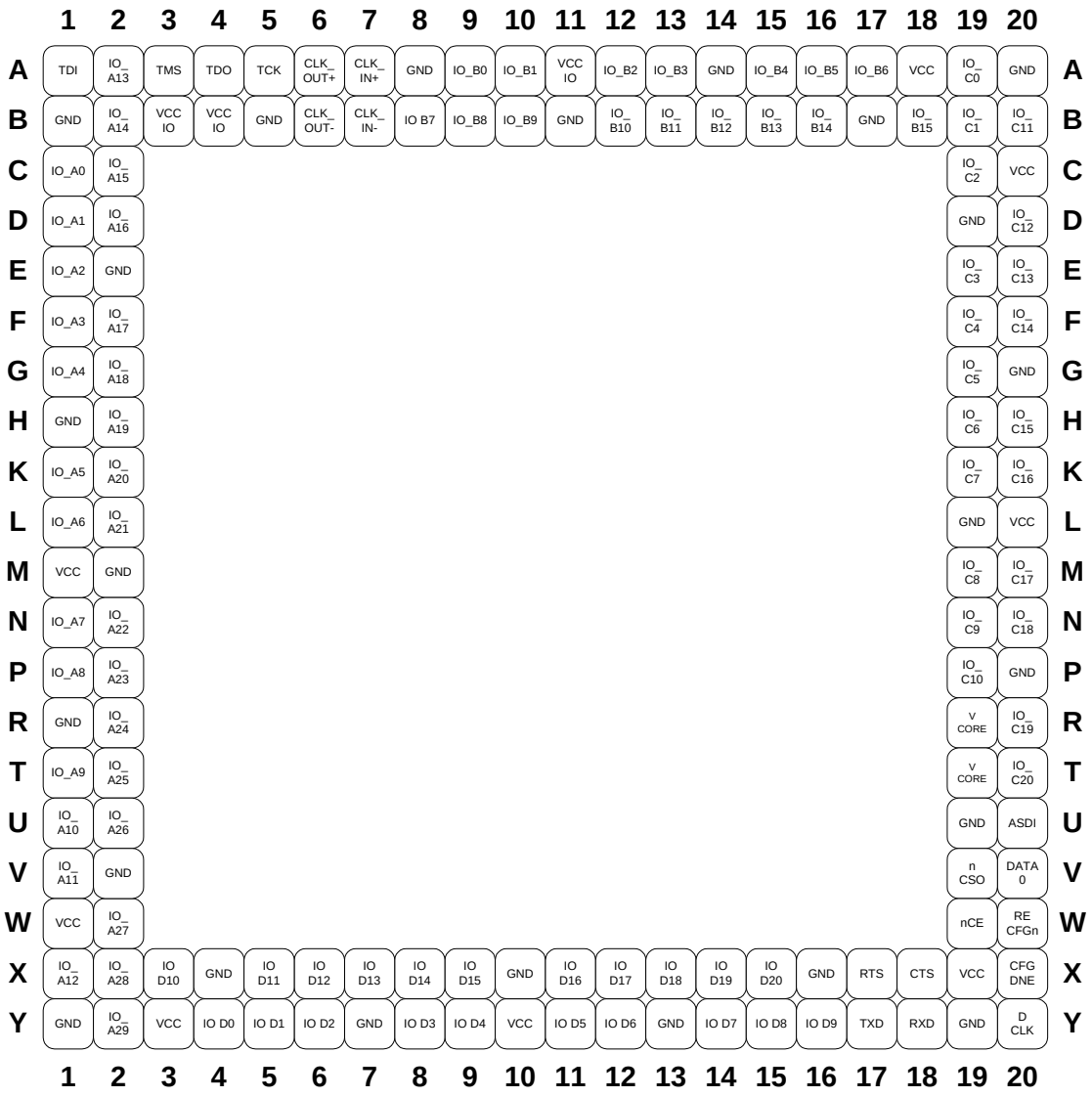


**Figure 7: Pin Diagram (Active Serial Option)**

## Appendix B: Cyclone II FPGA Pins

The following table lists all of the pin connections to the Cyclone II device from the components on the Firefly II Module.

| Cyclone II Pin # | Signal | Connected to… | Comments |
|---|---|---|---|
| H6 | FLASH_A0 | FLASH (U1) *Address* | |
| H5 | FLASH_A1 | | |
| J4 | FLASH_A2 | | |
| J1 | FLASH_A3 | | |
| J2 | FLASH_A4 | | |
| H4 | FLASH_A5 | | |
| H3 | FLASH_A6 | | |
| H1 | FLASH_A7 | | |
| F2 | FLASH_A8 | | |
| F1 | FLASH_A9 | | |
| E2 | FLASH_A10 | | |
| F4 | FLASH_A11 | | |
| D1 | FLASH_A12 | | |
| E1 | FLASH_A13 | | |
| D2 | FLASH_A14 | | |
| E3 | FLASH_A15 | | |
| E4 | FLASH_A16 | | |
| H2 | FLASH_A17 | | |
| G3 | FLASH_A18 | | |
| G6 | FLASH_A19 | | |
| G5 | FLASH_A20 | | |
| F3 | FLASH_A21 | | |
| C1 | FLASH_A22 | | |
| C2 | FLASH_A23 | FLASH (U1) *Address* | Used for optional 32MB FLASH |
| N4 | FLASH_A24 | FLASH (U1) *Address* | Used for optional 64MB FLASH |
| Y1 | FLASH_DQ0 | FLASH (U1) *Data (16-bit)* | |
| W3 | FLASH_DQ1 | | |
| W1 | FLASH_DQ2 | | |
| T3 | FLASH_DQ3 | | |
| P3 | FLASH_DQ4 | | |
| P1 | FLASH_DQ5 | | |
| N3 | FLASH_DQ6 | | |
| N1 | FLASH_DQ7 | | |
| V2 | FLASH_DQ8 | | |
| W2 | FLASH_DQ9 | | |
| U2 | FLASH_DQ10 | | |
| U3 | FLASH_DQ11 | | |
| T2 | FLASH_DQ12 | | |
| P2 | FLASH_DQ13 | | |
| R2 | FLASH_DQ14 | | |
| N2 | FLASH_DQ15 | | |
| Y3 | FLASH_OEn | FLASH (U6) *Control* | |
| R1 | FLASH_WEn | | |
| Y2 | FLASH_CEn | | |
| V1 | FLASH_RY/BYn | | |
| U1 | FLASH_WPn | | FLASH_WPn must be high to enable writing to the FLASH. A low signal will enable write-protect. |
| T1 | FLASH_RESETn | | |

| Cyclone II Pin # | Signal | Connected to… | Comments |
|---|---|---|---|
| N6 | RECONFIGn | CONFIGURATION CIRCUIT | Toggling this line will force the Cyclone FPGA to reconfigure itself using the Data in the Serial Configuration Device (U3) |
| A15 | SDRAM_A0 | SDRAM (U5) *Address* | |
| A14 | SDRAM_A1 | | |
| B20 | SDRAM_A2 | | |
| B18 | SDRAM_A3 | | |
| D14 | SDRAM_A4 | | |
| C16 | SDRAM_A5 | | |
| B17 | SDRAM_A6 | | |
| D15 | SDRAM_A7 | | |
| C17 | SDRAM_A8 | | |
| B14 | SDRAM_A9 | | |
| B19 | SDRAM_A10 | | |
| A16 | SDRAM_A11 | | |
| B16 | SDRAM_A12 | SDRAM (U5) *Address* | Used for optional 64MB SDRAM |
| A4 | SDRAM_DQ0 | SDRAM (U5) *Data (32-bit)* | |
| A7 | SDRAM_DQ1 | | |
| A5 | SDRAM_DQ2 | | |
| A8 | SDRAM_DQ3 | | |
| A6 | SDRAM_DQ4 | | |
| A10 | SDRAM_DQ5 | | |
| A9 | SDRAM_DQ6 | | |
| A11 | SDRAM_DQ7 | | |
| B11 | SDRAM_DQ8 | | |
| B10 | SDRAM_DQ9 | | |
| B9 | SDRAM_DQ10 | | |
| B6 | SDRAM_DQ11 | | |
| B7 | SDRAM_DQ12 | | |
| A3 | SDRAM_DQ13 | | |
| B8 | SDRAM_DQ14 | | |
| B5 | SDRAM_DQ15 | | |
| B4 | SDRAM_DQ16 | | |
| E7 | SDRAM_DQ17 | | |
| D7 | SDRAM_DQ18 | | |
| F9 | SDRAM_DQ19 | | |
| F8 | SDRAM_DQ20 | | |
| C9 | SDRAM_DQ21 | | |
| C7 | SDRAM_DQ22 | | |
| D8 | SDRAM_DQ23 | | |
| D11 | SDRAM_DQ24 | | |
| E9 | SDRAM_DQ25 | | |
| E11 | SDRAM_DQ26 | | |
| F11 | SDRAM_DQ27 | | |
| C10 | SDRAM_DQ28 | | |
| D9 | SDRAM_DQ29 | | |
| F10 | SDRAM_DQ30 | | |
| E8 | SDRAM_DQ31 | | |
| A20 | SDRAM_DQM0 | SDRAM (U5) *Byte Enables* | |
| D16 | SDRAM_DQM1 | | |
| A13 | SDRAM_DQM2 | | |
| C13 | SDRAM_DQM3 | | |
| A19 | SDRAM_BA0 | SDRAM (U5) *Bank Address* | |
| A17 | SDRAM_BA1 | | |
| A18 | SDRAM_RASn | SDRAM (U5) *Control* | |
| C18 | SDRAM_CASn | | |
| B13 | SDRAM_WEn | | |
| B15 | SDRAM_CSn | | |

| Cyclone II Pin # | Signal | Connected to… | Comments |
|---|---|---|---|
| C14 | SDRAM_CKE | SDRAM (U5) *Control* | |
| D5 | SDRAM_CLK | SDRAM (U5) *Clock* | |
| M5 | RS232_TXD | RS-232 (U4) | |
| M6 | RS232_RXD | | |
| P6 | RS232_CTS | | |
| P5 | RS232_RTS | | |
| A12 | FPGA_PLL_IN_A | Oscillator (Y1) | 24 MHz |

The following table lists all of the pin connections to the Cyclone II device from the external pins of the Firefly II Module.

| Cyclone II Pin # | Firefly II Pin | Connected to… | Comments |
|---|---|---|---|
| AA20 | IO_A0 | FPGA (U2) *Bank 7* | Paired with A_14 |
| AA19 | IO_A1 | | Paired with A_15 |
| AA18 | IO_A2 | | Paired with A_16 |
| AA17 | IO_A3 | | Paired with A_17 |
| AA16 | IO_A4 | | Paired with A_18 |
| AA15 | IO_A5 | | Paired with A_20 |
| AA14 | IO_A6 | | Paired with A_21 |
| AA13 | IO_A7 | | Paired with A_22 |
| AA12 | IO_A8 | | Paired with A_23 |
| W16 | IO_A9 | | Paired with A_25 |
| W15 | IO_A10 | | Paired with A_26 |
| U15 | IO_A11 | | Paired with A_27 |
| U13 | IO_A12 | | |
| Y16 | IO_A13 | | |
| AB20 | IO_A14 | | Paired with A_0 |
| AB19 | IO_A15 | | Paired with A_1 |
| AB18 | IO_A16 | | Paired with A_2 |
| AB17 | IO_A17 | | Paired with A_3 |
| AB16 | IO_A18 | | Paired with A_4 |
| Y13 | IO_A19 | | |
| AB15 | IO_A20 | | Paired with A_5 |
| AB14 | IO_A21 | | Paired with A_6 |
| AB13 | IO_A22 | | Paired with A_7 |
| AB12 | IO_A23 | | Paired with A_8 |
| U14 | IO_A24 | | |
| Y17 | IO_A25 | | Paired with A_9 |
| Y14 | IO_A26 | | Paired with A_10 |
| V15 | IO_A27 | | Paired with A_11 |
| W14 | IO_A28 | | Paired with A_29 |
| V14 | IO_A29 | | Paired with A_28 |
| AB10 | IO_B0 | FPGA (U2) *Bank 8* | Paired with B_8 |
| AB9 | IO_B1 | | Paired with B_9 |
| AB8 | IO_B2 | | Paired with B_10 |
| AB7 | IO_B3 | | Paired with B_11 |
| AB6 | IO_B4 | | Paired with B_12 |
| AB5 | IO_B5 | | Paired with B_13 |
| AB4 | IO_B6 | | Paired with B_14 |
| AA11 | IO_B7 | | |
| AA10 | IO_B8 | | Paired with B_0 |
| AA9 | IO_B9 | | Paired with B_1 |
| AA8 | IO_B10 | | Paired with B_2 |
| AA7 | IO_B11 | | Paired with B_3 |
| AA6 | IO_B12 | | Paired with B_4 |
| AA5 | IO_B13 | | Paired with B_5 |
| AA4 | IO_B14 | | Paired with B_6 |
| AB3 | IO_B15 | | |

| Cyclone II Pin # | Signal | Connected to… | Comments |
|---|---|---|---|
| Y22 | IO_C0 | FPGA (U2) *Bank 6* | |
| W22 | IO_C1 | | |
| V22 | IO_C2 | | |
| U22 | IO_C3 | | |
| T22 | IO_C4 | | |
| R22 | IO_C5 | | |
| Y19 | IO_C6 | | |
| Y20 | IO_C7 | | |
| V20 | IO_C8 | | |
| U20 | IO_C9 | | |
| R20 | IO_C10 | | |
| Y21 | IO_C11 | | |
| W21 | IO_C12 | | |
| V21 | IO_C13 | | |
| U21 | IO_C14 | | |
| T21 | IO_C15 | | |
| R21 | IO_C16 | | |
| Y18 | IO_C17 | | |
| U19 | IO_C18 | | |
| R19 | IO_C19 | | |
| R18 | IO_C20 | | |
| N22 | IO_C21 | | Optionally used for direct active serial programming. |
| N21 | IO_C22 | | |
| R17 | IO_C23 | | |
| P18 | IO_C24 | | |
| P17 | IO_C25 | | |
| M19 | IO_C26 | | |
| M18 | IO_C27 | | |
| C21 | IO_D0 | FPGA (U2) *Bank 5* | |
| D21 | IO_D1 | | |
| E21 | IO_D2 | | |
| F21 | IO_D3 | | |
| G21 | IO_D4 | | |
| C19 | IO_D5 | | |
| D19 | IO_D6 | | |
| F20 | IO_D7 | | |
| G18 | IO_D8 | | |
| H18 | IO_D9 | | |
| C22 | IO_D10 | | |
| D22 | IO_D11 | | |
| E22 | IO_D12 | | |
| F22 | IO_D13 | | |
| G22 | IO_D14 | | |
| J22 | IO_D15 | | |
| C20 | IO_D16 | | |
| D20 | IO_D17 | | |
| E20 | IO_D18 | | |
| G20 | IO_D19 | | |
| H19 | IO_D20 | | |
| W12 | CLK_IN+ | FPGA (U2) *PLL4* | |
| V12 | CLK_IN- | | |
| T18 | CLK_OUT+ | | |
| U18 | CLK_OUT- | | |
| M5 | TXD | RS-232 (U4) | |
| M6 | RXD | | |
| P6 | CTS | | |
| P5 | RTS | | |