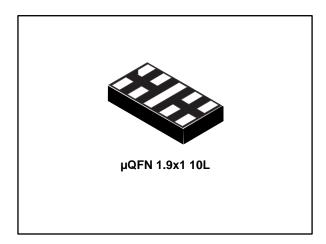
life.augmented

HSP051-4N10

4-line ESD protection for high speed lines

Datasheet - production data



Features

- Flow-through routing to keep signal integrity
- Ultralarge bandwidth: 10 GHz
- Ultralow capacitance:
 - 0.2 pF (I/O to I/O)
 - 0.35 pF (I/O to GND)
- Very low dynamic resistance: 0.48 Ω
- 100 Ω differential impedance
- Low leakage current: 100 nA at 25 °C
- Extended operating junction temperature range: -40 °C to 150 °C
- RoHS compliant

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards

Complies with the following standards

- MIL STD 883G-Method 3015-7: class 3B
 - 8 kV
- IEC 61000-4-2, level 4
 - 25 kV (air discharge)
 - 8 kV (contact discharge)

Applications

The HSP051-4N10 is designed to protect against electrostatic discharge on sub micron technology circuits driving:

- HDMI 1.4 and 2.0
- Digital video Interface
- Display port
- USB 3.0 and 3.1
- Serial ATA

Description

The HSP051-4N10 is a 4-channel ESD array with a rail to rail architecture designed specifically for the protection of high speed differential lines.

The ultralow variation of the capacitance ensures very low influence on signal-skew. The large bandwidth makes it compatible with HDMI 2.0 4K/2K (= 5.94 Gbps) and USB 3.1 (= 10 Gbps)

The device is packaged in μ QFN 1.9 mm x 1 mm with a 400 μ m pitch.

Figure 1: Functional schematic (top view)

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Characteristics HSP051-4N10

1 Characteristics

Table 1: Absolute maximum ratings (T_{amb} = 25 °C)

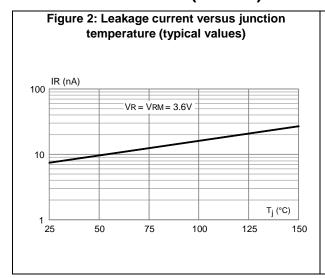
Symbol	Pa	Value	Unit	
V _{pp}	Peak pulse voltage	IEC61000-4-2 contact discharge	8	LAV
		IEC61000-4-2 air discharge	25	kV
T _{stg}	Storage junction temperature range		-65 to +150	
Tj	Operating junction temperature range		-40 to +150	°C
TL	Maximum lead temperature for soldering during 10 s		260	

Table 2: Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit	
V _{BR}	I _R = 1 mA		4.5	5.8		V	
I _{RM}	V _{RM} = 3.6 V			10	100	nA	
VcL	I _{PP} = 1 A, 8/20 μs				10	V	
VcL	IEC 61000-4-2, +8 kV contact (I _{PP} = 16 A), measured at 30 ns			13		V	
Rd	Dynamic resistance, pulse duration 100 ns	I/O to GND		0.48		Ω	
Κd		GND to I/O		0.96			
C1/0 - 1/0	V _{I/O} = 0 V	F = 200 MHz to 9 GHz		0.2	0.3	pF	
Cua	V _{I/O} = 0 V	F = 200 MHz to 2.5 GHz		0.4	0.55	pF	
CI/O - GND		F = 2.5 GHz to 9 GHz		0.35	0.45	pF	
fc	-3 dB			10		GHz	
Z _{diff}	Time domain reflectometry: $t_r = 200 \text{ ps } (10 - 90\%), Z_0 = 100 \Omega$		85	100	115	Ω	

HSP051-4N10 Characteristics

1.1 Characteristics (curves)



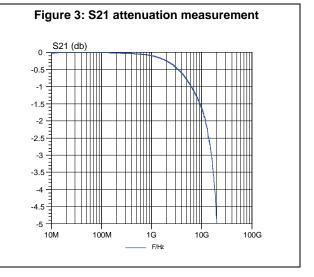
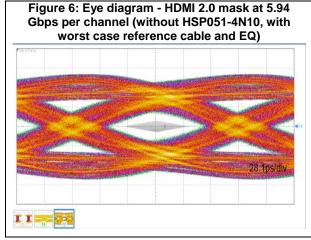
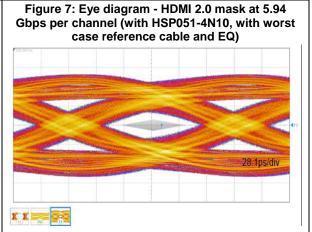


Figure 4: Eye diagram - HDMI mask at 3.4 Gbps per channel (without HSP051-4N10)

Figure 5: Eye diagram - HDMI mask at 3.4 Gbps per channel (with HSP051-4N10)



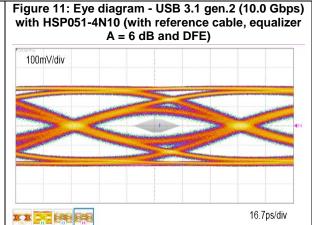


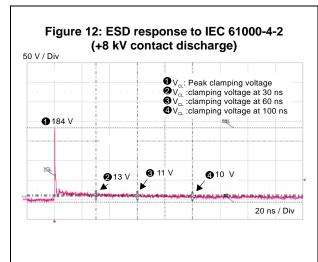
Characteristics HSP051-4N10

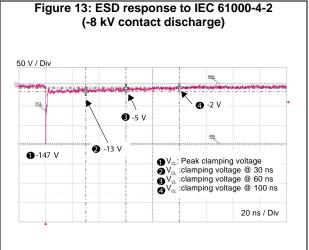
Figure 8: Eye diagram - USB 3.0 gen. 1 (5.0 Gbps) without HSP051-4N10 (with reference cable and equalizer)

Figure 9: Eye diagram - USB 3.0 gen. 1 (5.0 Gbps) with HSP051-4N10 (with reference cable and equalizer)

Figure 10: Eye diagram - USB 3.1 gen.2 (10.0 Gbps) without HSP051-4N10 (with reference cable, equalizer A = 6 dB and DFE)







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HSP051-4N10 Characteristics

 $V_{CL(V)}$

10

20 25

ns, rise time 10 ns, average window 70 ns 90ns)

IPP (A)

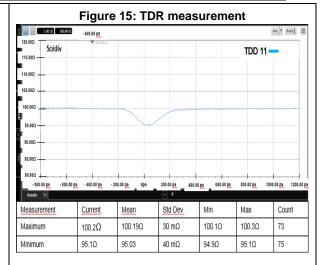
20
15
10
5

-5 -10

-15

-20 <u>-25 -20 -15 -10</u>

Figure 14: TLP measurement (pulse duration 100





HSP051-4N10 Package information

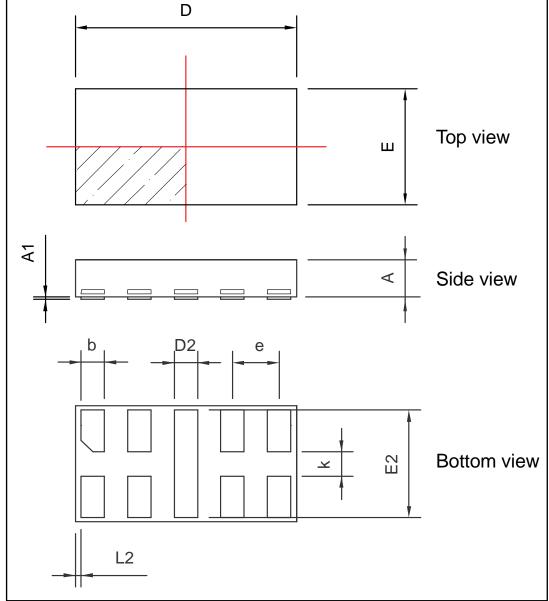
2 **Package information**

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 16: µQFN1.9x1 10L package outline

2.1 μQFN1.9x1 10L package information

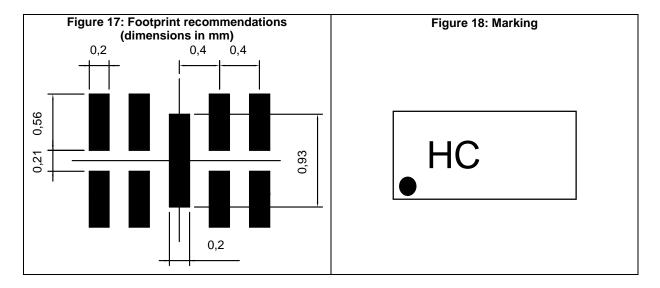
D



HSP051-4N10 Package information

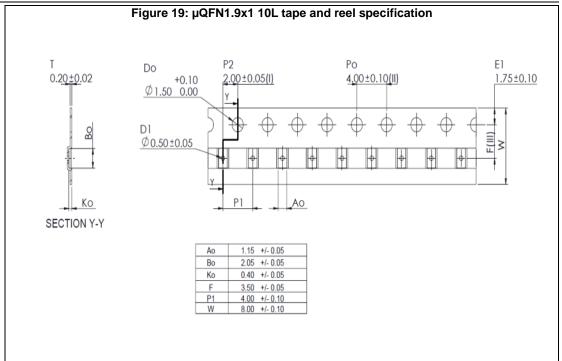
Table 3: µQFN1.9x1 10L package mechanical data

Table 5. par 141.5x1 102 parage mediament data					
	Dimensions Millimeters				
Ref.					
	Min.	Тур.	Max.		
А	0.28	0.32	0.35		
A1	0.00	0.02	0.05		
b	0.15	0.20	0.25		
D	1.85	1.90	1.95		
D2	0.15	0.20	0.25		
Е	0.95	1.00	1.05		
E2	0.88	0.93	0.98		
е		0.40			
k		0.21			
L2	0.02	0.05	0.07		





the marking codes can be rotated by 180° to differentiate assembly location. In no case should this product marking be used to orient the component for placement on a PCB. Only pin 1 mark is to be used for this purpose.



3 Recommendation on PCB assembly

0,14 0,4 0,4 0,4 0,4

Figure 20: Recommended stencil window position

3.1 Solder paste

- 1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
- 2. "No clean" solder paste is recommended.
- 3. Offers a high tack force to resist component movement during high speed.
- 4. Solder paste with fine particles: powder particle size is 20-45 μm.

3.2 Placement

- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
- 3. Standard tolerance of ± 0.05 mm is recommended.
- 4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- 5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- 6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.3 PCB design preference

- To control the solder paste amount, the closed via is recommended instead of open vias
- 2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.



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Via to GND

Via to GND

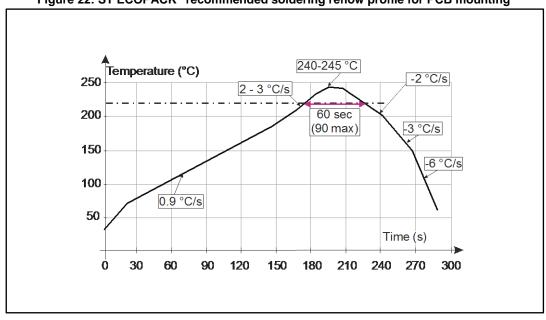
Footprint pad

PCB tracks

Figure 21: Printed circuit board layout recommendations

3.4 Reflow profile

Figure 22: ST ECOPACK $^{\circ}$ recommended soldering reflow profile for PCB mounting





Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

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HSP051-4N10 Ordering information

4 Ordering information

Figure 23: Ordering information scheme

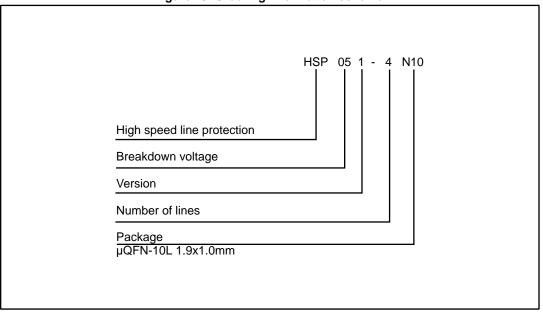


Table 4: Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
HSP051-4N10	HC	μQFN-10L	1.61 mg	7000	Tape and reel

5 Revision history

Table 5: Document revision history

Date	Revision	Changes	
11-Jul-2014	1	Initial release.	
19-May-2017 2		Updated Figure 16: "µQFN1.9x1 10L package outline" and Figure 19: "µQFN1.9x1 10L tape and reel specification".	

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