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FQI4N90

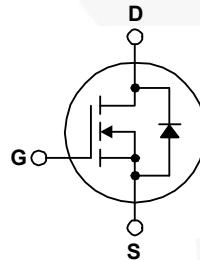
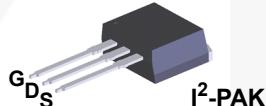
N-Channel QFET® MOSFET 900 V, 4.2 A, 3.3 Ω

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 4.2 A, 900 V, $R_{DS(on)}$ = 3.3 Ω (Max.) @ $V_{GS} = 10$ V, $I_D = 2.1$ A
- Low Gate Charge (Typ. 24 nC)
- Low C_{rss} (Typ. 9.5 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQI4N90TU	Unit
V_{DSS}	Drain-Source Voltage	900	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	4.2	A
	- Continuous ($T_C = 100^\circ\text{C}$)	2.65	A
I_{DM}	Drain Current - Pulsed	(Note 1)	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
I_{AR}	Avalanche Current	(Note 1)	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	3.13	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	140	W
	- Derate above 25°C	1.12	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering, 1/8" from case for 5 seconds.	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQI4N90TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.89	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in ² Pad of 2-oz Copper), Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQI4N90TU	FQI4N90	I ² -PAK	Tube	N/A	N/A	50 units

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	900	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	--	0.9	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 900 \text{ V}$, $V_{GS} = 0 \text{ V}$	--	--	10	μA
		$V_{DS} = 720 \text{ V}$, $T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30 \text{ V}$, $V_{DS} = 0 \text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}$, $V_{DS} = 0 \text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	3.0	--	5.0	V
$R_{DS(\text{on})}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 2.1 \text{ A}$	--	2.7	3.3	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50 \text{ V}$, $I_D = 2.1 \text{ A}$	--	3.5	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$	--	860	1100	pF
C_{oss}	Output Capacitance		--	90	120	pF
C_{rss}	Reverse Transfer Capacitance		--	9.5	12.5	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 450 \text{ V}$, $I_D = 4.2 \text{ A}$, $R_G = 25 \Omega$	--	25	60	ns
t_r	Turn-On Rise Time		--	70	150	ns
$t_{d(off)}$	Turn-Off Delay Time		--	45	100	ns
t_f	Turn-Off Fall Time		--	40	90	ns
Q_g	Total Gate Charge	$V_{DS} = 720 \text{ V}$, $I_D = 4.2 \text{ A}$, $V_{GS} = 10 \text{ V}$	--	24	30	nC
Q_{gs}	Gate-Source Charge		--	5.8	--	nC
Q_{gd}	Gate-Drain Charge		--	11.5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	4.2	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	16.8	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_S = 4.2 \text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$, $I_S = 4.2 \text{ A}$, $dI_F / dt = 100 \text{ A}/\mu\text{s}$	--	440	--	ns
Q_{rr}	Reverse Recovery Charge	--	3.3	--	μC	

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. $L = 61 \text{ mH}$, $I_{AS} = 4.2 \text{ A}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 4.2 \text{ A}$, $dI/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Characteristics

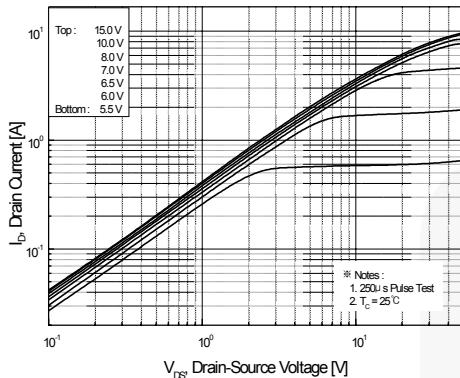


Figure 1. On-Region Characteristics

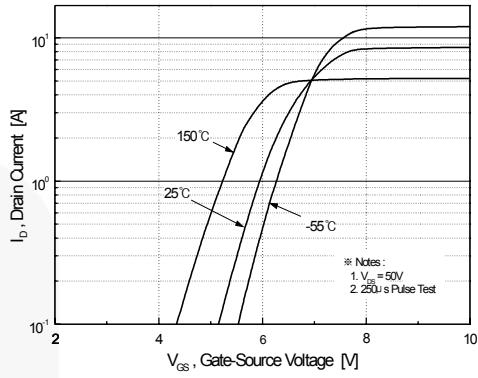


Figure 2. Transfer Characteristics

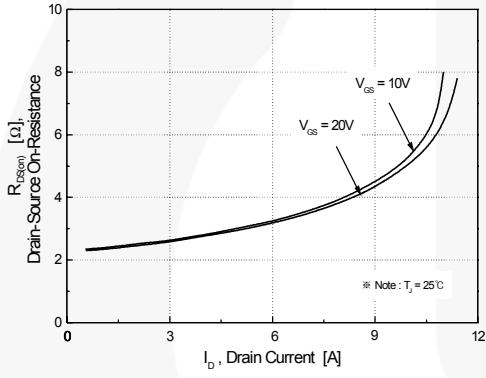


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

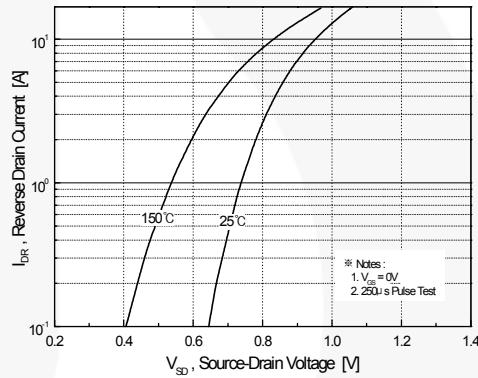


Figure 4. Body Diode Forward Voltage
Variation vs. Source Current and
Temperature

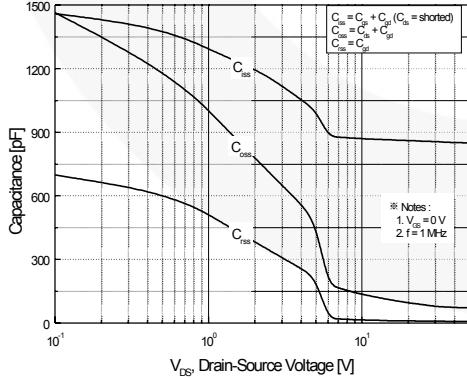


Figure 5. Capacitance Characteristics

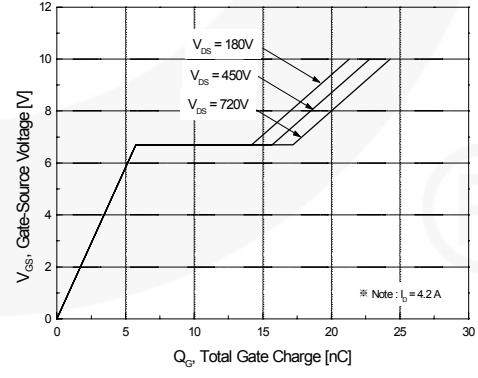


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

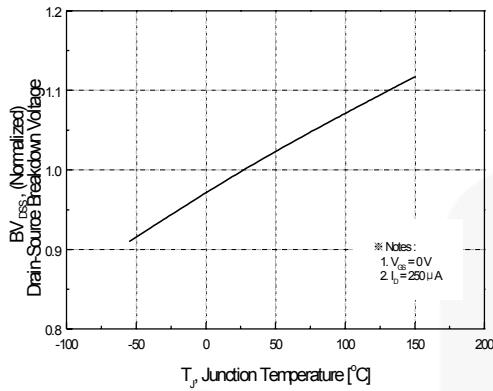


Figure 7. Breakdown Voltage Variation vs. Temperature

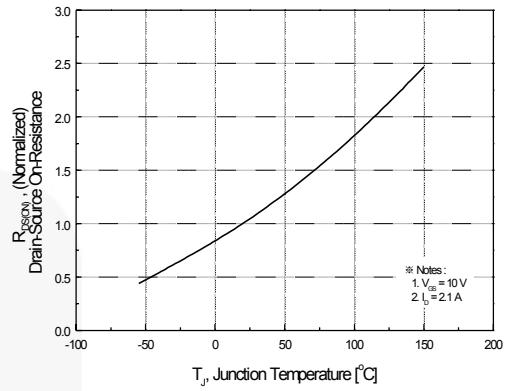


Figure 8. On-Resistance Variation vs. Temperature

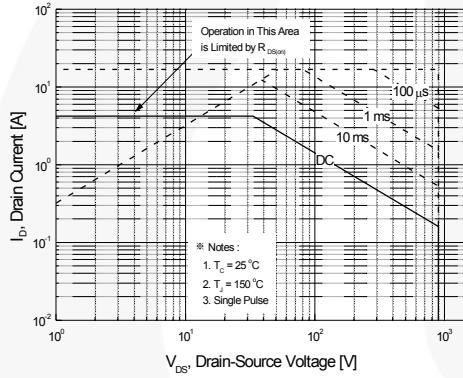


Figure 9. Maximum Safe Operating Area

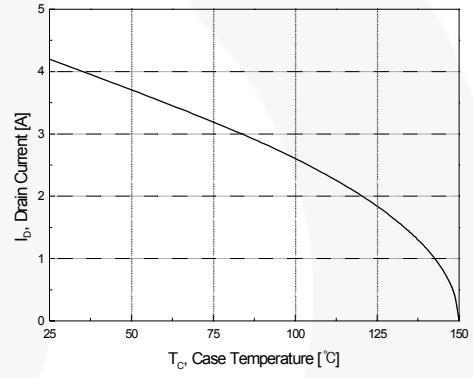


Figure 10. Maximum Drain Current vs. Case Temperature

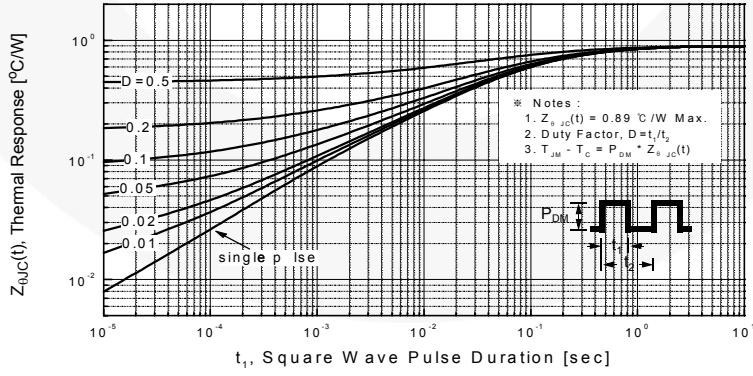


Figure 11. Transient Thermal Response Curve

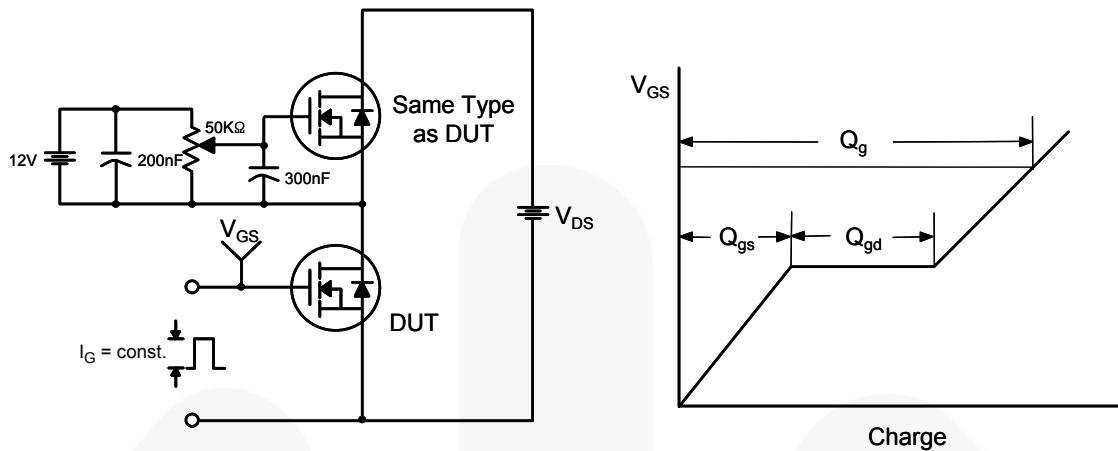


Figure 12. Gate Charge Test Circuit & Waveform

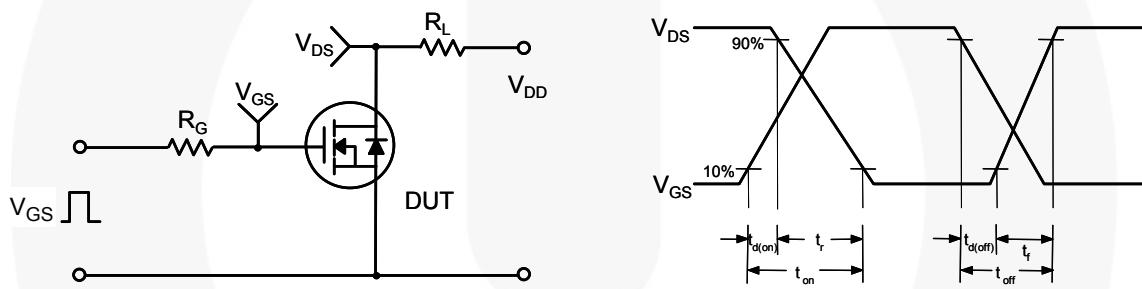


Figure 13. Resistive Switching Test Circuit & Waveforms

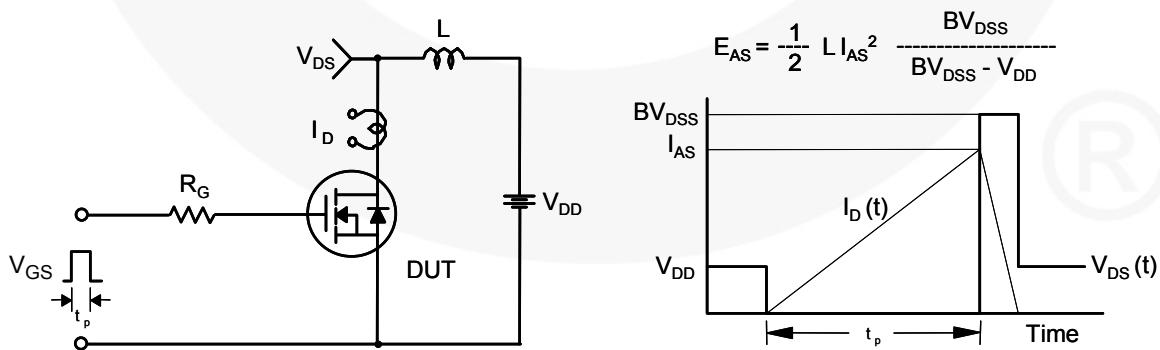


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

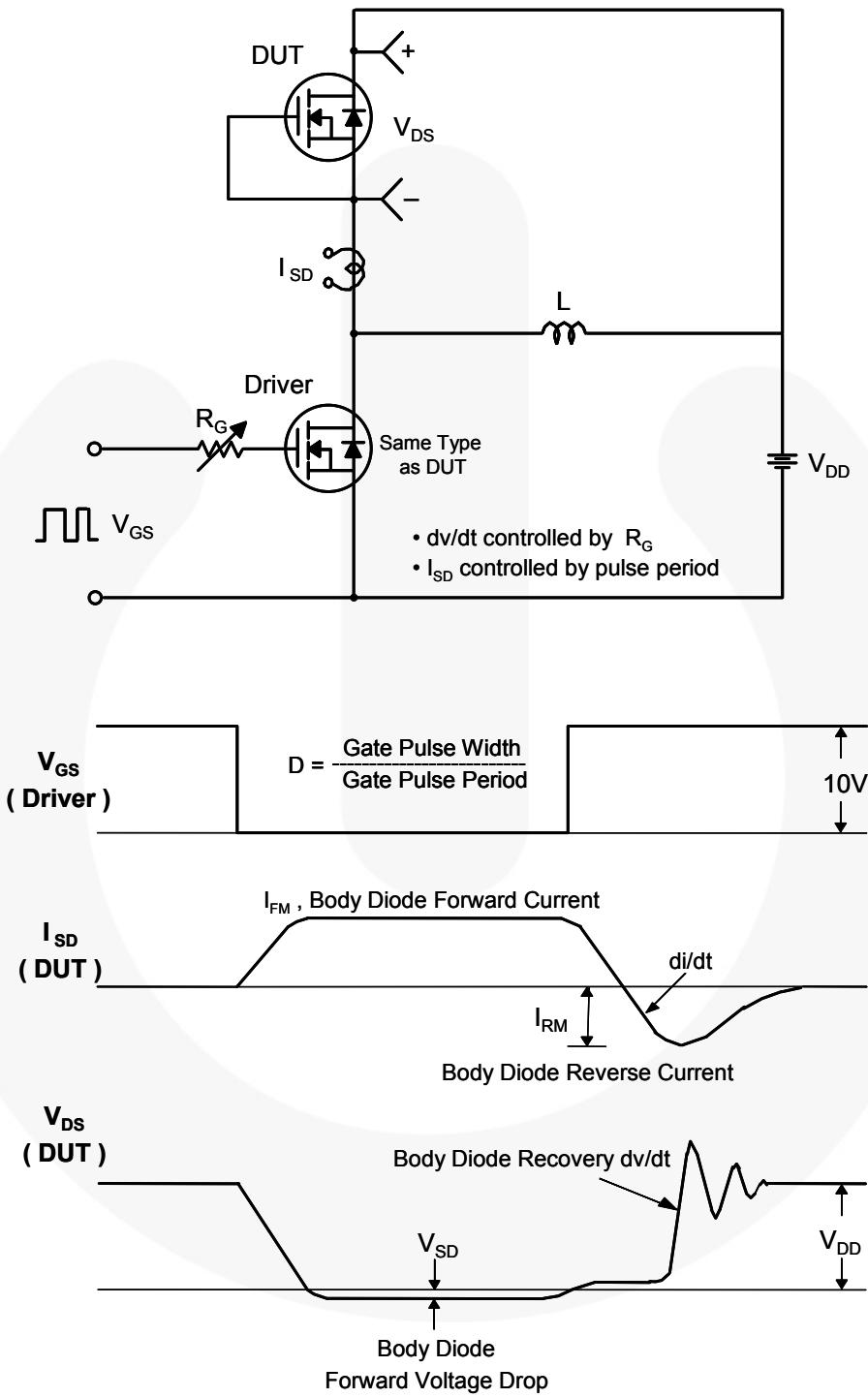
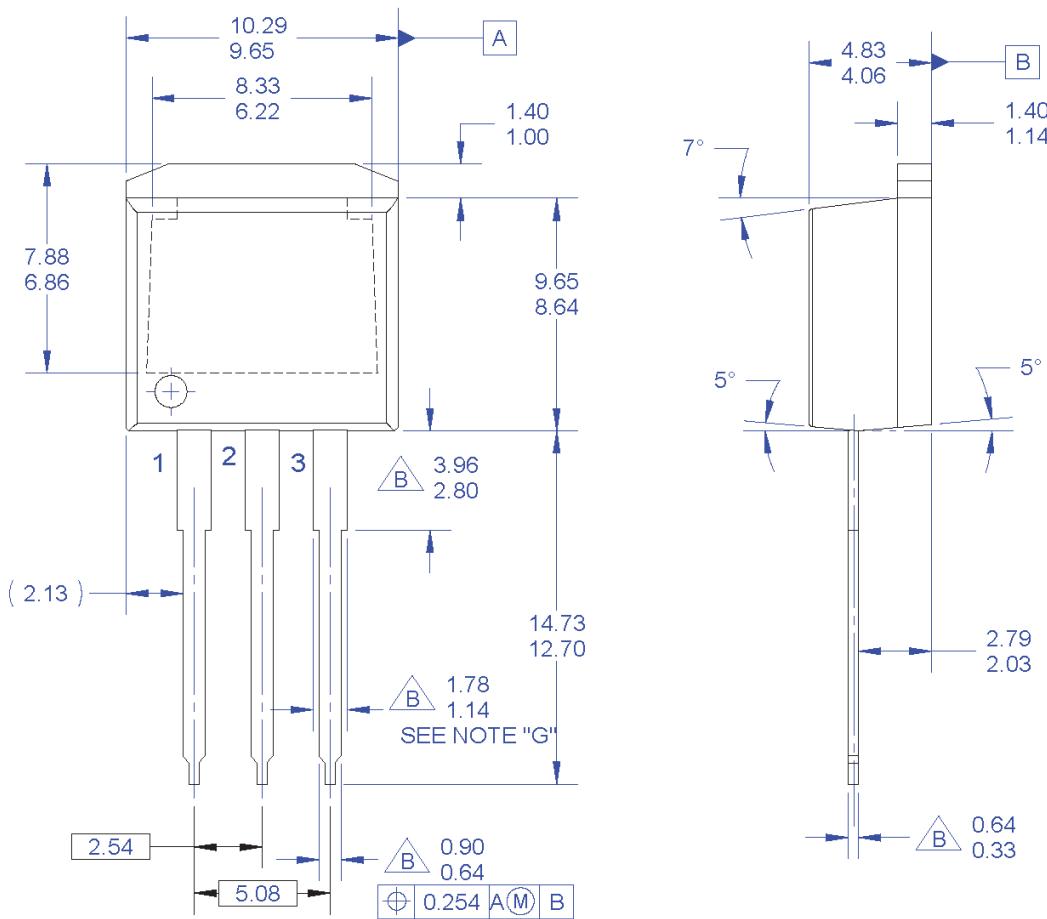


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- B.** DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

Figure 16. TO262 (I²PAK), Molded, 3-Lead, Jedec Variation AA

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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