CS4343
16 Port 10G CDR with Octal EDC

Product Description

The CS4343 EDC PHY is a serial 15 Gbps Octal PHY with 16 Port CDR Electronic Dispersion Compensation (EDC). The device's 28 nm architecture enables higher port counts and increased faceplate and backplane bandwidth for next generation data center, carrier, and enterprise systems. The CS4343 EDC PHY leads the industry with less than 1 ns latency in a 17 mm × 17 mm package, while lowering power consumption by 50% over previous generations. The CS4343 EDC PHY provides a wide operating frequency range covering 1 GbE, 10 GbE, 1G FC, 2G FC, 4G FC, 8G FC, 16G FC, Infiniband SDR, DDR, QDR, FDR, CPRI Options 1 to 7, and support for all the major standards used in data centers, storage, high performance computing, and wireless backhaul applications including 1 GbE, 10 GbE, 40 GbE, 100 GbE, InfiniBand, Fibre Channel, CPRI, and OBSAI.

The CS4343 EDC PHY functionality supports eight full-duplex 10G links, or two full-duplex 40G links. EDC capability allows the device to operate with linear SFP+/QSFP optical modules, Direct Attach Copper, 40GBase-CR4 cables, and 10GBase-ZR and DWDM SMF applications. The device is fully compliant to 10G SFP+, 802.3ba 40G and 100G nPPI, and nAUI specifications. The fully autonomous device does not require external processors to control the convergence or dynamic adaption of the dispersion compensation. The CS4343 EDC PHY also integrates the auto negotiation and coefficient training functionality for 40G KR4/CR4 applications, and rate negotiation 16G Fibre channel, for seamless interoperability with existing equipment.

The CS4343 EDC PHY includes an integrated 2 × 2 switch enabling redundant backplane and faceplate applications without needing an external crossbar device. The integrated switch functionality supports 1+1 protection switching and broadcast functionality in both directions. The device supports link quality monitoring for the inactive redundant link to enable fast switching. In addition, the CS4343 EDC PHY has a fully symmetric architecture with EDC capability on both ingress and egress directions. This enables applications such as translation from KR4 backplane to CR4 cable in blade server designs using a single device, reducing system cost.

The CS4343 EDC PHY has integrated AC coupling capacitors on all receiver inputs to reduce overall system BOM cost. The device also includes capabilities such as real time eye monitoring, loopbacks, PRBS generators and checkers, hardware interrupt, and GPIO pins for test and debug purposes.

Market(s)

Inside Data Centers

Product Type

PHY / SerDes

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