

N-Channel Power MOSFET

30V, 61A, 8.8mΩ

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

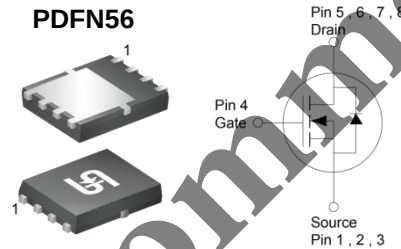
KEY PERFORMANCE PARAMETERS

PARAMETER		VALUE	UNIT
V_{DS}		30	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	8.8	mΩ
	$V_{GS} = 4.5V$	11.4	
Q_g		6.3	nC

APPLICATIONS

- DC-DC Converters
- Battery Power Management
- ORing FET/Load Switching


 RoHS
COMPLIANT

 HALOGEN
FREE


Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	61	A
	$T_A = 25^\circ\text{C}$		13	
Pulsed Drain Current		I_{DM}	244	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	18	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	48.6	mJ
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	56	W
	$T_C = 125^\circ\text{C}$		11	
Total Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2.6	W
	$T_A = 125^\circ\text{C}$		0.5	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.2	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	48	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	30	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	$V_{GS(TH)}$	1.2	1.9	2.5	V
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 30V$	I_{DSS}	--	--	1	μA
	$V_{GS} = 0V, V_{DS} = 30V$ $T_J = 125^{\circ}C$		--	--	100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10V, I_D = 13A$	$R_{DS(on)}$	--	6.5	8.8	m Ω
	$V_{GS} = 4.5V, I_D = 13A$		--	9.5	11.4	
Forward Transconductance (Note 3)	$V_{DS} = 5V, I_D = 13A$	g_{fs}	--	45	--	S
Dynamic (Note 4)						
Total Gate Charge	$V_{GS} = 10V, V_{DS} = 15V,$ $I_D = 13A$	Q_g	--	12.6	--	nC
Total Gate Charge	$V_{GS} = 4.5V, V_{DS} = 15V,$ $I_D = 13A$	Q_g	--	6.3	--	
Gate-Source Charge		Q_{gs}	--	2.4	--	
Gate-Drain Charge		Q_{gd}	--	2.3	--	
Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V$ $f = 1.0MHz$	C_{iss}	--	750	--	pF
Output Capacitance		C_{oss}	--	190	--	
Reverse Transfer Capacitance		C_{rss}	--	78	--	
Gate Resistance	$f = 1.0MHz$	R_g	0.5	1.5	3	Ω
Switching (Note 4)						
Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 15V,$ $I_D = 7.5A, R_G = 10\Omega,$ $R_L = 2\Omega$	$t_{d(on)}$	--	9.6	--	ns
Turn-On Rise Time		t_r	--	4.5	--	
Turn-Off Delay Time		$t_{d(off)}$	--	25.5	--	
Turn-Off Fall Time		t_f	--	3.4	--	
Source-Drain Diode						
Forward Voltage (Note 3)	$V_{GS} = 0V, I_S = 13A$	V_{SD}	--	--	1.2	V
Reverse Recovery Time	$I_S = 13A,$ $di/dt = 100A/\mu s$	t_{rr}	--	18	--	ns
Reverse Recovery Charge		Q_{rr}	--	11.4	--	nC

Notes:

1. Silicon limited current only.
2. $L = 0.3\text{mH}$, $V_{GS} = 10V$, $V_{DD} = 25V$, $R_G = 25\Omega$, $I_{AS} = 18A$, Starting $T_J = 25^\circ\text{C}$
3. Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
4. Switching time is essentially independent of operating temperature.

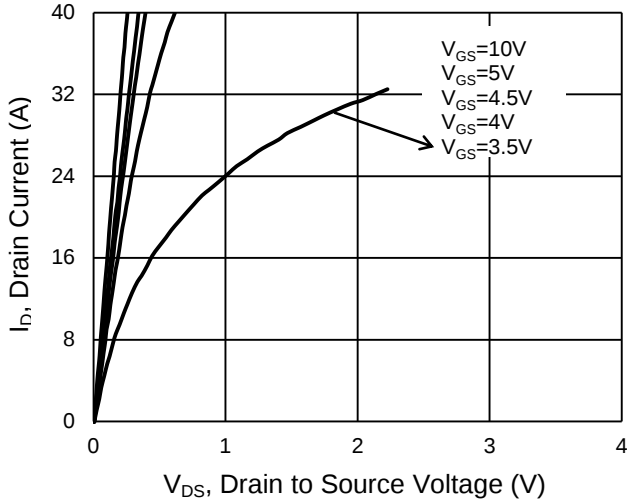
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM088NA03CR RLG	PDFN56	2,500pcs / 13" Reel

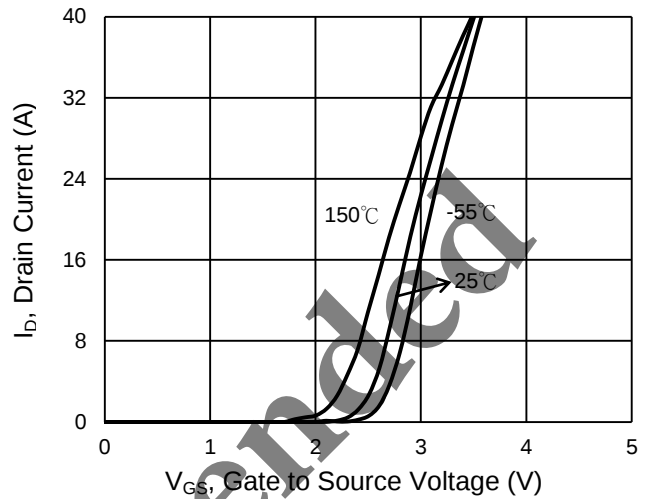
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

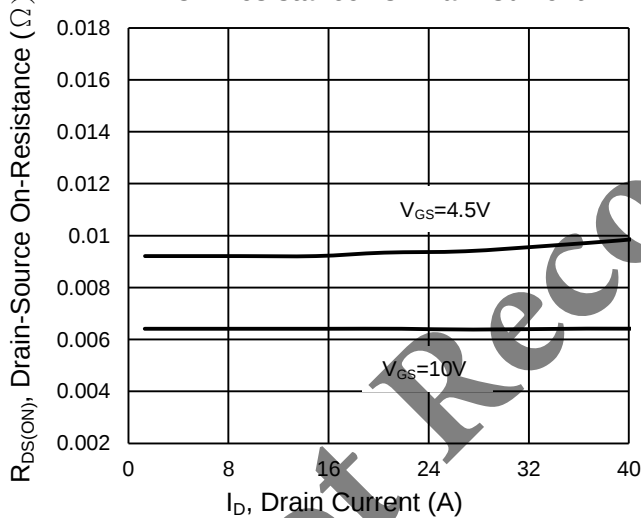
Output Characteristics



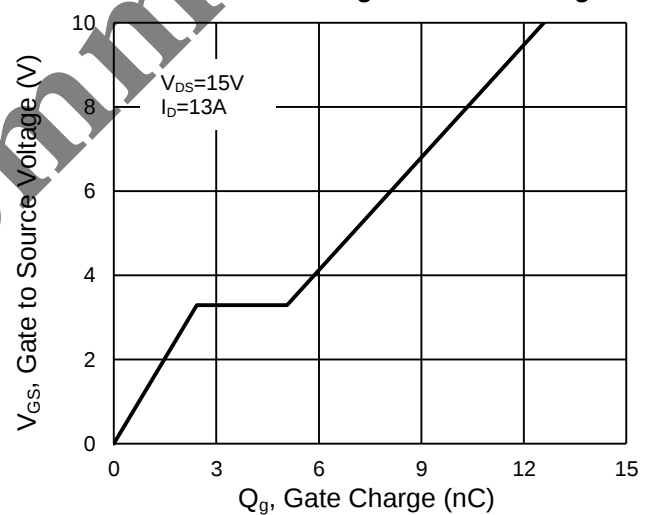
Transfer Characteristics



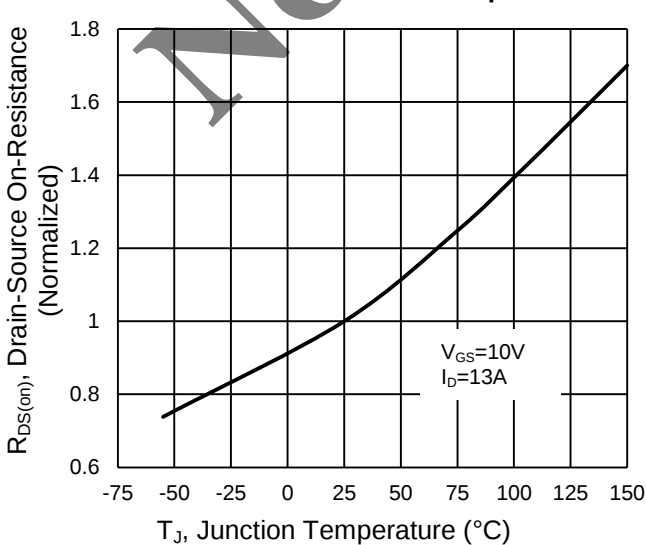
On-Resistance vs. Drain Current



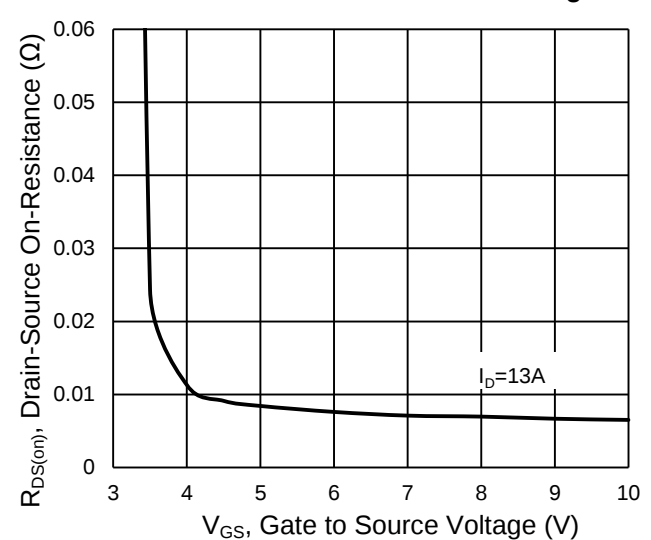
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



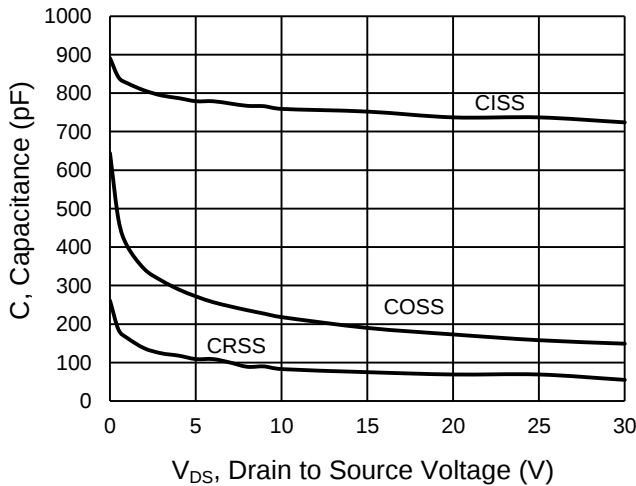
On-Resistance vs. Gate-Source Voltage



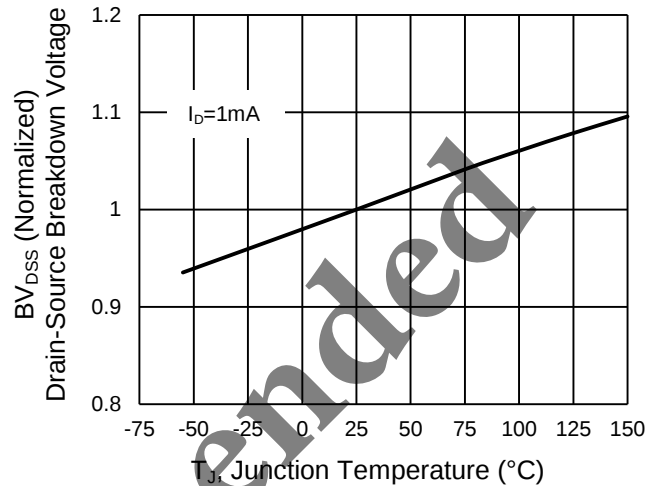
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($T_A = 25^\circ\text{C}$ unless otherwise noted)

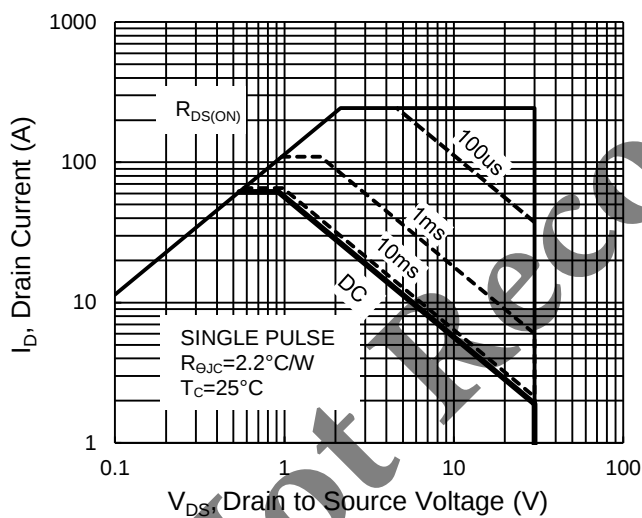
Capacitance vs. Drain-Source Voltage



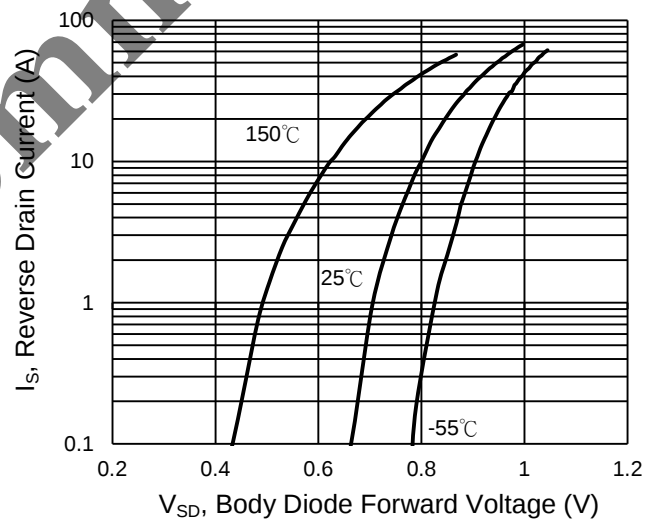
BV_{DSS} vs. Junction Temperature



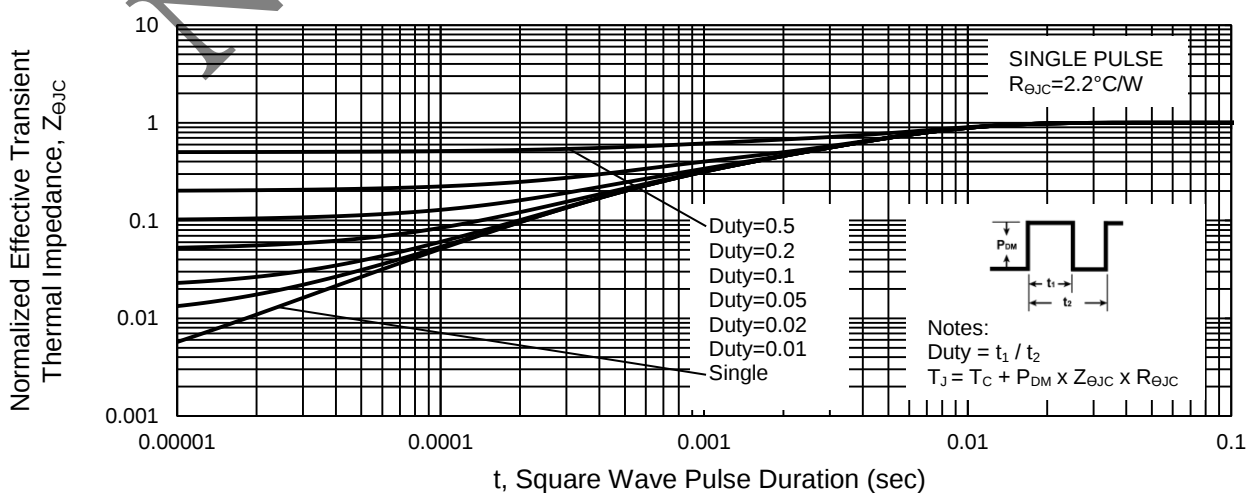
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

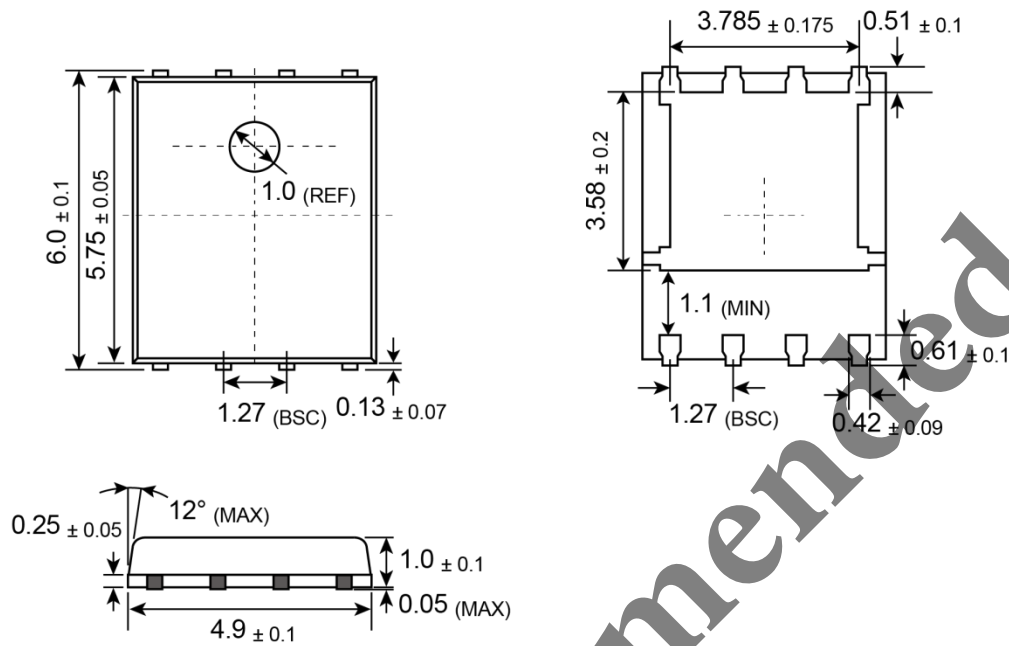


Normalized Thermal Transient Impedance, Junction-to-Case

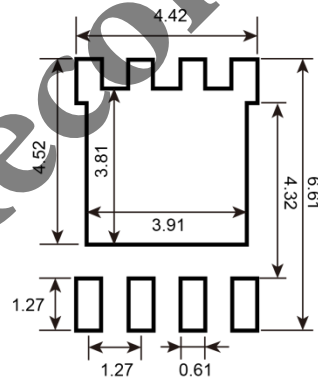


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

Not Recommended

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