

IRFY9140C, IRFY9140CM

PD-91294F

**Power MOSFET
Thru-Hole (TO-257AA)
-100V, P-channel, HEXFET™ MOSFET Technology**

Features

- Simple drive requirements
- Hermetically sealed
- Electrically Isolated
- Ceramic eyelets
- Ideal suited for space level applications
- ESD Rating: Class 2 per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Adhered to JANTX screening flow according to MIL-PRF-19500 for high-reliability applications

Description

HEXFET MOSFET technology is the key to IR HiRel advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.

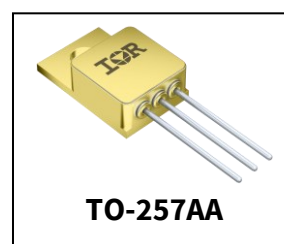
Ordering Information

Table 1 **Ordering options**

Part number	Package	Screening Level
IRFY9140C	TO-257AA	COTS
IRFY9140CM	TO-257AA	COTS
IRFY9140CSCX	TO-257AA	JANTX-equivalent

Product Summary

- **BV_{DSS}** : -100V
- **I_D** : -15.8A
- **$R_{DS(on),max}$** : 0.20Ω
- **Q_G, max** : 60nC



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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = -10V, T_C = 25^{\circ}C$	Continuous Drain Current	-15.8	A
$I_{D2} @ V_{GS} = -10V, T_C = 100^{\circ}C$	Continuous Drain Current	-10	A
$I_{DM} @ T_C = 25^{\circ}C$	Pulsed Drain Current ¹	-60	A
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	100	W
	Linear Derating Factor	0.8	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ²	640	mJ
I_{AR}	Avalanche Current ¹	-15.8	A
E_{AR}	Repetitive Avalanche Energy ¹	10	mJ
dv/dt	Peak Diode Reverse Recovery ³	-5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (0.063in./1.6mm from case for 10s)	
	Weight	4.3 (Typical)	g

¹ Repetitive Rating: Pulse width limited by maximum junction temperature.

² $V_{DD} = -50V$, starting $T_J = 25^{\circ}C$, $L = 5.1mH$, Peak $I_L = -15.8A$, $V_{GS} = -10V$

³ $I_{SD} \leq -15.8A$, $di/dt \leq -200A/\mu s$, $V_{DD} \leq -100V$, $T_J \leq 150^{\circ}C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics

Table 3 Static and Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V, I_D = -1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.1	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.20	Ω	$V_{GS} = -10V, I_{D2} = -10A^1$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
G_{fs}	Forward Transconductance	6.2	—	—	S	$V_{DS} = -15V, I_{D2} = -10A^1$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	$V_{DS} = -80V, V_{GS} = 0V$
		—	—	-250		$V_{DS} = -80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Leakage Reverse	—	—	100		$V_{GS} = 20V$
Q_G	Total Gate Charge	—	—	60	nC	$I_{D1} = -15.8A$
Q_{GS}	Gate-to-Source Charge	—	—	13		$V_{DS} = -50V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	35.2		$V_{GS} = -10V$
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	$I_{D1} = -15.8A^{**}$ $V_{DD} = -50V$ $R_G = 7.5\Omega$ $V_{GS} = -10V$
t_r	Rise Time	—	—	85		
$t_{d(off)}$	Turn-Off Delay Time	—	—	85		
t_f	Fall Time	—	—	65		
$L_s + L_D$	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. From package) with Source wires internally bonded from Source Pin to Drain Pad
C_{iss}	Input Capacitance	—	1400	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	600	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	200	—		$f = 1.0MHz$

****** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-15.8	A	
I _{SM}	Pulsed Source Current (Body Diode) ¹	—	—	-60	A	
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _J = 25°C, I _S = -15.8A, V _{GS} = 0V ²
t _{rr}	Reverse Recovery Time	—	—	280	ns	T _J = 25°C, I _F = -15.8A, V _{DD} ≤ -50V di/dt = -100A/μs ²
Q _{rr}	Reverse Recovery Charge	—	2.4	—	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	1.25	$^\circ\text{C}/\text{W}$
$R_{\theta JCS}$	Case-to-Sink	—	0.21	—	
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	80	

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300\ \mu\text{s}$; Duty Cycle $\leq 2\%$

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Electrical Characteristics Curves

3 Electrical Characteristics Curves

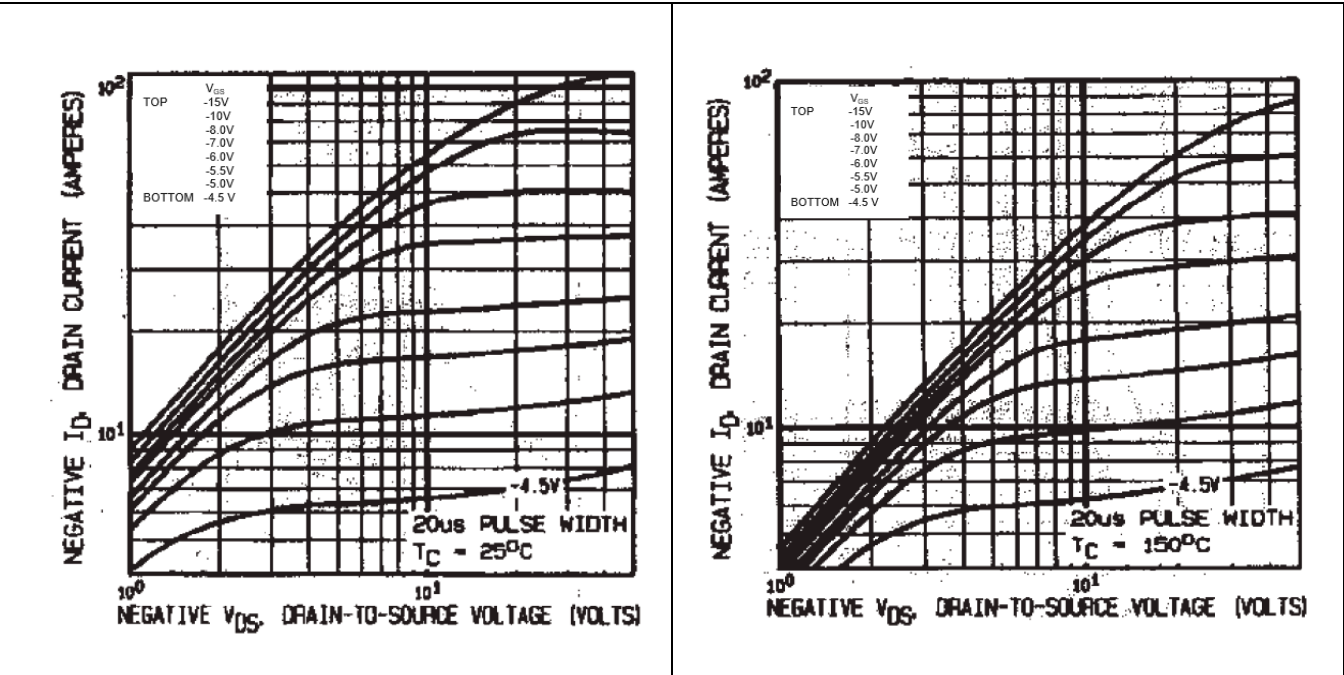


Figure 1 Typical Output Characteristics

Figure 2 Typical Output Characteristics

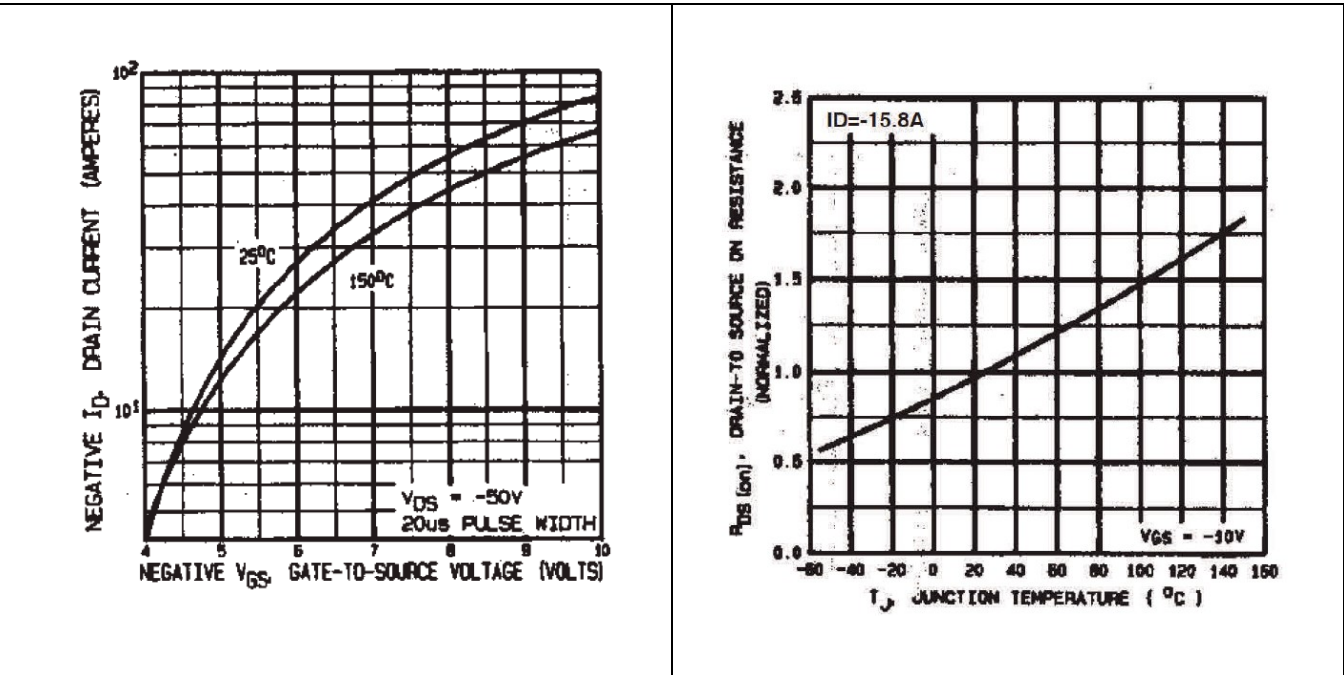


Figure 3 Typical Transfer Characteristics

Figure 4 Normalized On-Resistance Vs. Temperature

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Power MOSFET THRU-HOLE (TO-257AA)

Electrical Characteristics Curves

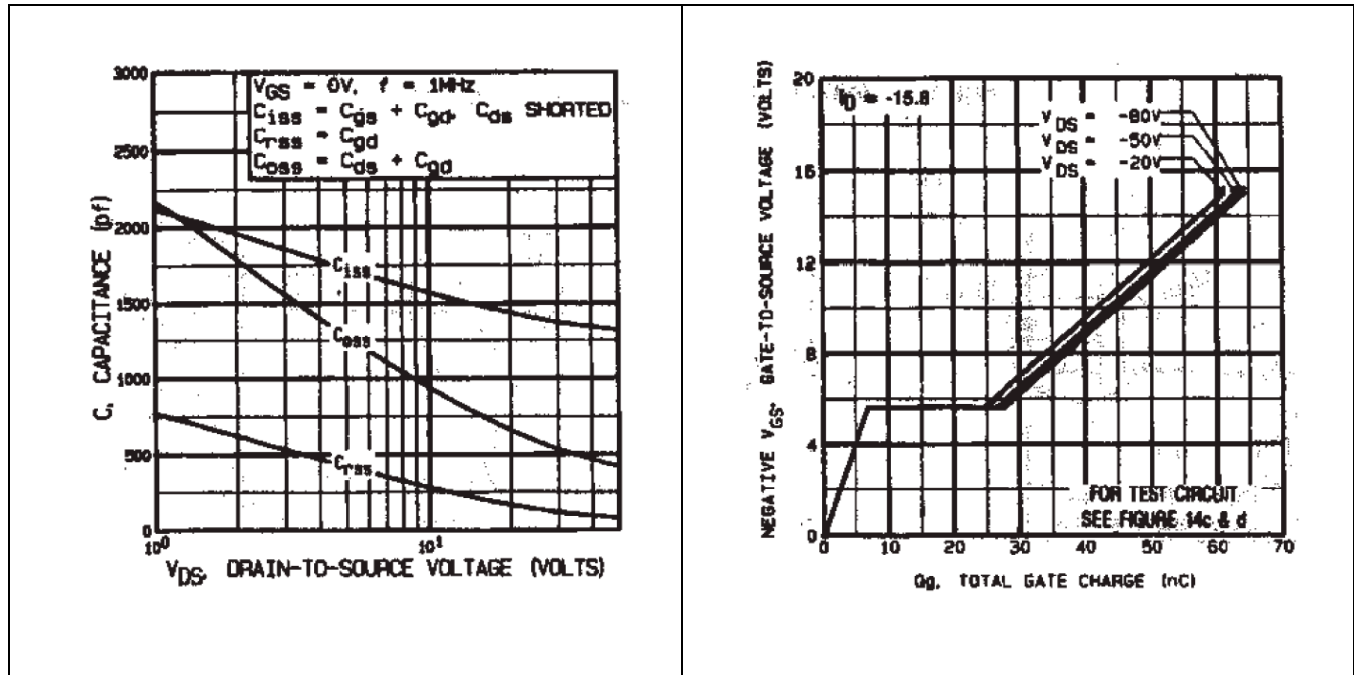


Figure 5 Typical Capacitance Vs. Drain-to-Source Voltage

Figure 6 Typical Gate Charge Vs. Gate-to-Source Voltage

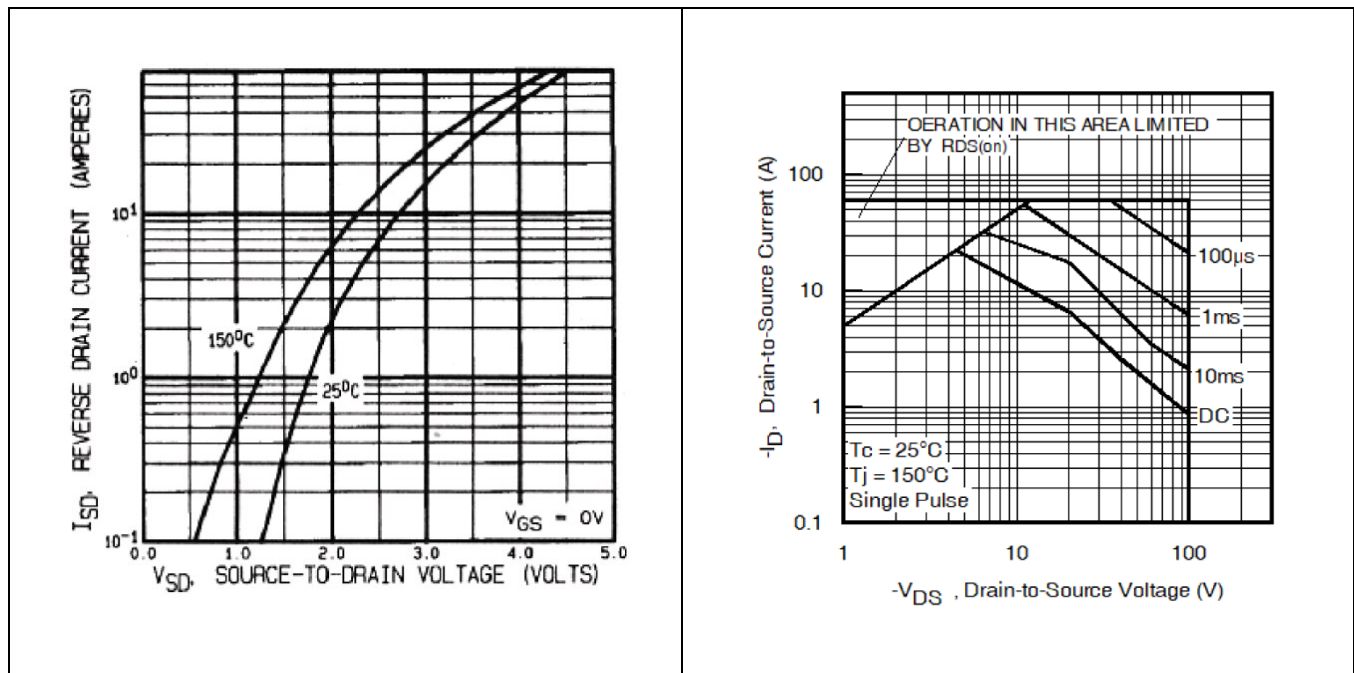


Figure 7 Typical Source-Drain Vs. Diode Forward Voltage

Figure 8 Maximum Safe Operating Area

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Electrical Characteristics Curves

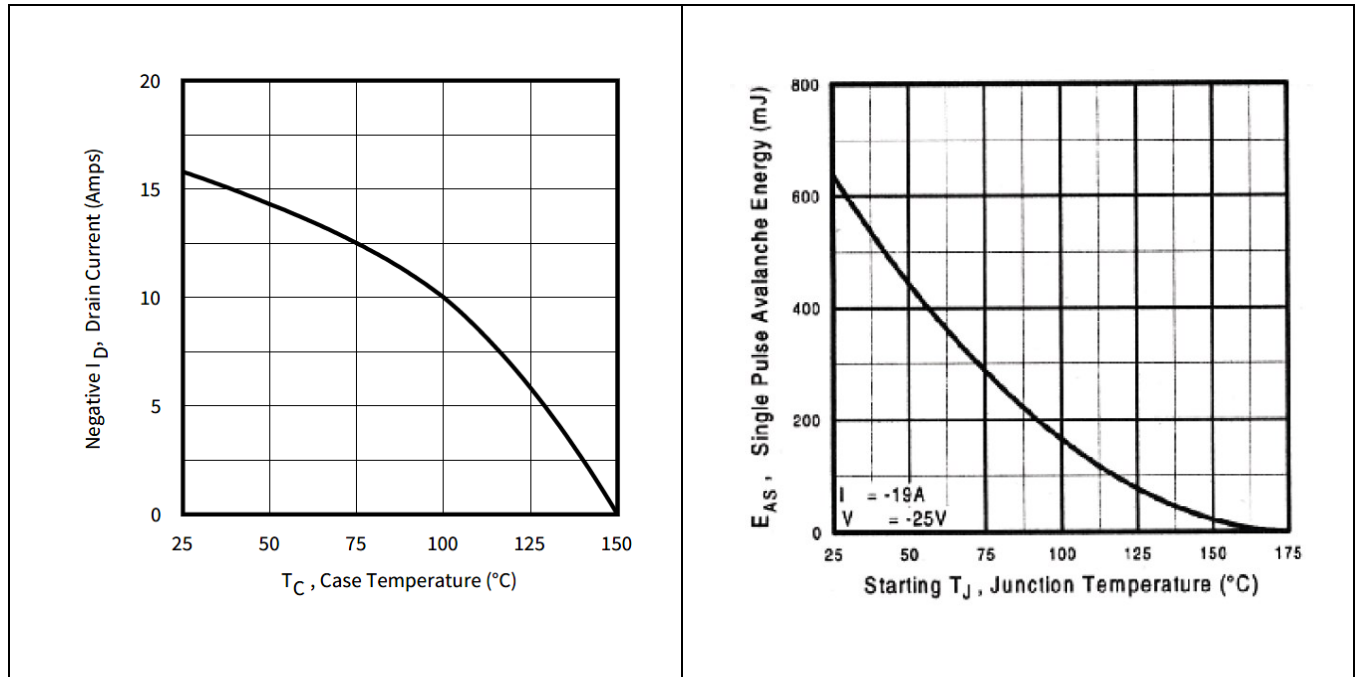


Figure 9 Maximum Drain Current Vs. Case Temperature

Figure 10 Maximum Avalanche Energy Vs. Drain Current

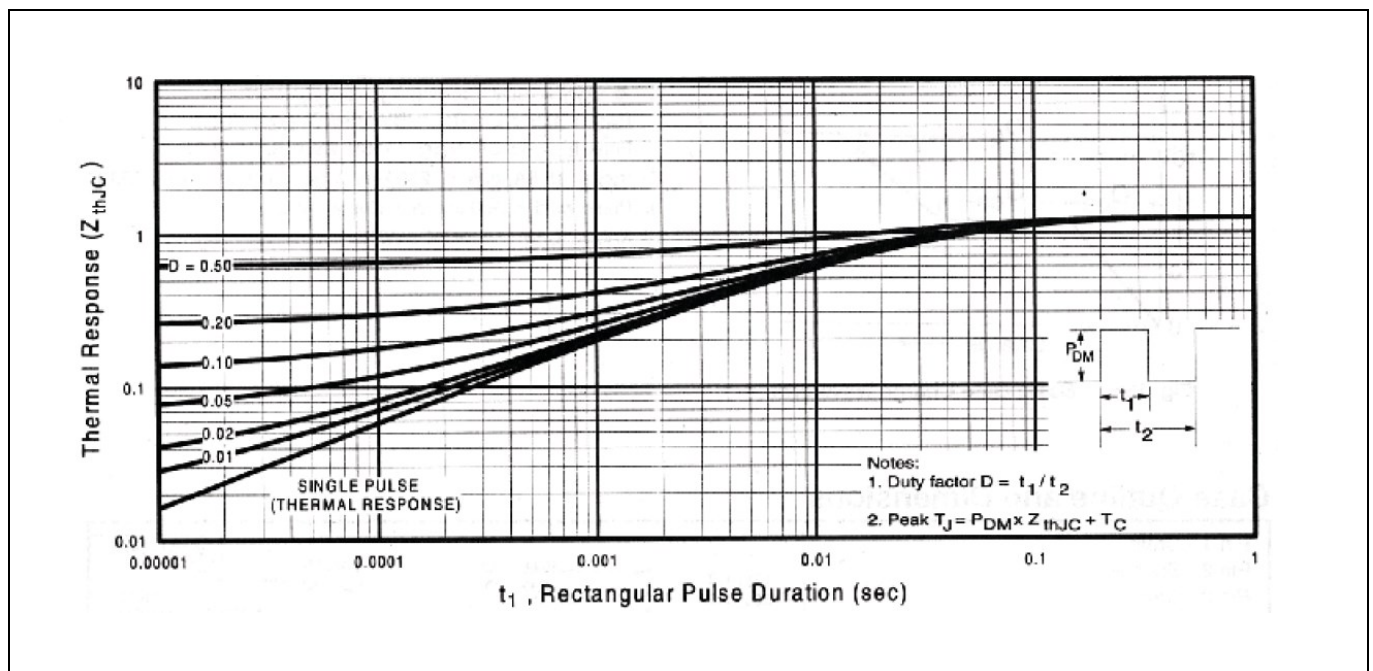


Figure 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Test Circuits (Pre-irradiation)

4 Test Circuits (Pre-irradiation)

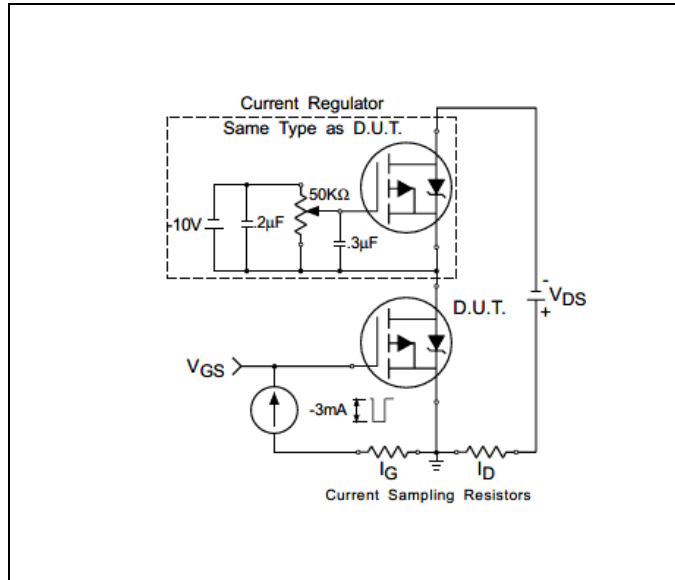


Figure 12 Gate Charge Test Circuit

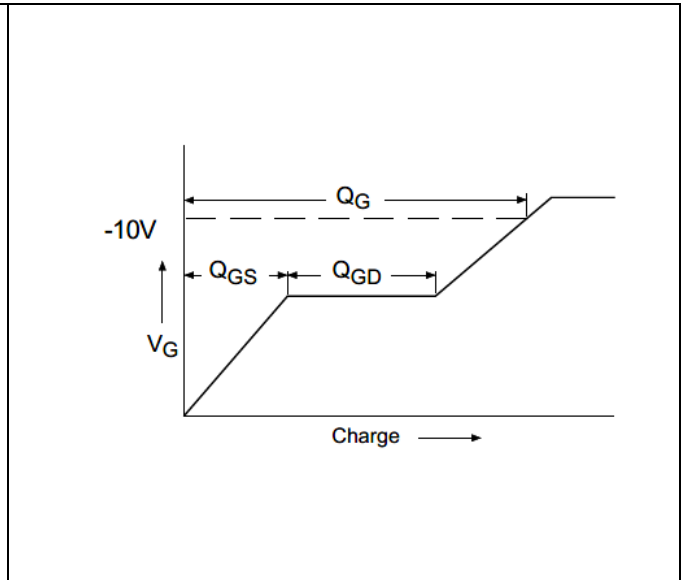


Figure 13 Gate Charge Waveform

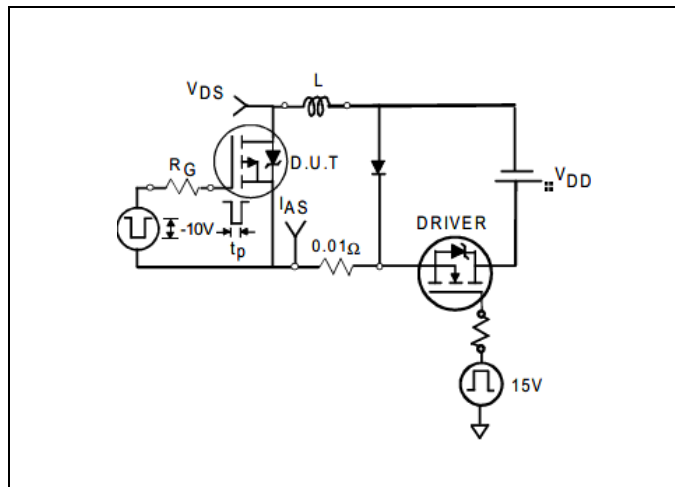


Figure 14 Unclamped Inductive Test Circuit

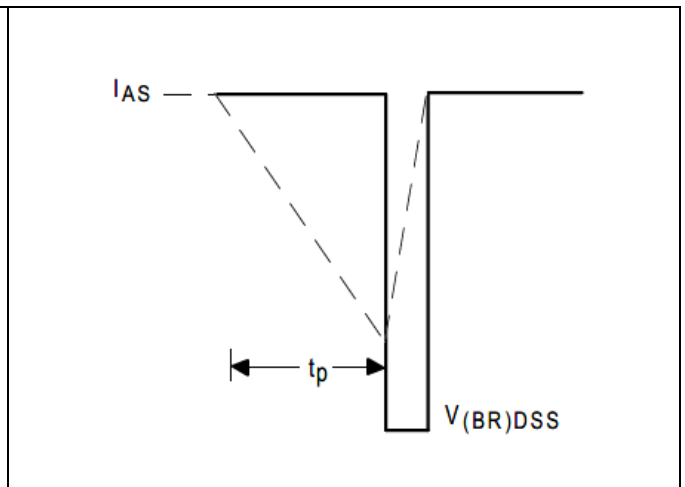


Figure 15 Unclamped Inductive Waveform

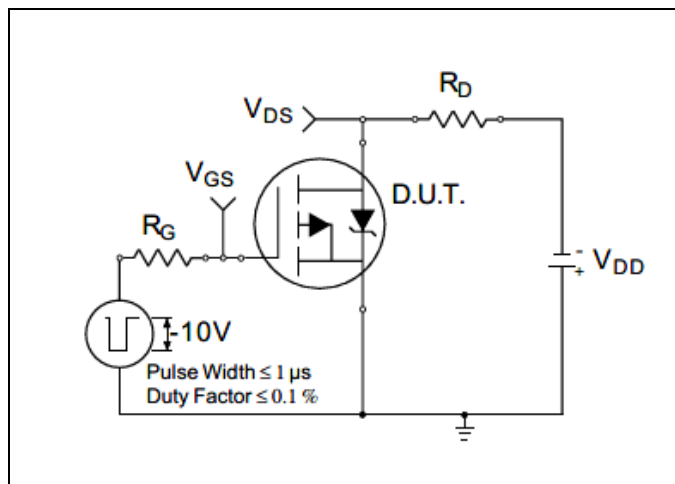


Figure 16 Switching Time Test Circuit

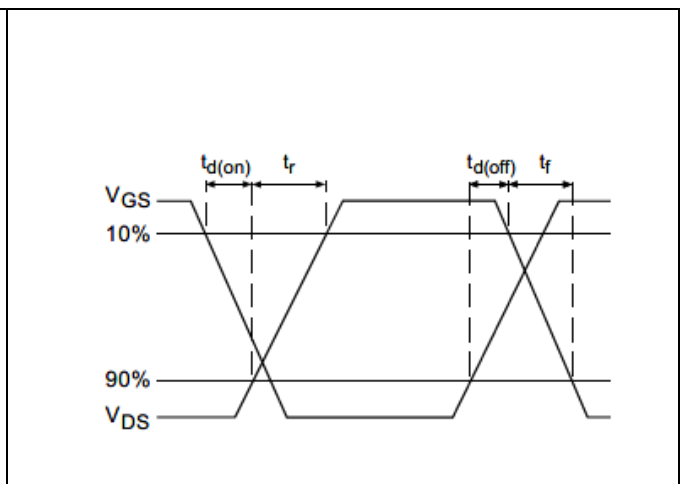
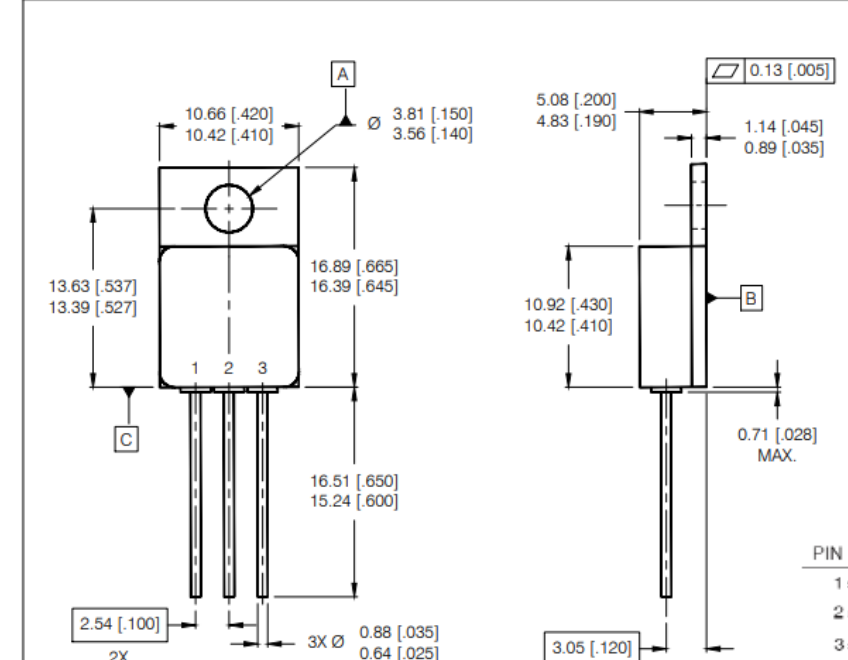


Figure 17 Switching Time Waveforms

5 Package Outline

REV.	DESCRIPTION	ECN	DATE
B	INITIAL RELEASE	1120_ER6904	4-2-20



FRONT VIEW DIMENSIONS:

- Top width: 10.66 [.420] / 10.42 [.410]
- Top hole diameter: \varnothing 3.81 [.150] / 3.56 [.140]
- Left height: 13.63 [.537] / 13.39 [.527]
- Right height: 16.89 [.665] / 16.39 [.645]
- Pin pitch: 2.54 [.100] (2X)
- Pin diameter: 3X \varnothing 0.88 [.035] / 0.64 [.025]
- Bottom height: 16.51 [.650] / 15.24 [.600]

SIDE VIEW DIMENSIONS:

- Top width: 0.13 [.005]
- Top height: 5.08 [.200] / 4.83 [.190]
- Top hole diameter: 1.14 [.045] / 0.89 [.035]
- Pin height: 10.92 [.430] / 10.42 [.410]
- Pin diameter: 0.71 [.028] MAX.
- Bottom height: 3.05 [.120]

CERAMIC EYELETS:

IRFY...CM
IRHY...CM

1 2 3
D S G

PIN ASSIGNMENTS


- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

NOTES:

- DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
- CONTROLLING DIMENSION: INCH.
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.
- STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

SYMBOLS:

\varnothing 0.50 [.020] (M) C A (M) B



An Infineon Technologies Company

TITLE: TO-257AA PACKAGE
OUTLINE (STD & LOW OHMIC)

DRAWING NO. D100723G-WEB

REV B

IRFY9140C, IRFY9140CM
Power MOSFET THRU-HOLE (TO-257AA)

Revision history

Revision history

Document version	Date of release	Description of changes
	09/22/2003	Final datasheet (PD-91294C)
Rev D	09/29/2003	Updated per Package outline
Rev E	09/21/2016	Updated per ECN-1120-04715
Rev F	12/06/2024	Updated per ECN-1120-10102

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