

# CDCV857

## 2.5-V PHASE LOCK LOOP CLOCK DRIVER

SCAS645A – AUGUST 2000 – REVISED OCTOBER 2000

- Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 60 to 200 MHz
- Low Jitter (cyc-cyc):  $\pm 75$  ps
- Distributes One Differential Clock Input to Ten Differential Outputs
- Three-State Outputs When the Input Differential Clocks Are  $< 20$  MHz
- Operates From Dual 2.5-V Supplies
- 48-Pin TSSOP Package
- Consumes  $< 200$ - $\mu$ A Quiescent Current
- External Feedback PIN (FBIN,  $\overline{\text{FBIN}}$ ) Are Used to Synchronize the Outputs to the Input Clocks

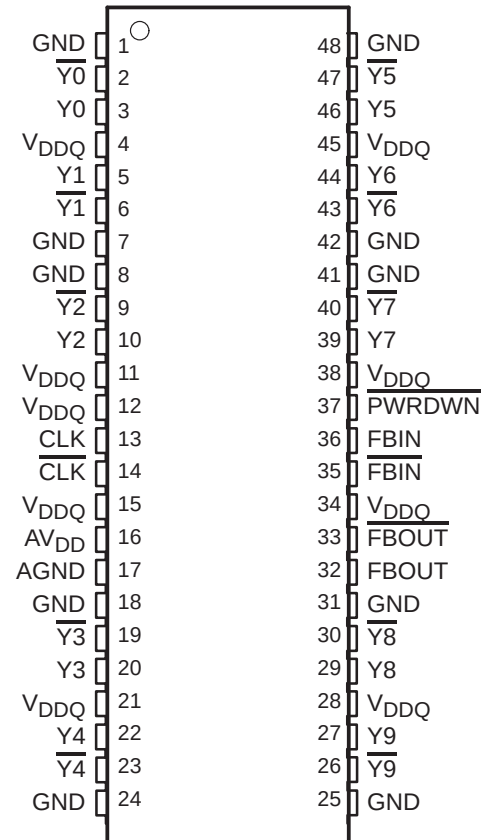
### description

The CDCV857 is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK,  $\overline{\text{CLK}}$ ) to ten differential pairs of clock outputs (Y[0:9],  $\overline{\text{Y}}[0:9]$ ) and one differential pair of feedback clock output (FBOU,  $\overline{\text{FBOU}}$ ). The clock outputs are controlled by the clock inputs (CLK,  $\overline{\text{CLK}}$ ), the feedback clocks (FBIN,  $\overline{\text{FBIN}}$ ), and the analog power input ( $\text{AV}_{\text{DD}}$ ). When  $\text{PWRDWN}$  is high, the outputs switch in phase and frequency with CLK. When  $\text{PWRDWN}$  is low, all outputs are disabled to high impedance state (3-state), and the PLL is shut down (low power mode). The device also enters this low power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit will detect the low frequency condition and after applying a  $> 20$  MHz input signal this detection circuit turns on the PLL again and enables the outputs.

When  $\text{AV}_{\text{DD}}$  is strapped low, the PLL is turned off and bypassed for test purposes. The CDCV857 is also able to track spread spectrum clocking for reduced EMI.

Since the CDCV857 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCV857 is characterized for operation from  $0^\circ\text{C}$  to  $85^\circ\text{C}$ .

DGG PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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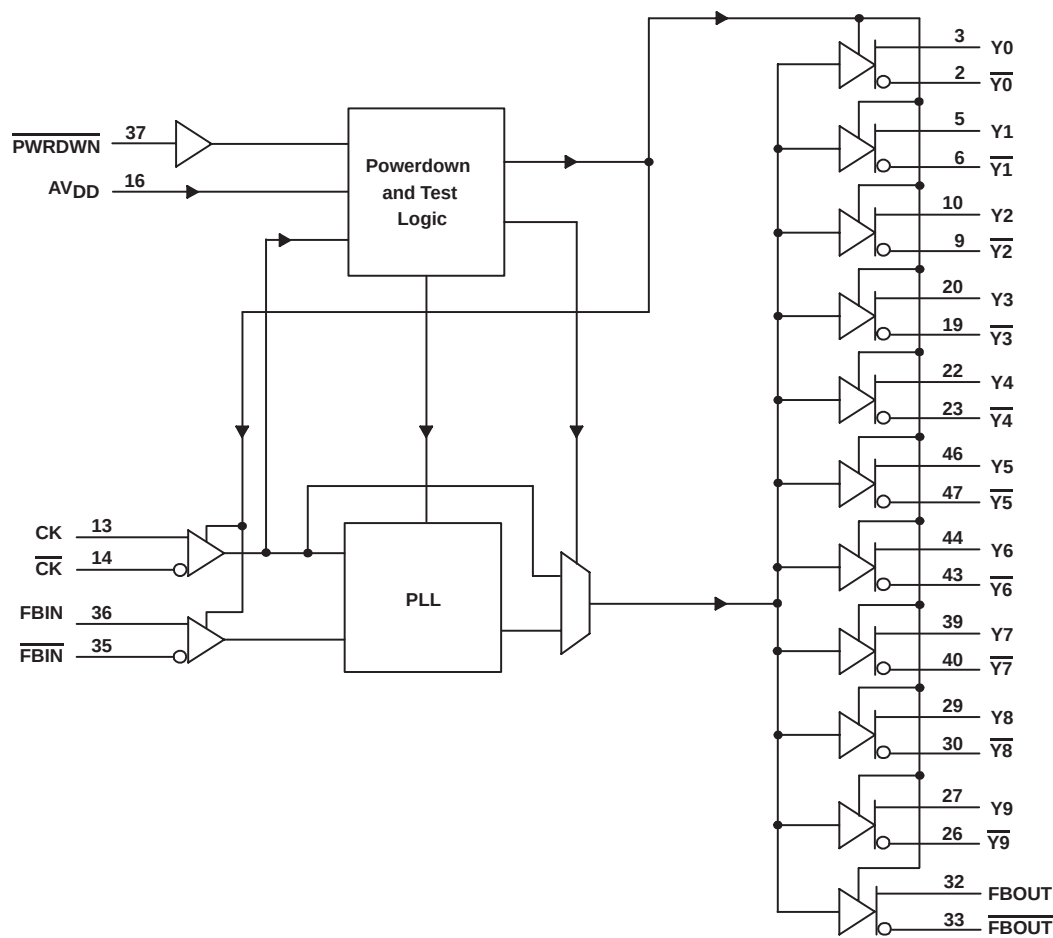
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FUNCTION TABLE  
(Select Functions)

| INPUTS           |        |         |         | OUTPUTS |        |                   |                   | PLL          |
|------------------|--------|---------|---------|---------|--------|-------------------|-------------------|--------------|
| AV <sub>DD</sub> | PWRDWN | CLK     | CLK     | Y[0:9]  | Y[0:9] | F <sub>BOUT</sub> | F <sub>BOUT</sub> |              |
| GND              | H      | L       | H       | L       | H      | L                 | H                 | Bypassed/Off |
| GND              | H      | H       | L       | H       | L      | H                 | L                 | Bypassed/Off |
| X                | L      | L       | H       | Z       | Z      | Z                 | Z                 | Off          |
| X                | L      | H       | L       | Z       | Z      | Z                 | Z                 | Off          |
| 2.5 V (nom)      | H      | L       | H       | L       | H      | L                 | H                 | On           |
| 2.5 V (nom)      | H      | H       | L       | H       | L      | H                 | L                 | On           |
| 2.5 V (nom)      | X      | <20 MHz | <20 MHz | Z       | Z      | Z                 | Z                 | Off          |

functional block diagram



### Terminal Functions

| TERMINAL<br>NAME     | NO.                                           | I/O | DESCRIPTION                                |
|----------------------|-----------------------------------------------|-----|--------------------------------------------|
| AGND                 | 17                                            |     | Ground for 2.5-V analog supply             |
| AV <sub>DD</sub>     | 16                                            |     | 2.5-V Analog supply                        |
| CLK, CLK             | 13, 14                                        | I   | Differential clock input                   |
| FBIN, FBIN           | 35, 36                                        | I   | Feedback differential clock input          |
| FBOU, FBOU           | 32, 33                                        | O   | Feedback differential clock output         |
| GND                  | 1, 7, 8, 18,<br>24, 25, 31,<br>41, 42, 48     |     | Ground                                     |
| PWRDWN               | 37                                            | I   | Output enable for Y and $\overline{Y}$     |
| V <sub>DDQ</sub>     | 4, 11, 12,<br>15, 21, 28,<br>34, 38, 45       |     | 2.5-V Supply                               |
| Y[0:9]               | 3, 5, 10,<br>20, 22, 27,<br>29, 39, 44,<br>46 | O   | Buffered output copies of input clock, CLK |
| $\overline{Y}$ [0:9] | 2, 6, 9, 19,<br>23, 26, 30,<br>40, 43, 47     | O   | Buffered output copies of input clock, CLK |

#### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

|                                                                                                  |                                  |
|--------------------------------------------------------------------------------------------------|----------------------------------|
| Supply voltage range, V <sub>DDQ</sub> , AV <sub>DD</sub>                                        | 0.5 V to 3.6 V                   |
| Input voltage range, V <sub>I</sub> (see Notes 1 and 2)                                          | –0.5 V to V <sub>DDQ</sub> 0.5 V |
| Output voltage range, V <sub>O</sub> (see Notes 1 and 2)                                         | –0.5 V to V <sub>DDQ</sub> 0.5 V |
| Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DDQ</sub> )  | ±50 mA                           |
| Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DDQ</sub> ) | ±50 mA                           |
| Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>DDQ</sub> )              | ±50 mA                           |
| Continuous current to GND or V <sub>DDQ</sub>                                                    | ±100 mA                          |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package                               | 89°C/W                           |
| Storage temperature range T <sub>stg</sub>                                                       | –65°C to 150°C                   |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This value is limited to 3.6 V maximum.
  3. The package thermal impedance is calculated in accordance with JESD 51.

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### recommended operating conditions (see Note 4)

|                                                                     |                                                               |           | MIN                        | TYP                 | MAX                       | UNIT |
|---------------------------------------------------------------------|---------------------------------------------------------------|-----------|----------------------------|---------------------|---------------------------|------|
| Supply voltage, V <sub>DDQ</sub> , AV <sub>DD</sub>                 |                                                               |           | 2.3                        |                     | 2.7                       | V    |
| Low level input voltage, V <sub>IL</sub>                            | CLK, $\overline{\text{CLK}}$ , FBIN, $\overline{\text{FBIN}}$ |           | V <sub>DDQ</sub> /2 – 0.18 |                     |                           | V    |
|                                                                     | PWRDWN                                                        |           | –0.3                       |                     | 0.7                       |      |
| High level input voltage, V <sub>IH</sub>                           | CLK, $\overline{\text{CLK}}$ , FBIN, $\overline{\text{FBIN}}$ |           | V <sub>DDQ</sub> /2 + 0.18 |                     |                           | V    |
|                                                                     | PWRDWN                                                        |           | 1.7                        |                     | V <sub>DDQ</sub> + 0.3    |      |
| DC input signal voltage (see Note 5)                                |                                                               |           | –0.3                       |                     | V <sub>DDQ</sub>          | V    |
| Differential input signal voltage, V <sub>ID</sub> (see Note 6)     | DC                                                            | CLK, FBIN | 0.36                       |                     | V <sub>DDQ</sub> + 0.6    | V    |
|                                                                     | AC                                                            | CLK, FBIN | 0.7                        |                     | V <sub>DDQ</sub> + 0.6    |      |
| Output differential cross-voltage, V <sub>OX</sub> (see Note 7)     |                                                               |           | V <sub>DDQ</sub> /2 – 0.2  | V <sub>DDQ</sub> /2 | V <sub>DDQ</sub> /2 + 0.2 | V    |
| Input differential pair cross-voltage, V <sub>IX</sub> (see Note 7) |                                                               |           | V <sub>DDQ</sub> /2 – 0.2  |                     | V <sub>DDQ</sub> /2 + 0.2 | V    |
| High-level output current, I <sub>OH</sub>                          |                                                               |           |                            |                     | –12                       | mA   |
| Low-level output current, I <sub>OL</sub>                           |                                                               |           |                            |                     | 12                        | mA   |
| Input slew rate, SR                                                 |                                                               |           | 1                          |                     | 4                         | V/ns |
| Operating free-air temperature, T <sub>A</sub>                      |                                                               |           | 0                          |                     | 85                        | °C   |

- NOTES: 4. Unused inputs must be held high or low to prevent them from floating.  
5. DC input signal voltage specifies the allowable dc execution of differential input.  
6. Differential input signal voltage specifies the differential voltage  $|V_{TR} - V_{CP}|$  required for switching, where  $V_{TR}$  is the true input level and  $V_{CP}$  is the complementary input level.  
7. Differential cross-point voltage is expected to track variations of  $V_{CC}$  and is the voltage at which the differential signals must be crossing.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER         |                                                           |                                                | TEST CONDITIONS                                                                | MIN                       | TYP <sup>†</sup>       | MAX                       | UNIT |
|-------------------|-----------------------------------------------------------|------------------------------------------------|--------------------------------------------------------------------------------|---------------------------|------------------------|---------------------------|------|
| V <sub>IK</sub>   | Input voltage                                             | All inputs                                     | V <sub>DDQ</sub> = 2.3 V, I <sub>I</sub> = –18 mA                              |                           |                        | –1.2                      | V    |
| V <sub>OH</sub>   | High-level output voltage                                 |                                                | V <sub>DDQ</sub> = min to max, I <sub>OH</sub> = –1 mA                         | V <sub>DDQ</sub> – 0.1    |                        |                           | V    |
|                   |                                                           |                                                | V <sub>DDQ</sub> = 2.3 V, I <sub>OH</sub> = –12 mA                             | 1.7                       |                        |                           |      |
| V <sub>OL</sub>   | Low-level output voltage                                  |                                                | V <sub>DDQ</sub> = min to max, I <sub>OL</sub> = 1 mA                          |                           |                        | 0.1                       | V    |
|                   |                                                           |                                                | V <sub>DDQ</sub> = 2.3 V, I <sub>OL</sub> = 12 mA                              |                           |                        | 0.6                       |      |
| I <sub>OH</sub>   | High-level output current                                 |                                                | V <sub>DDQ</sub> = 2.3 V, V <sub>O</sub> = 1 V                                 | –18                       | –32                    |                           | mA   |
| I <sub>OL</sub>   | Low-level output current                                  |                                                | V <sub>DDQ</sub> = 2.3 V, V <sub>O</sub> = 1.2 V                               | 26                        | 35                     |                           | mA   |
| V <sub>O</sub>    | Output voltage swing                                      | Differential outputs are terminated with 120 Ω |                                                                                | 1.1                       | V <sub>DDQ</sub> – 0.4 |                           | V    |
| V <sub>OX</sub>   | Output differential cross-voltage <sup>§</sup>            |                                                |                                                                                | V <sub>DDQ</sub> /2 – 0.2 | V <sub>DDQ</sub> /2    | V <sub>DDQ</sub> /2 + 0.2 |      |
| I <sub>I</sub>    | Input current                                             |                                                | V <sub>DDQ</sub> = 2.7 V, V <sub>I</sub> = 0 V to 2.7 V                        |                           |                        | ±10                       | μA   |
| I <sub>OZ</sub>   | High-impedance-state output current                       |                                                | V <sub>DDQ</sub> = 2.7 V, V <sub>O</sub> = V <sub>DDQ</sub> or GND             |                           |                        | ±10                       | μA   |
| I <sub>DDPD</sub> | Power down current on V <sub>DDQ</sub> + AV <sub>DD</sub> |                                                | CLK and CLK̄ = 0 MHz; PWRDWN = Low; Σ of I <sub>DD</sub> and A <sub>I</sub> DD |                           | 100                    | 200                       | μA   |
| I <sub>DD</sub>   | Dynamic current on V <sub>DDQ</sub>                       | all outputs loaded as shown in Figure 3        | f <sub>O</sub> = 200 MHz                                                       |                           | 275                    | 330                       | mA   |
|                   |                                                           |                                                | f <sub>O</sub> = 167 MHz                                                       |                           | 250                    | 300                       |      |
| A <sub>I</sub> DD | Supply current on AV <sub>DD</sub>                        | f <sub>O</sub> = 200 MHz                       |                                                                                |                           | 10                     | 12                        | mA   |
|                   |                                                           | f <sub>O</sub> = 167 MHz                       |                                                                                |                           | 8                      | 10                        |      |
| C <sub>I</sub>    | Input capacitance                                         |                                                | V <sub>CC</sub> = 2.5 V V <sub>I</sub> = V <sub>CC</sub> or GND                | 2                         | 2.5                    | 3                         | pF   |
| C <sub>O</sub>    | Output capacitance                                        |                                                | V <sub>CC</sub> = 2.5 V V <sub>O</sub> = V <sub>CC</sub> or GND                | 2.5                       | 3                      | 3.5                       | pF   |

<sup>†</sup> All typical values are at respective nominal V<sub>DDQ</sub>.

<sup>‡</sup> The value of V<sub>OC</sub> is expected to be |V<sub>T</sub>R + V<sub>CP</sub>|/2. In case of each clock directly terminated by a 120-Ω resistor, where V<sub>T</sub>R is the true input signal voltage and V<sub>CP</sub> is the complementary input signal voltage.

<sup>§</sup> Differential cross-point voltage is expected to track variations of V<sub>DDQ</sub> and is the voltage at which the differential signals must be crossing.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature**

|                 |                                               | MIN | MAX | UNIT |
|-----------------|-----------------------------------------------|-----|-----|------|
| f <sub>CK</sub> | Operating clock frequency                     | 60  | 200 | MHz  |
|                 | Application clock frequency                   |     |     |      |
|                 | Input clock duty cycle                        | 40% | 60% |      |
|                 | Stabilization time <sup>¶</sup> (PLL mode)    |     | 10  | μs   |
|                 | Stabilization time <sup>¶</sup> (Bypass mode) |     | 30  | ns   |

<sup>¶</sup> Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

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### switching characteristics

| PARAMETER                                                                            | TEST CONDITIONS             | MIN         | TYP <sup>†</sup> | MAX | UNIT |
|--------------------------------------------------------------------------------------|-----------------------------|-------------|------------------|-----|------|
| $t_{PLH}^{\ddagger}$ Low to high level propagation delay time                        | Test mode/CLK to any output |             | 4.5              |     | ns   |
| $t_{PHL}^{\ddagger}$ High-to low level propagation delay time                        | Test mode/CLK to any output |             | 4.5              |     | ns   |
| $t_{jit(per)}^{\S}$ Jitter (period), See Figure 6                                    | 66 MHz                      | –90         |                  | 90  | ps   |
|                                                                                      | 100/133/167/200 MHz         | –75         |                  | 75  | ps   |
| $t_{jit(cc)}^{\S}$ Jitter (cycle-to-cycle), See Figure 3                             | 66 MHz                      | –180        |                  | 180 | ps   |
|                                                                                      | 100/133/167/200 MHz         | –75         |                  | 75  | ps   |
| $t_{jit(hper)}^{\S}$ Half-period jitter, See Figure 7                                | 66 MHz                      | –160        |                  | 160 | ps   |
|                                                                                      | 100/133/167/200 MHz         | –100        |                  | 100 | ps   |
| $t_{slr(i)}$ Input clock slew rate, See Figure 8                                     |                             | 1           |                  | 4   | V/ns |
| $t_{slr(o)}$ Output clock slew rate, See Figure 8                                    |                             | 1           |                  | 2   | V/ns |
| $t_{d(\emptyset)}^{\S}$ Dynamic phase offset (this includes jitter), See Figure 4(b) | SSC off                     | 66 MHz      | –180             | 180 | ps   |
|                                                                                      |                             | 100/133 MHz | –130             | 130 |      |
|                                                                                      |                             | 167/200 MHz | –90              | 90  |      |
|                                                                                      | SSC on                      | 66 MHz      | –230             | 230 |      |
|                                                                                      |                             | 100/133 MHz | –170             | 170 |      |
|                                                                                      |                             | 167/200 MHz | –100             | 100 |      |
| $t_{(\emptyset)}$ Static phase offset, See Figure 4(a)                               | 66/100/133/167 MHz          | –100        |                  | 100 | ps   |
|                                                                                      | 200 MHz                     | –150        |                  | 50  |      |
| $tsk(o)^{\parallel}$ Output skew, See Figure 5                                       |                             |             |                  | 75  | ps   |
| $t_r, t_f$ Output rise and fall times (20% – 80%)                                    | Load: 120 $\Omega$ /14 pF   | 650         |                  | 900 | ps   |

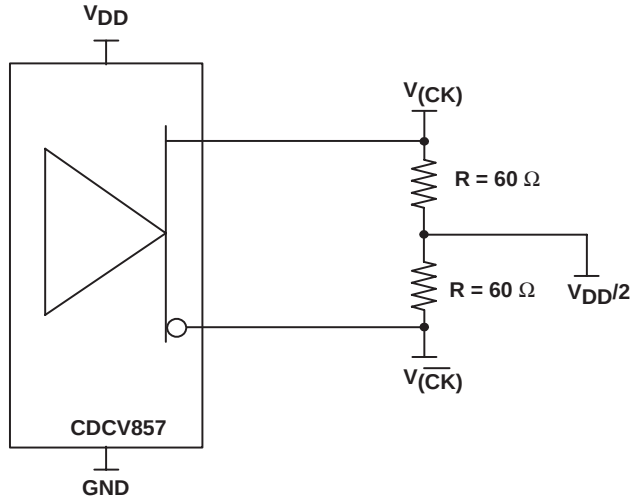
<sup>†</sup> All typical values are at a respective nominal  $V_{DDQ}$ .

<sup>‡</sup> Refers to transition of noninverting output.

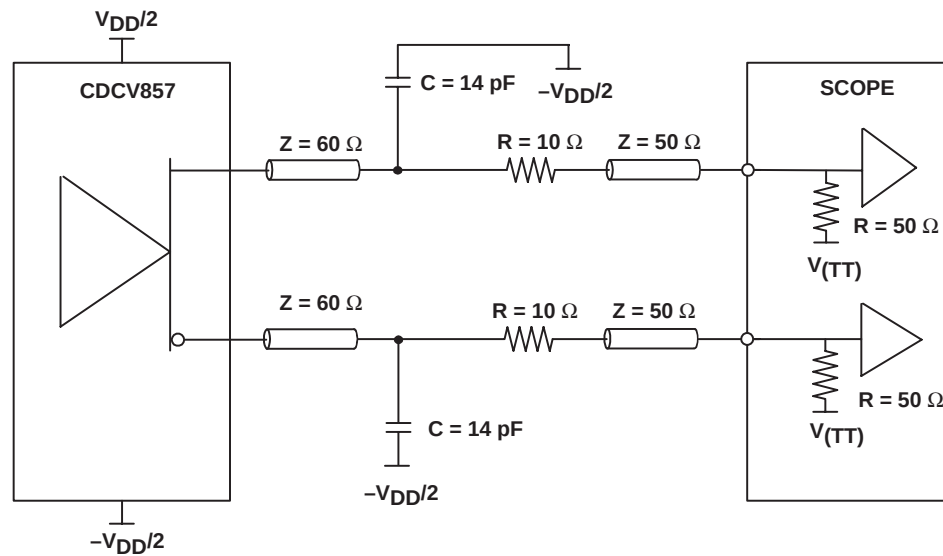
<sup>§</sup> This parameter is assured by design but can not be 100% production tested.

<sup>||</sup> All differential output pins are terminated with 120  $\Omega$ /14 pF.

### PARAMETER MEASUREMENT INFORMATION

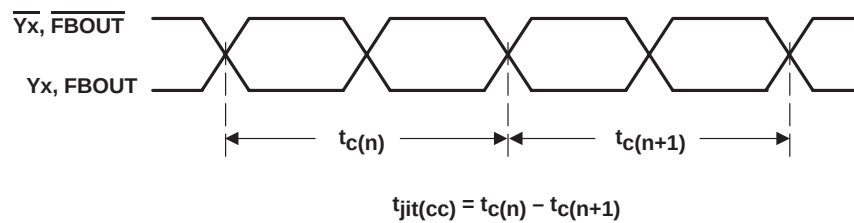


**Figure 1. IBIS Model Output Load (used for slew rate measurement)**



NOTE:  $V_{(TT)} = \text{GND}$

**Figure 2. Output Load Test Circuit**



**Figure 3. Cycle-to-Cycle Jitter**

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### PARAMETER MEASUREMENT INFORMATION

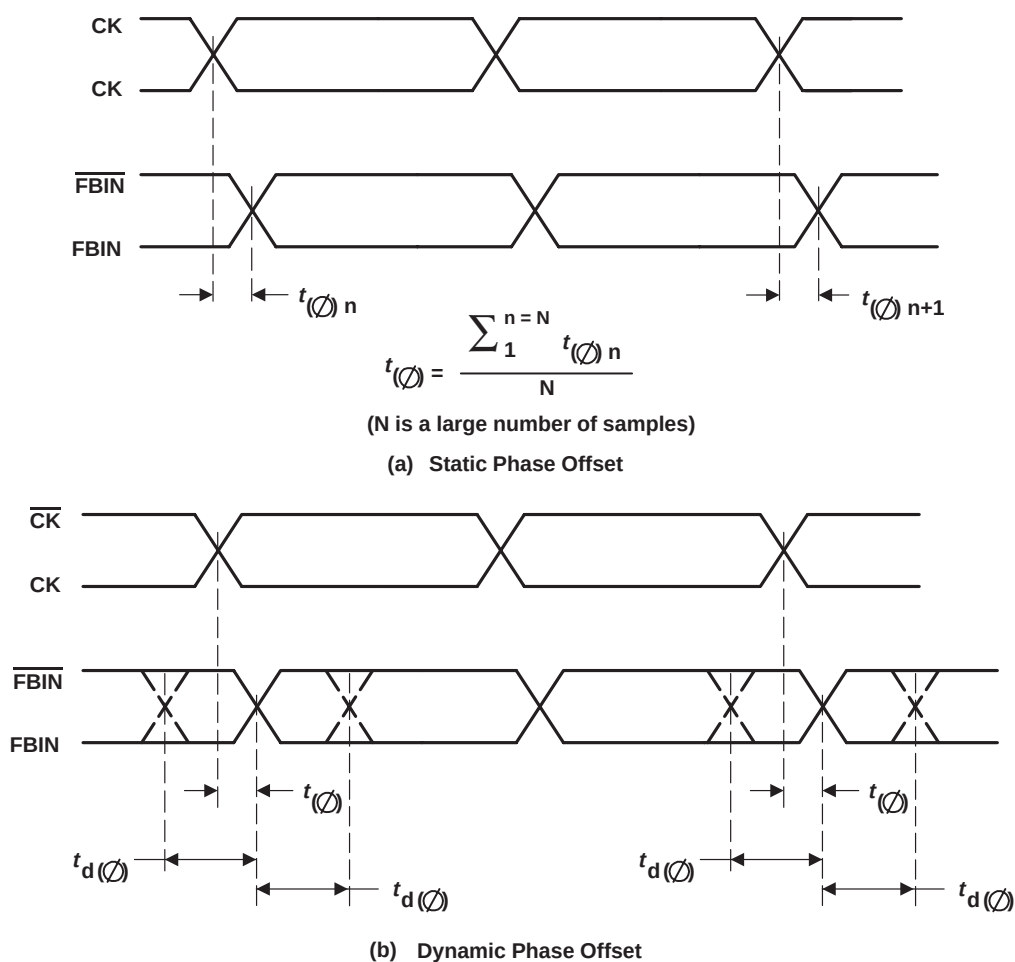


Figure 4. Phase Offset

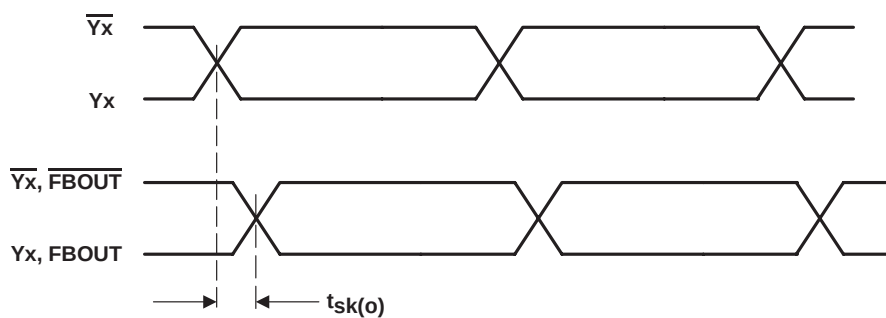


Figure 5. Output Skew



### PARAMETER MEASUREMENT INFORMATION

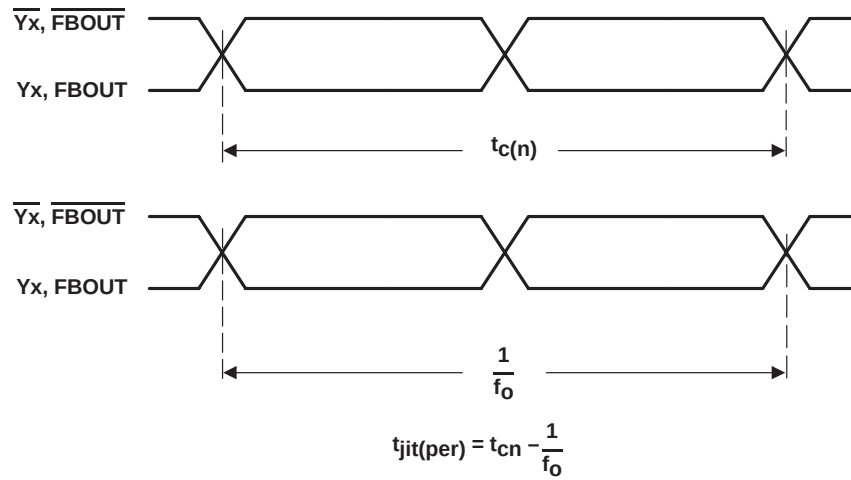


Figure 6. Period Jitter

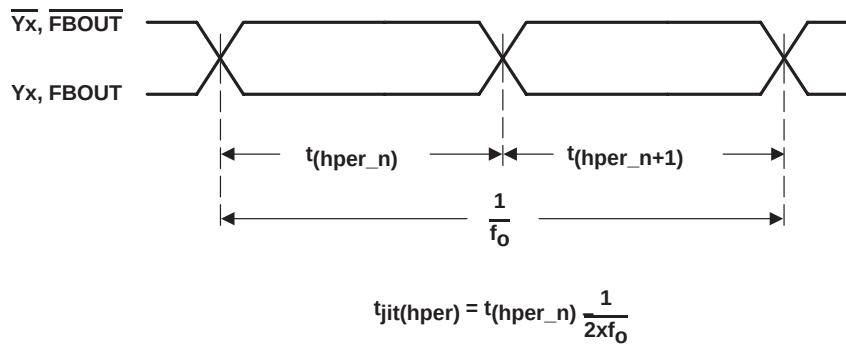


Figure 7. Half-Period Jitter



Figure 8. Input and Output Slew Rates

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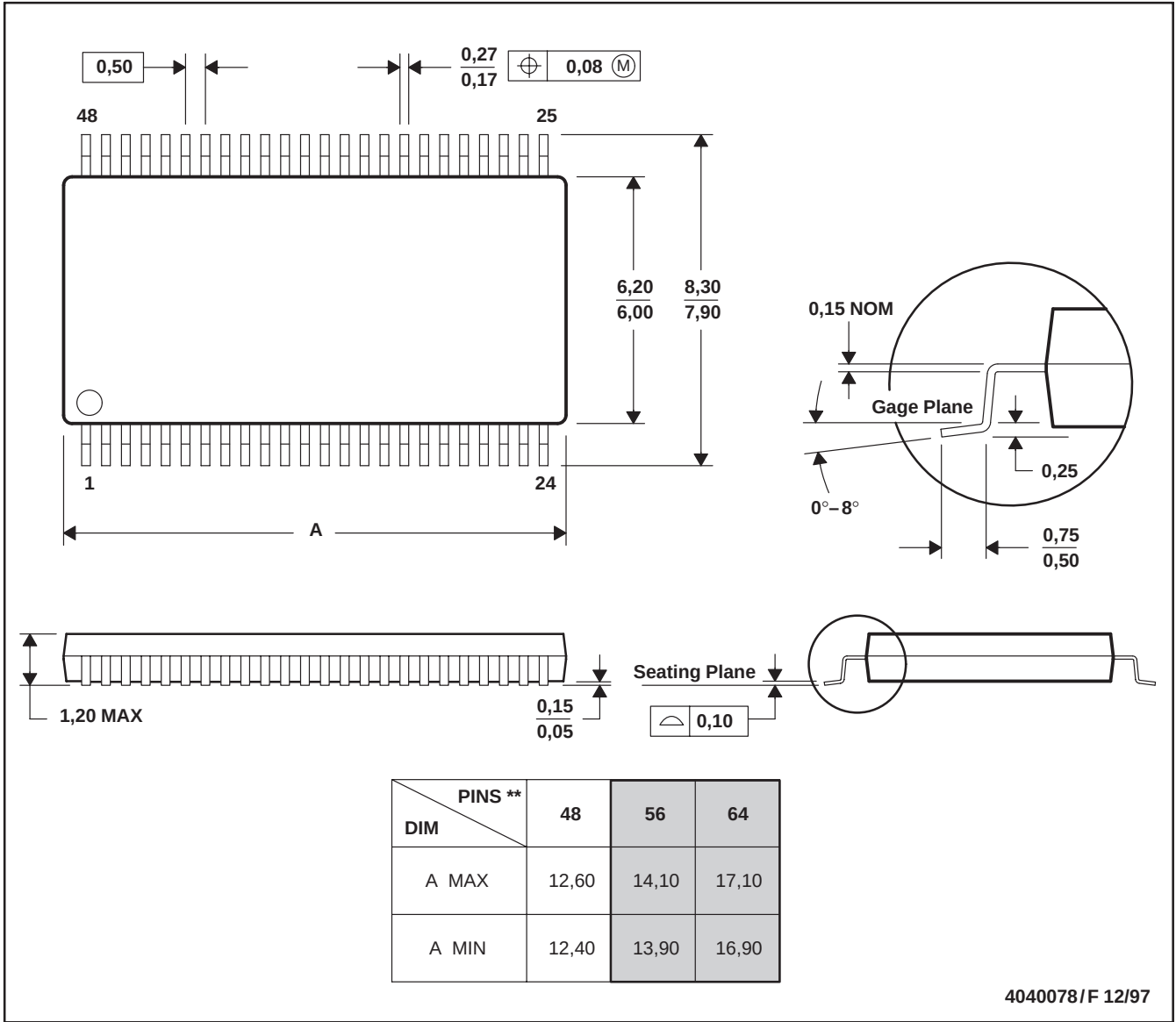
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MECHANICAL DATA

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold protrusion not to exceed 0,15.  
D. Falls within JEDEC MO-153

## PACKAGING INFORMATION

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CDCV857DGG       | ACTIVE                | TSSOP        | DGG             | 48   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| CDCV857DGGG4     | ACTIVE                | TSSOP        | DGG             | 48   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| CDCV857DGGR      | ACTIVE                | TSSOP        | DGG             | 48   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| CDCV857DGGRG4    | ACTIVE                | TSSOP        | DGG             | 48   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

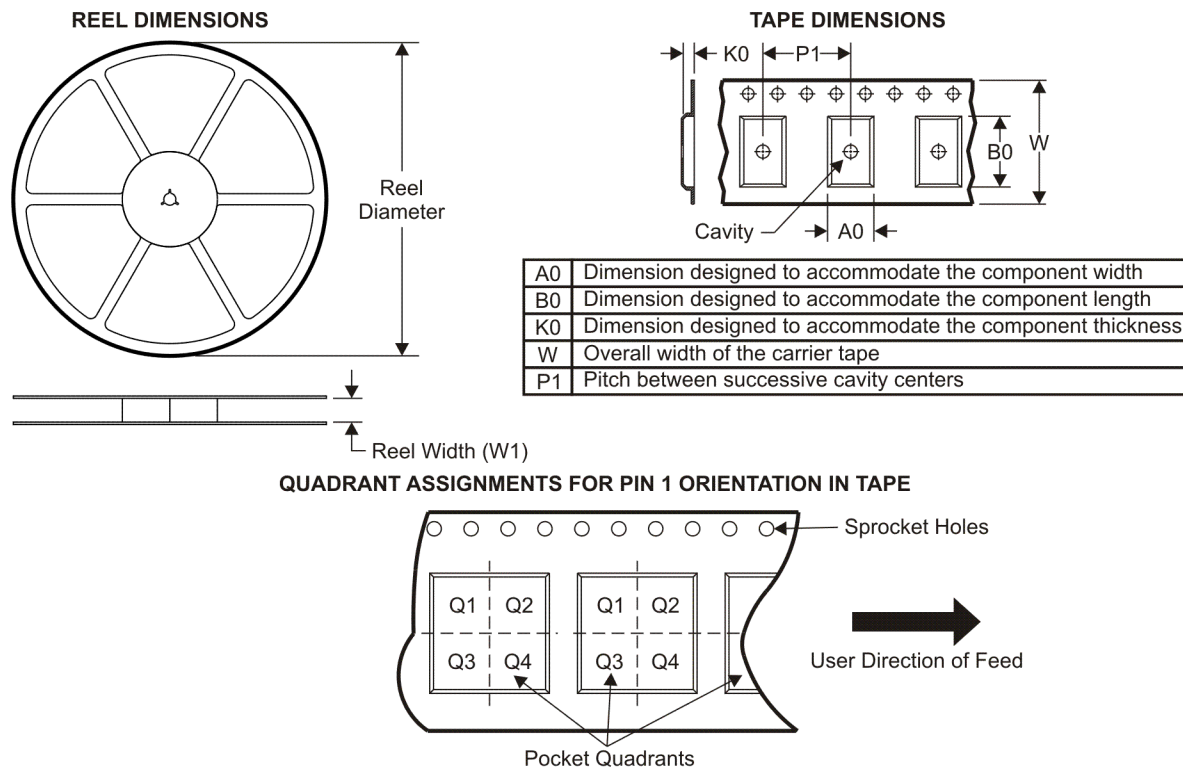
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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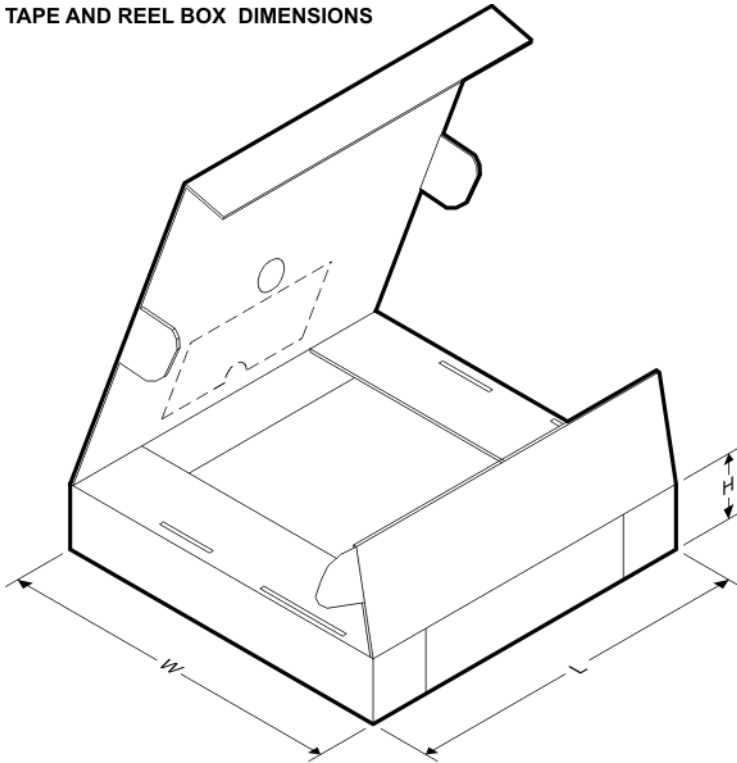
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCV857DGGR | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 15.8    | 1.8     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDCV857DGGR | TSSOP        | DGG             | 48   | 2000 | 346.0       | 346.0      | 41.0        |

## IMPORTANT NOTICE

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|                    |                                                                          |
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