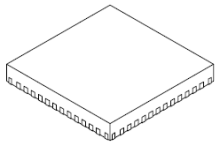
TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB67H400AFTG

PWM Chopper-Type Brushed DC Motor Driver

1. Description

The TB67H400AFTG is brushed DC motor driver of a PWM chopper-type.
The TB67H400AFTG is a dual channel H-SW driver which can control two brushed DC motors. Moreover, the parallel control function (Large mode) of an output part is built in, and 1ch high current drive is also possible. Fabricated with the BiCD process, the TB67H400AFTG is rated at 50 V, 4.0 A (2 ch)/8.0 A (1 ch).



P-WQFN48-0707-0.50-003

Weight: 0.10 g (Typ.)

2. Features

- Monolithic motor driver using BiCD process.
- Capable of controlling two brushed DC motor.
- 2 drive modes (PWM controlled constant current/ direct PWM)
- 4 operation modes (Clock-wise/Counter clock-wise/Brake/Stop (Off))
- Low on-resistance output stage (High side+Low side:0.49 Ω (Typ.))
- High voltage and current (for specification, please refer to absolute maximum ratings and operating ranges.)
- Built-in error detection circuits (Thermal shutdown (TSD), over-current detection (ISD), and power-on reset (POR)).
- The VCC regulator for internal circuit operation is built in.
- Able to customize PWM (internal chopping) frequency by external components.

Note: Please be careful about the thermal conditions during use.

Start of commercial production
2015-03

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3. Pin Assignment

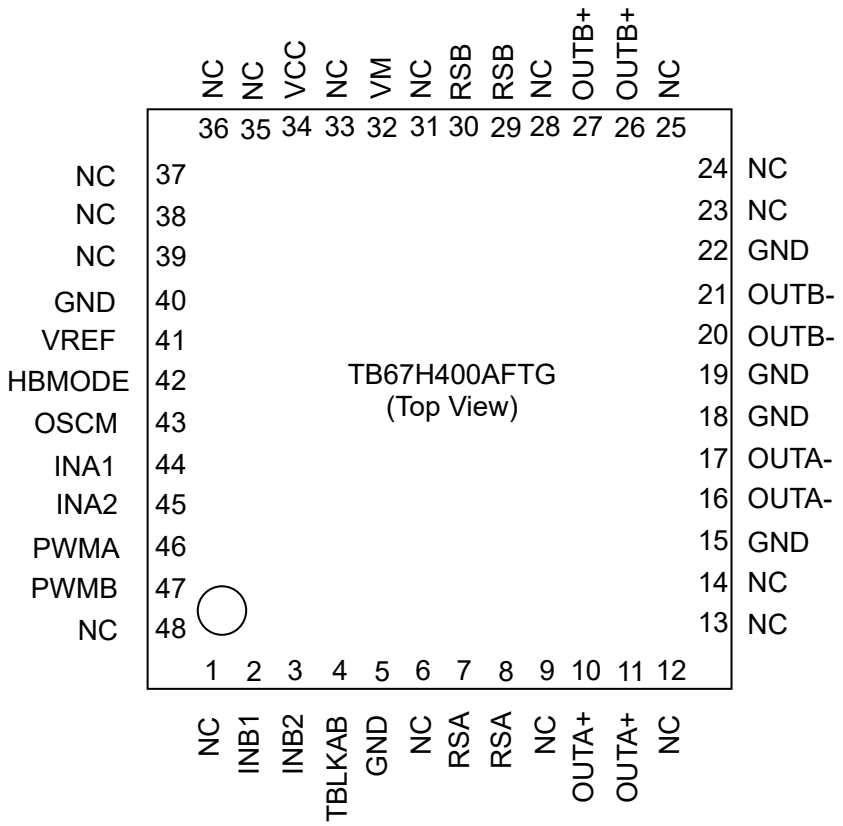

Figure3 Pin Assignment

Note: Please connect the WQFN package corner pad and the exposed pad to the PCB ground pattern.

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4. Block diagram

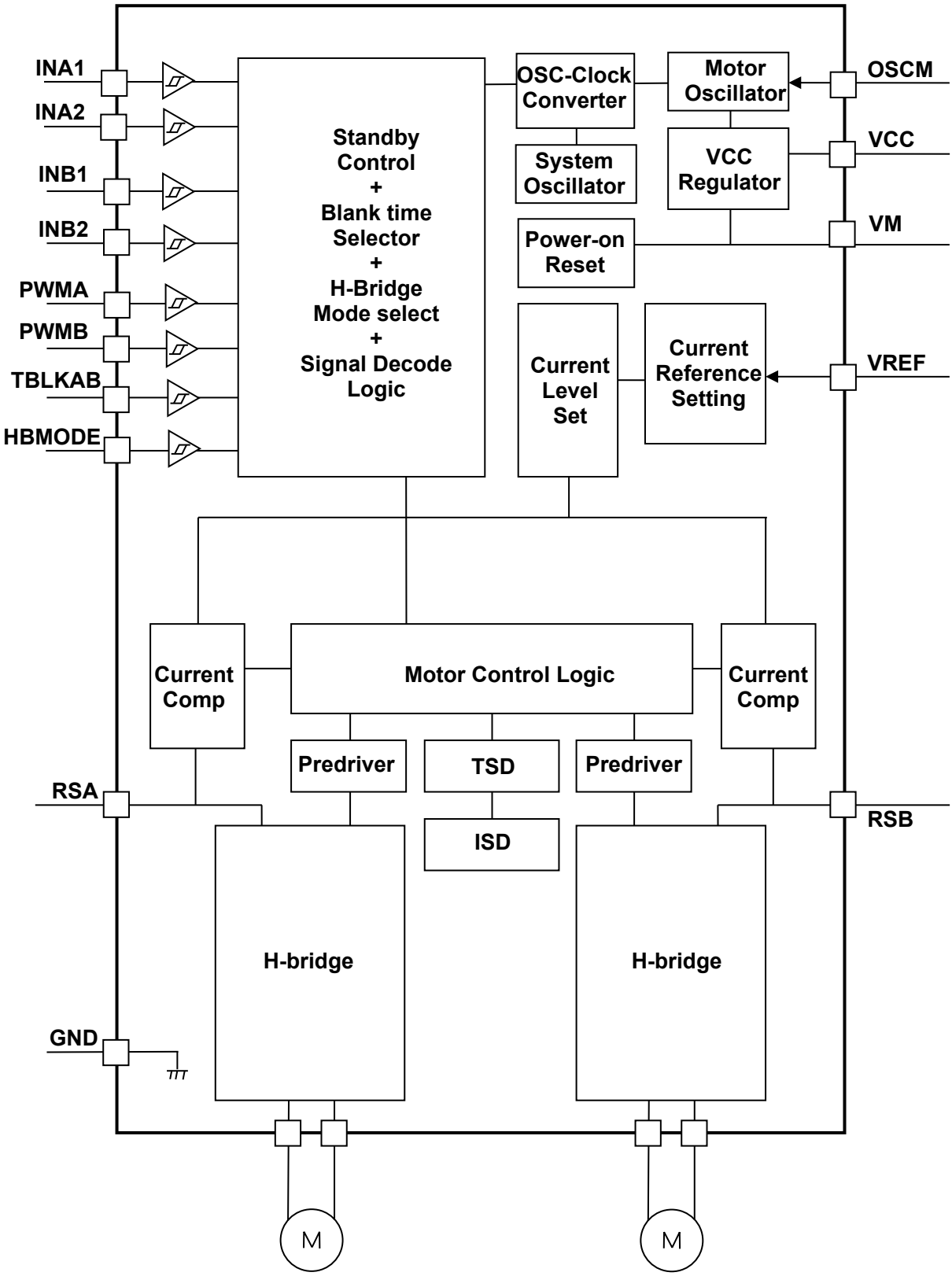

Figure 4 Block diagram

Note: Please note that in the block diagram, functional blocks or constants may be omitted or simplified for explanatory purposes.

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Note: All the grounding wires of the TB67H400AFTG must run on the solder mask of the PCB. It must also be externally terminated at a single point. Also, the grounding method should be considered for efficient heat dissipation.Careful attention should be paid to the layout of the output, VM and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged.Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VM, RS, OUT, and GND) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed.The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current. Careful attention should be paid to design patterns and mountings.

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5. Pin Description

Table5 Pin Description

Pin No.	Pin name	Function
1	NC	Non connection
2	INB1	Motor Bch IN1 signal input pin
3	INB2	Motor Bch IN2 signal input pin
4	TBLKAB	Motor Ach and Bch Digital tBLK setting pin
5	GND	Ground pin
6	NC	Non connection
7	RSA	Motor Ach output current sense pin
8	RSA	Motor Ach output current sense pin
9	NC	Non connection
10	OUTA+	Motor Ach+ output pin
11	OUTA+	Motor Ach+ output pin
12	NC	Non connection
13	NC	Non connection
14	NC	Non connection
15	GND	Ground pin
16	OUTA-	Motor Ach- output pin
17	OUTA-	Motor Ach- output pin
18	GND	Ground pin
19	GND	Ground pin
20	OUTB-	Motor Bch- output pin
21	OUTB-	Motor Bch- output pin
22	GND	Ground pin
23	NC	Non connection
24	NC	Non connection
25	NC	Non connection
26	OUTB+	Motor Bch+ output pin
27	OUTB+	Motor Bch+ output pin
28	NC	Non connection

Note: Please do not connect any pattern to the NC pin.
Please connect the pins with the same names, at the nearest point of the device.

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Pin No.	Pin name	Function
29	RSB	Motor Bch output current sense pin
30	RSB	Motor Bch output current sense pin
31	NC	Non connection
32	VM	Motor Voltage supply pin
33	NC	Non connection
34	VCC	Internal regulator voltage monitor pin
35	NC	Non connection
36	NC	Non connection
37	NC	Non connection
38	NC	Non connection
39	NC	Non connection
40	GND	Ground pin
41	VREF	Motor output current setting pin
42	HBMODE	H-Bridge operation mode setting pin
43	OSCM	Oscillator frequency setting pin
44	INA1	Motor Ach IN1 signal input pin
45	INA2	Motor Ach IN2 signal input pin
46	PWMA	Motor Ach short brake signal input pin
47	PWMB	Motor Bch short brake signal input pin
48	NC	Non connection

Note: Please do not connect any pattern to the NC pin.
Please connect the pins with the same names, at the nearest point of the device.

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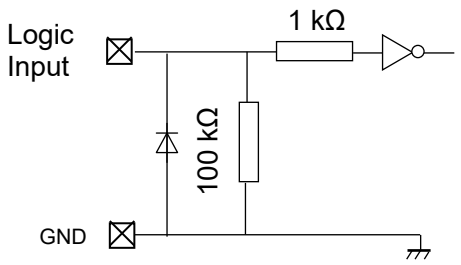
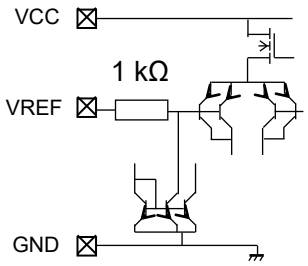
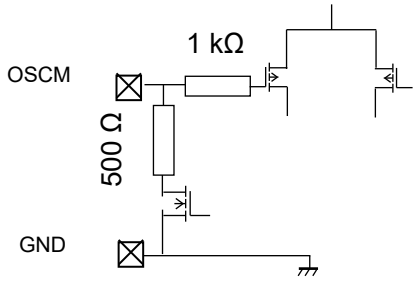
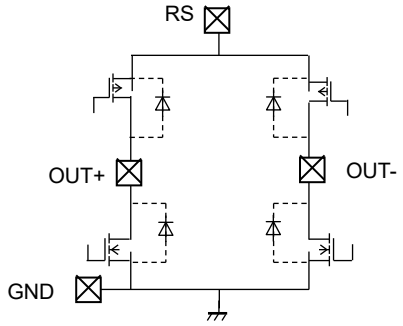
6. Input / Output Equivalent Circuit

Table6 Input / Output Equivalent Circuit

Pin name	Input/output signal	Equivalent circuit
INA1 INA2 PWMA INB1 INB2 PWMB TBLKAB HBMODE	Digital input (V_{IH}/V_{IL}) V_{IH}: 2.0 V (Min) to 5.5 V (Max) V_{IL} : 0 V (Min) to 0.8 V (Max)	
VCC VREF	V_{CC} regulator specification 4.75 V (Min) to 5.0 V (Typ.) to 5.25 V (Max) V_{REF} input voltage range 0 V to 4.0 V	
OSCM	OSCM setup frequency 0.64 MHz (Min) to 1.12 MHz (Typ.) to 2.4 MHz (Max)	
OUTA+ OUTA- OUTB+ OUTB- RSA RSB	V_M operation range 10 V (Min) to 47 V (Max) OUTPUT pin voltage range 10 V (Min) to 47 V (Max)	

Note: The equivalent circuit diagrams may be simplified for explanatory purposes.

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7. Operation Description

7.1. Logic input function table

INA1, INA2
These pins set the drive mode for Motor Ach.

Table7.1.1 INA1,INA2 Pin

	PWMA	INA1	INA2	OUTA+	OUTA-	Function
INPUT	L	L	L	OFF (Hi-Z)	OFF (Hi-Z)	STANDBY MODE (Note)
	H					STOP (OFF)
	L	L	H	L	L	Short brake
	H			L	H	CCW (Counter clock-wise)
	L	H	L	L	L	Short brake
	H			H	L	CW (Clock-wise)
	L	H	H	L	L	Short brake
	H					

INB1, INB2
These pins set the drive mode for Motor Bch.

Table7.1.2 INB1,INB2 Pin

	PWMB	INB1	INB2	OUTB+	OUTB-	Function
INPUT	L	L	L	OFF (Hi-Z)	OFF (Hi-Z)	STANDBY MODE (Note)
	H					STOP (OFF)
	L	L	H	L	L	Short brake
	H			L	H	CCW (Counter clock-wise)
	L	H	L	L	L	Short brake
	H			H	L	CW (Clock-wise)
	L	H	H	L	L	Short brake
	H					

Note: The standby mode is only enabled when all 6 logic input pins (INA1, INA2, PWMA, INB1, INB2, and PWMB) are set to Low level.

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TBLKAB
This pin will set the noise rejection time.

Table7.1.3 TBLKAB Pin

TBLKAB	TBLK noise rejection time
L	Digital $t_{BLK} = f_{OSCM} \times 4$ clk
H	Digital $t_{BLK} = f_{OSCM} \times 6$ clk

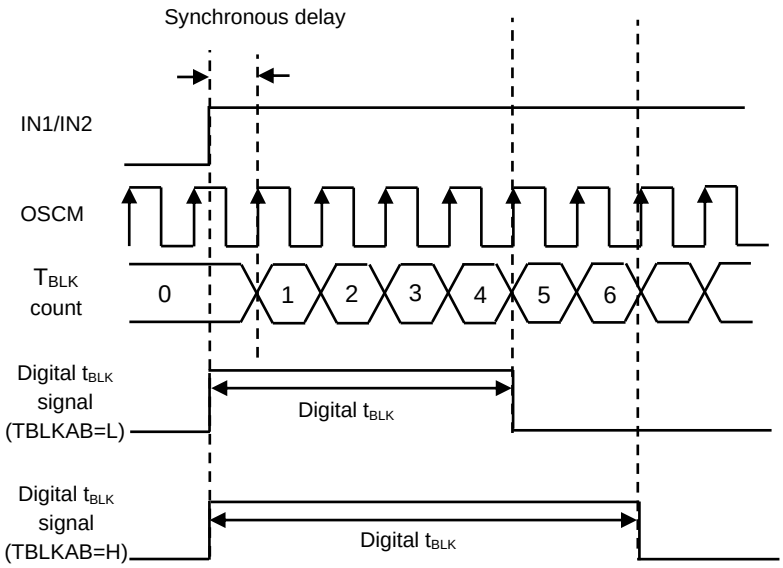

Figure7.1 TBLKAB Pin

Note: ・Please note that the timing charts or constants may be omitted or simplified for explanatory.
・The Digital t_{BLK} is used to avoid error judgment of varistor recovery current that occurs in charge drive mode when H-bridges are used with DC motors. The Digital t_{BLK} time can be controlled with TBLKAB pin.
By setting Digital t_{BLK}, direct PWM control and constant current control is possible, but the motor current will rise above the predefined current level (NF) while digital t_{BLK} is active.
・Besides Digital $t_{BLK,}$ Analog t_{BLK} (400 ns Typ.)) settled by an internal constant of IC is also attached.

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7.2. Digital t_{BLK} timing for Brushed DC Motor

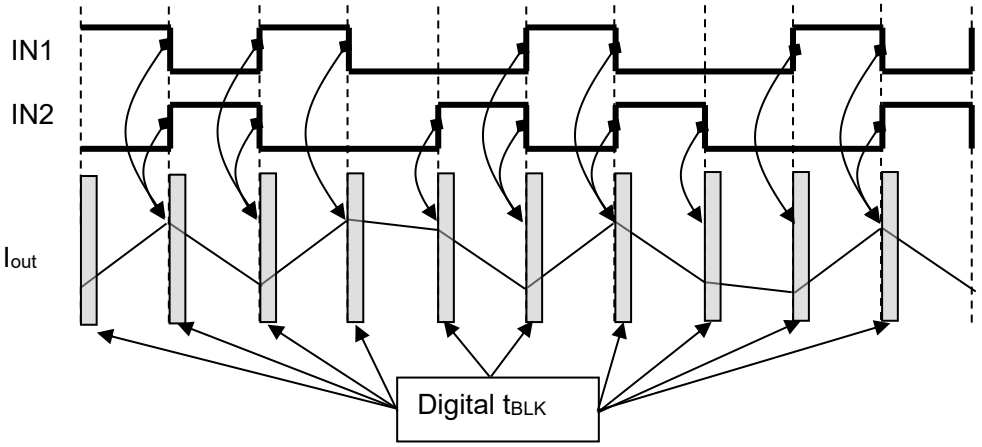

Figure7.2.1 Digital t_{BLK} timing for Brushed DC Motor

The Digital t_{BLK} is inserted at the beginning of each charge period of the constant current chopping, and also when either of INA1, INA2, INB1, or INB2 is switched.

Note: Please note that the timing charts or constants may be omitted or simplified for explanatory.

HBMODE
This pin sets the H-Bridge operation mode.

Table 7.2.1 HBMODE Pin

Pin name	Function	Input	Setting
HBMODE	H-Bridge operation setting	L	Small mode
		H	Large mode

Note: ・When using the Large mode, please make sure that the impedance between A channel and B channel is balanced. Also, make sure that the output pins (OUTA+ and OUTA-, OUTB+ and OUTB-), RS pins (RSA and RSB) are connected to each other when using the Large mode.
・Please set the HBMODE to Low or High with the PCB pattern. (Do not change the logic input level during operation.)
・When the HBMODE pin is set to High level, the motor control will be controlled by the Ach inputs (INA1, INA2, and PWMA). The Bch inputs (INB1, INB2, and PWMB) will be invalid. (When using the TB67H400AFTG in the Large mode, setting the INB1, INB2, and PWMB to Low level is preferred.) TBLKAB pin is effective in both Small and Large modes (HBMODE=L/H).

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H-Bridge connection example in each mode

- 2 Small DC motor operation setting example (HBMODE=L)

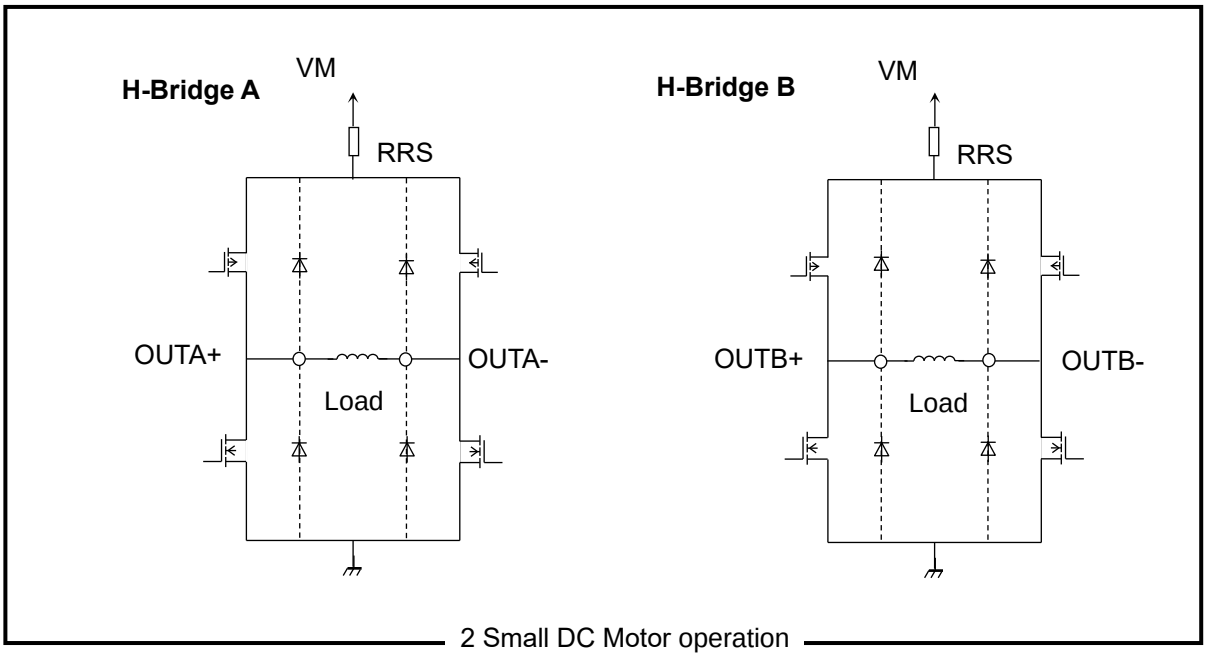

Figure7.2.2 2 Small DC motor operation setting example (HBMODE=L)

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- 1 Large DC motor operation setting example (HBMODE=H)

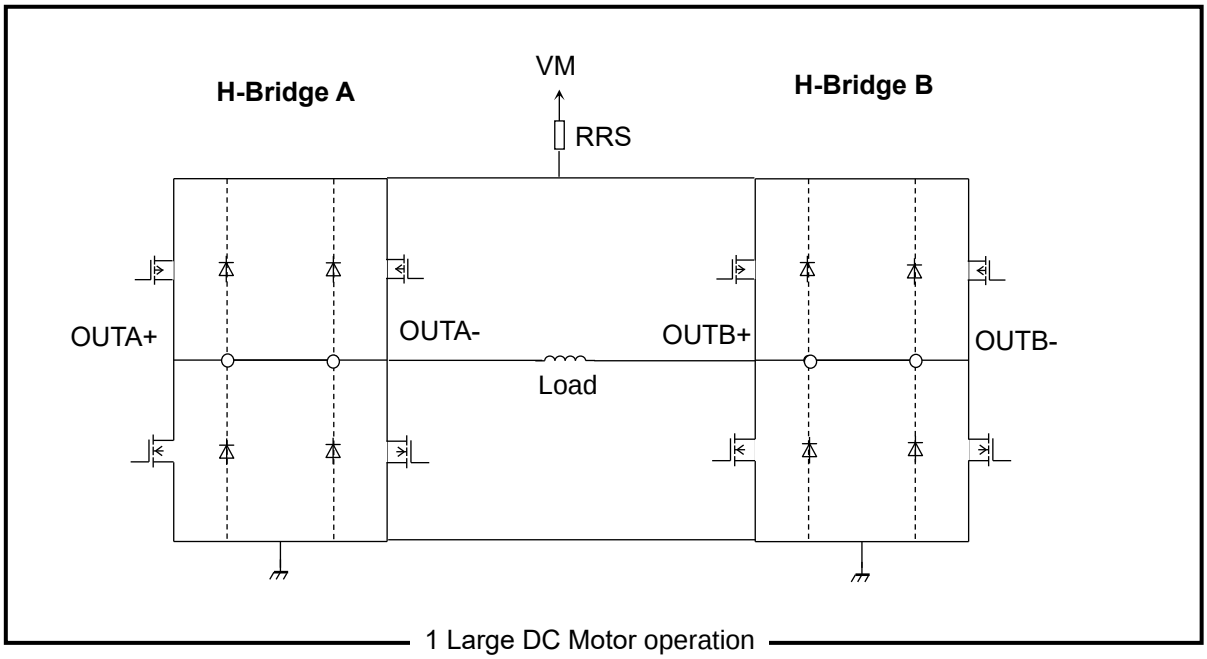

Figure 7.2.3 1 Large DC motor operation setting example (HBMODE=H)

Note: Please note that in the equivalent input circuit, functional blocks or constants may be omitted or simplified for explanatory purposes.

DC Small mode: H-Bridge A and B will operate separately (for two brushed DC motor operation)
DC Large mode: H-Bridge A and B will operate as a single H-Bridge. (for one brushed DC motor operation)

When the HBMODE is set to High level (Large mode), the pin function will be as follows.

Table 7.2.2 Large mode

Pin	HBMODE=H (Large mode)
INA1	INL1
INA2	INL2
PWMA	PWML
PWMB	Don't care (Motor will be Controlled by INL1, INL2, and PWML pins)
INB1	
INB2	
TBLKAB	TBLKL
RSA	RSL
RSB	
OUTA+	OUTL+
OUTA-	
OUTB+	OUTL-
OUTB-	

Note: Please connect the "RSA and RSB", "OUTA+ and OUTA-", and "OUTB+ and OUTB-"when using the Large mode operation.

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7.3. Motor control (constant current control)

Current waveform of Mixed Decay Mode, and a setting
In the case of constant current control, the rate of Mixed Decay Mode which determines the current ripple is fixed to 37.5%.

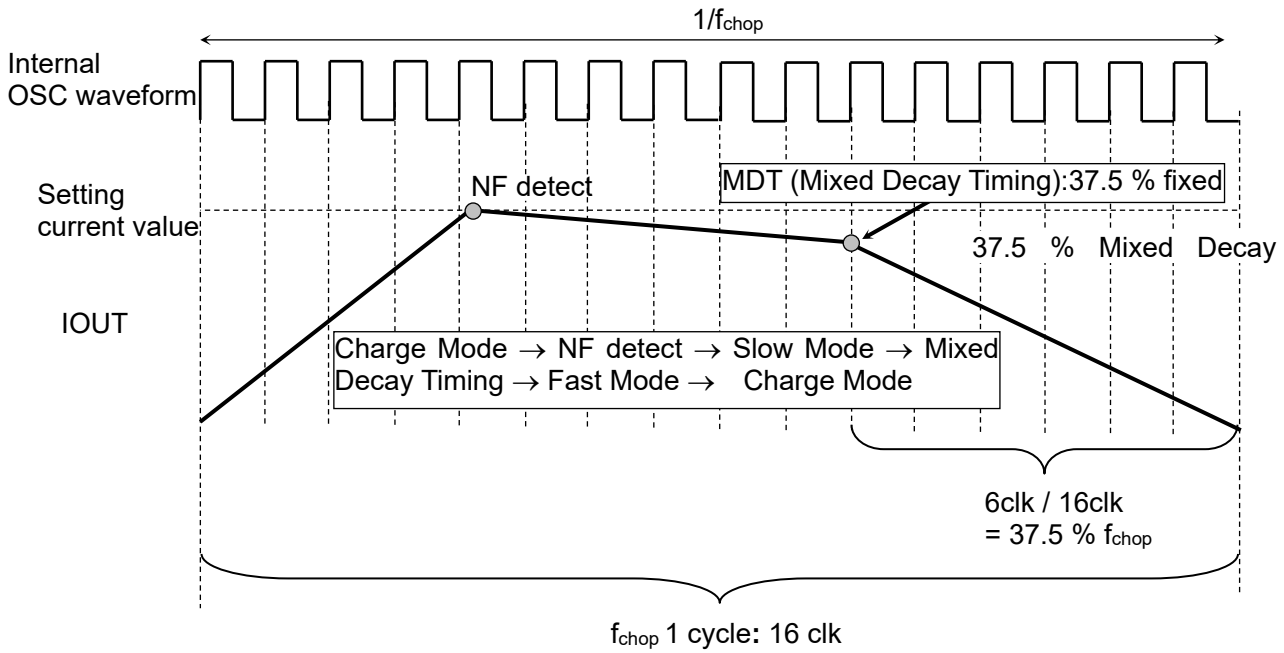

Figure7.3.1 Mixed Decay waveform 1

Mixed Decay Mode current waveform

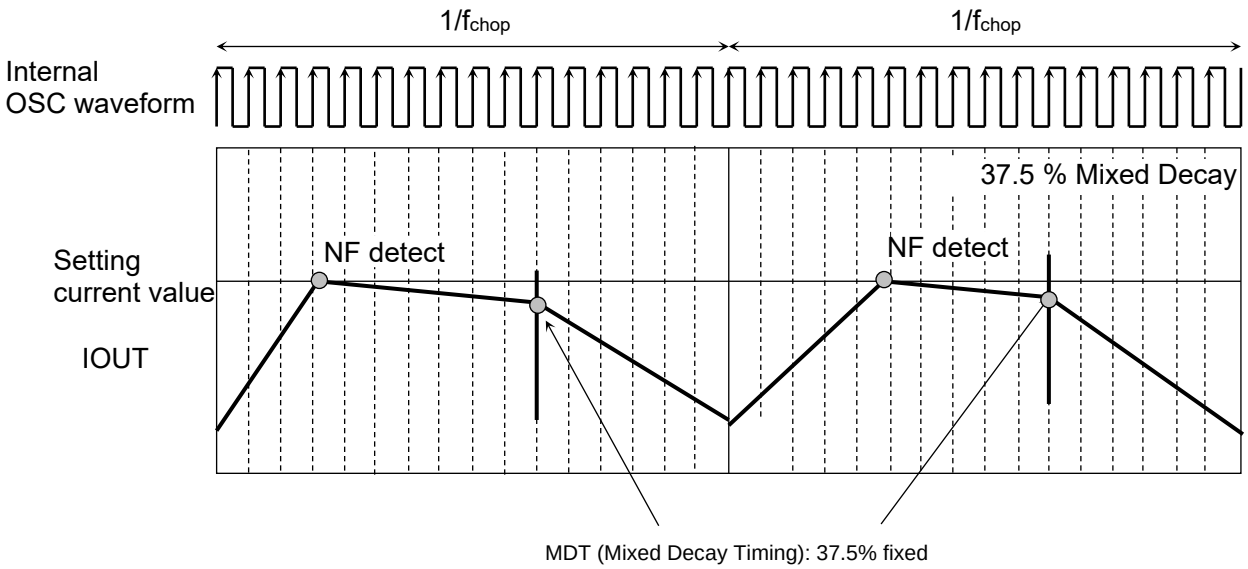

Figure7.3.2 Mixed Decay waveform 2

Note: Please note that the timing charts or constants may be omitted or simplified for explanatory.

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7.4. Current waveform in Mixed (Slow + Fast) Decay Mode

- When a current value increases (Mixed Decay point is fixed to 37.5 %)

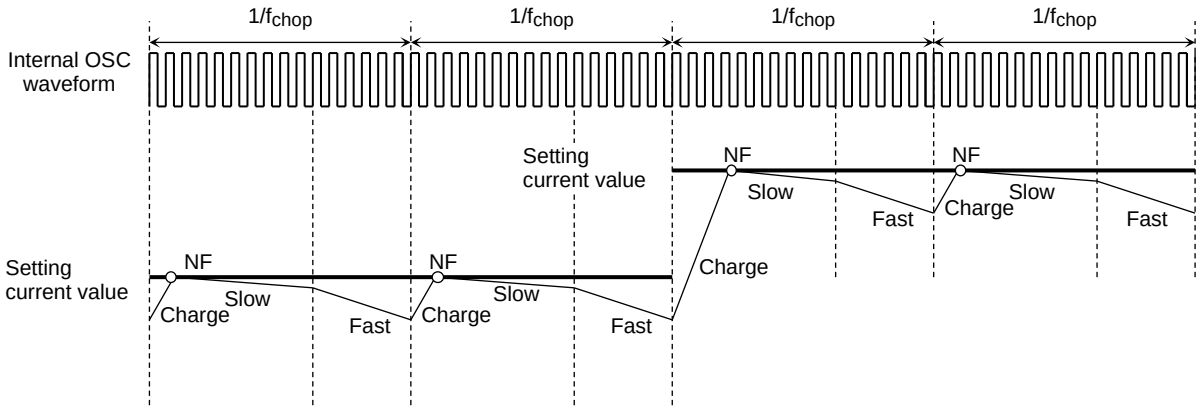

Figure7.4.1 If the set current value is in the increasing direction

- When a current value decreases (Mixed Decay timing = 37.5 %)

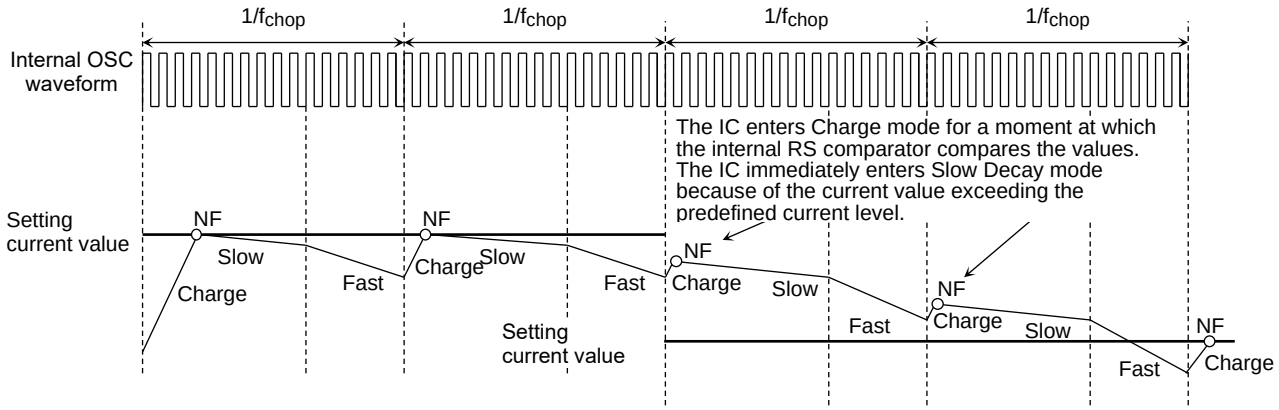

Figure7.4.2 When the set current value is in the decreasing direction

The Charge period starts as the internal oscillator clock starts counting. When the output current reaches the predefined current level, the internal RS comparator detects the predefined current level (NF); as a result, the IC enters Slow Decay mode.
The TB67H400AFTG transits from Slow Decay mode to Fast Decay mode at the point 37.5 % of a PWM frequency (one chopping frequency) remains in a whole PWM frequency period (on the rising edge of the 11th clock of the OSCM clock).
When the OSCM pin clock counter clocks 16 times, the Fast Decay mode ends; and at the same time, the counter is reset, which brings the TB67H400AFTG into Charge mode again.

Note: These figures are intended for illustrative purposes only. If designed more realistically, they would show transient response curves.
Note: Please note that the timing charts or constants may be omitted or simplified for explanatory.

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8. Output stage transistor operation mode (Advanced Dynamic Mixed Decay)

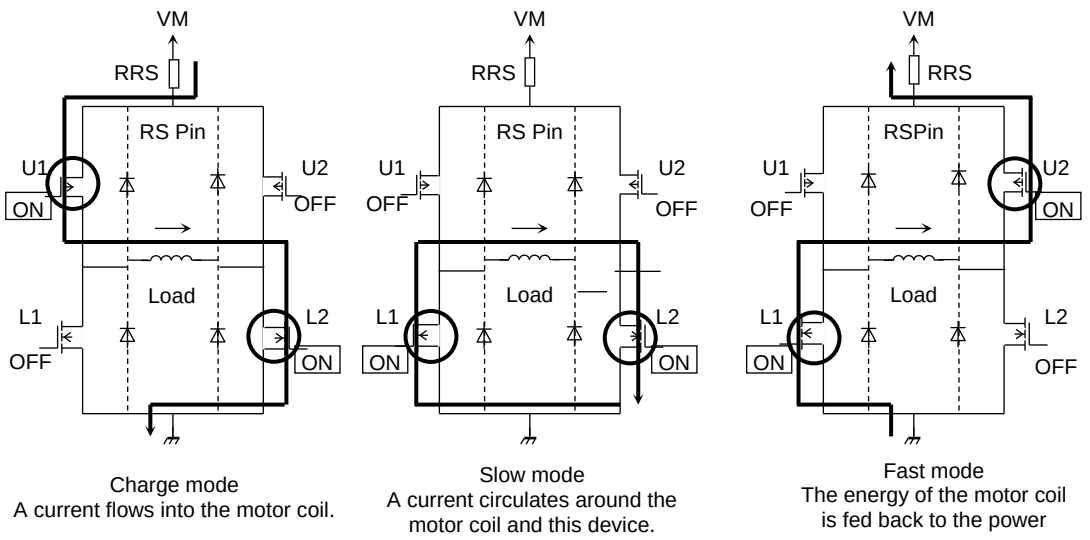

Figure8 Output stage transistor operation mode 1

8.1. Output transistor operational function

Table8.1.1 Function of output stage transistor operation 1

MODE	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: The parameters shown in the table above are examples when the current flows in the directions shown in the figures above.
For the current flowing in the reverse direction, the parameters change as shown in the table below.

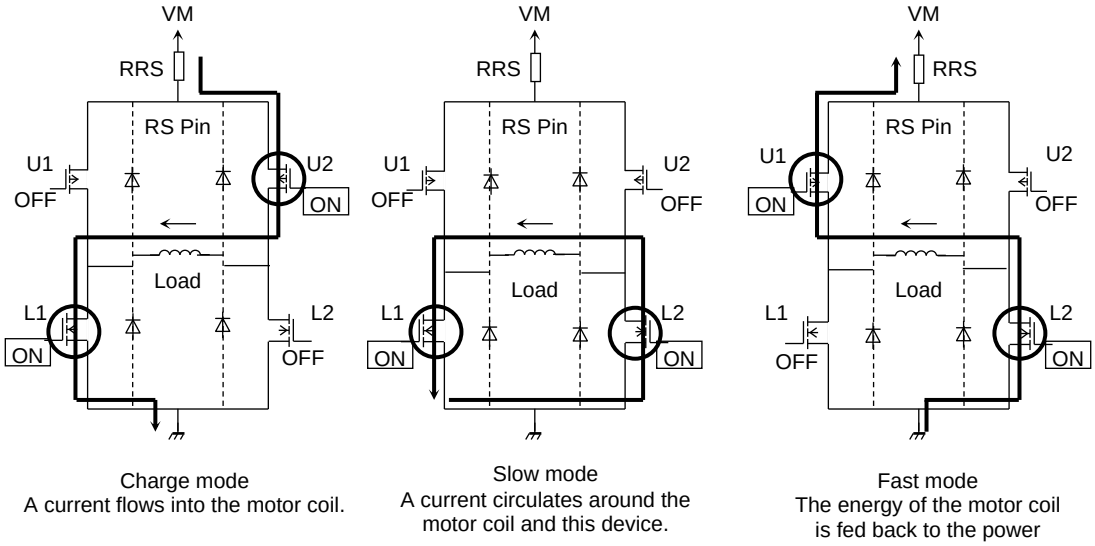

Figure8.1 Output stage transistor operation mode 2

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Table8.1.2 Function of output stage transistor operation 2

MODE	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

Note: This IC controls the motor current to be constant by 3 modes listed above.
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

9. Calculation of the predefined output current

For PWM constant current control, this IC uses a clock generated by the OSCM oscillator.
The peak output current (Setting current value) can be set via the current-sensing resistor (R_{RS}) and the reference voltage (V_{ref}), as follows:

$$I_{out}\,(max) = V_{ref}\,(gain) \times \frac{V_{ref}\,(V)}{R_{RS}\,(\Omega)}$$

V_{ref} (gain): the V_{ref} decay rate is 1 / 5.0 (Typ.)

For example: In the case of a 100% setup
When V_{ref} is 3.0 V and RSS is 0.51 Ω, the motor constant current (Peak current) will be calculated as:

I_{out} = 3.0 V / 5.0 / 0.51 Ω= 1.18 A

10. Calculation of the OSCM oscillation frequency (chopper reference frequency)

An approximation of the OSCM oscillation frequency (f_{OSCM}) and chopper frequency (f_{chop}) can be calculated by the following expressions.

f_{OSCM} = 1 / [0.56 × {COSC × (ROSC + 500)}]
Note: COSC, ROSC: External components for OSCM (When COSC is 270 pF and ROSC is 5.1 kΩ, f_{OSCM} is about 1.12 MHz (typ.).)

f_{chop} = f_{OSCM} / 16
Note: When f_{OSCM} is 1.12 MHz, f_{chop} is about 70 kHz (typ.).

If chopping frequency is raised, the ripple of current will become small and wave-like reproducibility will improve. However, the gate loss inside IC goes up and generation of heat becomes large.

The standard frequency is about 70 kHz. A setup in the range of 50 to 100 kHz is recommended.

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11. Absolute maximum ratings (T_a = 25 °C)

Table11 Absolute maximum rating

Characteristics	Symbol	Rating	Unit	Remarks
Motor power supply	V_M	50	V	—
Motor output voltage	V_{out}	50	V	—
Motor output current	I_{out}(S)	4.0	A	Small mode (Note1)
	I_{out}(L)	8.0	A	Large mode (Note1)
VCC voltage	V_{CC}	6.0	V	—
Digital input voltage	$V_{IN(H)}$	6.0	V	—
	$V_{IN(L)}$	-0.4	V	—
Vref input voltage	V_{ref}	GND to 4.2	V	—
Power dissipation	P_D	1.3	W	(Note2)
Operating temperature	T_{opr}	-20 to 85	°C	—
Storage temperature	T_{stg}	-55 to 150	°C	—
Junction temperature	T_j	150	°C	—

Note1: While in use, please make sure to take the heat generation matter into consideration, and use below 70 % of the absolute maximum ratings ($I_{out(S)}$ ≤ 2.8 A, $I_{out(L)}$ ≤ 5.6 A) as a reference. Operating conditions (such as surrounding temperature or board conditions) may limit the operating current. (Depends on the heat conditions.)

Note2: The value in the state where it is not mounted on the board. Ta exceeding 25 °C would require derating at 10.4 mW/°C.

T_a : Ambient temperature.

T_{opr} : Operating ambient temperature.

T_j : Operating junction temperature. The maximum junction temperature is limited by the thermal shutdown circuit (TSD).
Use the maximum junction temperature (T_j) at 120 °C or less. The maximum current cannot be used under certain thermal conditions.

Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. The TB67H400AFTG does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied. All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

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12. Operating ranges (T_a=-20 to 85 °C)

Table12 Operating ranges

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
VM power supply	V_M	10	24	47	V	—
Motor output current	$I_{out(S)}$	—	1.5	3.0	A	Small mode
	$I_{out(L)}$	—	3.0	6.0	A	Large mode
Logic input voltage	$V_{IN(H)}$	2.0	—	5.5	V	Logic [High] level
	$V_{IN(L)}$	GND	—	0.8	V	Logic [Low] level
Logic input frequency	f_{LOGIC}	—	—	400	kHz	IN1, IN2, PWM
PWM signal frequency	$f_{chop(range)}$	40	70	150	kHz	—
Vref input voltage	V_{ref}	GND	2.0	4.0	V	—

Note: The actual maximum current may be limited by the operating environment (operating conditions such operating duration, or by the surrounding temperature or board heat dissipation). Determine a realistic maximum current by calculating the heat generated under the operating environment.

13. Electrical characteristics

13.1. Electrical characteristics 1 (T_a=25 °C and V_M=24 V, unless otherwise specified)

Table13 Electrical characteristics 1

Characteristics		Symbol	Test conditions	Min	Typ.	Max	Unit
Logic input voltage	High	$V_{IN(H)}$	Logic input pins (Note)	2.0	—	5.5	V
	Low	$V_{IN(L)}$	Logic input pins (Note)	0	—	0.8	V
Logic input hysteresis voltage		$V_{IN(HYS)}$	Logic input pins (Note)	100	—	300	mV
Logic input current	High	$I_{IN(H)}$	Logic input pins:3.3 V	—	33	—	μA
	Low	$I_{IN(L)}$	Logic input pins:0 V	—	—	1	μA
Power consumption		I_{M1}	Output: OPEN, Standby mode	—	2	3.5	mA
		I_{M2}	Output: OPEN, PWM=H, IN1, IN2=Low	—	3.5	5.5	mA
		I_{M3}	Output: OPEN	—	5.5	7	mA
Output leakage current	High	I_{OH}	V_{RS}=V_M=50 V, V_{out}=0 V	—	—	1	μA
	Low	I_{OL}	V_{RS}=V_M=V_{out}=50 V	1	—	—	μA
Output current channel differential		ΔI_{out1}	Bridge A, B differential	-5	0	5	%
Output current accuracy		ΔI_{out2}	I_{out}=1.5 A	-5	0	5	%
RS pin current		I_{RS}	V_{RS}=V_M=24 V	0	—	10	μA
Drain-source ON-resistance (High side + low side)		$R_{on(H+L)}$	T_j=25 °C, Forward direction High side+Low side Small mode	—	0.49	0.6	Ω

Note: $V_{IN(H)}$ is defined as the V_{IN} voltage that causes the outputs (OUTA+, OUTA-, OUTB+ and OUTB-) to change when a pin under test is gradually raised from 0 V. $V_{IN(L)}$ is defined as the V_{IN} voltage that causes the outputs (OUTA+, OUTA-, OUTB+ and OUTB-) to change when the pin is then gradually lowered.
The difference between $V_{IN(H)}$ and $V_{IN(L)}$ is defined as the $V_{IN(HYS)}$.

Note: The internal circuits are designed to avoid miss-function or leakage current; when the logic signal is applied while the V_M voltage is not supplied. But for fail-safe, please control the power supply and logic signal timing correctly.

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13.2. Electrical characteristics 2 (T_a=25 °C and V_M=24 V, unless otherwise specified)

Table13.2 Electrical characteristics 2

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Vref input current	I_{ref}	V_{ref}=2.0 V	—	0	1	μA
Internal regulator voltage	V_{CC}	I_{CC}=5.0 mA	4.75	5.0	5.25	V
Internal regulator current	I_{CC}	V_{CC}=5.0 V	—	2.5	5	mA
Vref gain rate	$V_{ref(gain)}$	V_{ref}=2.0 V	1/5.2	1/5.0	1/4.8	—
TSD threshold (Note1)	T_{jTSD}	—	145	160	175	°C
VM power on reset voltage	V_{MR}	—	7.0	8.0	9.0	V
Over current threshold (Note2)	I_{SD}	—	4.1	4.9	5.7	A

Note1: Thermal shutdown (TSD) circuit
When the junction temperature of the device reaches the TSD threshold, the TSD circuit is triggered; the internal reset circuit then turns off the output transistors. In order to avoid malfunction by switching etc., detection mask time is prepared inside IC. Once the TSD circuit is triggered, the device will be set to standby mode, and can be cleared by reasserting the VM power source, or setting to standby mode (INA1, INA2, INB1, INB2, PWMA, and PWMB=All Low). The TSD circuit is a backup function to detect a thermal error, therefore is not recommended to be used aggressively.

Note2: Over-current shutdown (ISD) circuit
When the output current reaches the threshold, the ISD circuit is triggered; the internal reset circuit then turns off the output transistors. In order to avoid malfunction by switching etc., detection mask time is prepared inside IC. Once the ISD circuit is triggered, the device will be set to standby mode, and can be cleared by reasserting the VM power source, or setting to standby mode (INA1, INA2, INB1, INB2, PWMA, and PWMB=All Low).

13.2.1. Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.
If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the TB67H400AFTG or other components will be damaged or fail due to the motor back-EMF.

13.2.2. Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.

If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.

The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

13.2.3. IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

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14. AC electrical characteristics (T_a = 25 °C, V_M = 24 V, and 6.8 mH/5.7 Ω, unless otherwise specified)

Table14 AC electrical characteristics

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Minimum phase pulse width	t_{LOGIC}	—	100	—	—	ns
	t_{wp}	—	50	—	—	
	t_{wn}	—	50	—	—	
Output transistor switching characteristics	t_r	—	30	80	130	ns
	t_f	—	40	90	140	
	$t_{pLH(LOGIC)}$	IN1, IN2, PWM - OUT	250	—	1200	
	$t_{pHL(LOGIC)}$	IN1, IN2, PWM - OUT	250	—	1200	
Analog blanking time	At_{BLK}	V_M=24 V, I_{out}=1.5 A Analog t_{BLK}	250	400	550	ns
Digital blanking time	$Dt_{BLK(L)}$	TBLKAB:L, f_{OSCM}=1120 kHz	—	3.6	—	μs
	$Dt_{BLK(H)}$	TBLKAB:H, f_{OSCM}=1120 kHz	—	5.4	—	μs
OSCM oscillation frequency accuracy	Δf_{OSCM}	C_{OSC}= 270 pF, R_{OSC} =5.1 kΩ	-15	—	+15	%
OSC oscillation reference frequency	f_{OSCM}	C_{OSC}= 270 pF, R_{OSC} =5.1 kΩ	952	1120	1288	kHz
Chopping frequency	f_{chop}	Output: Active(I_{out}=1.5 A), f_{OSCM} = 1120 kHz	—	70	—	kHz

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15. AC characteristics timing chart

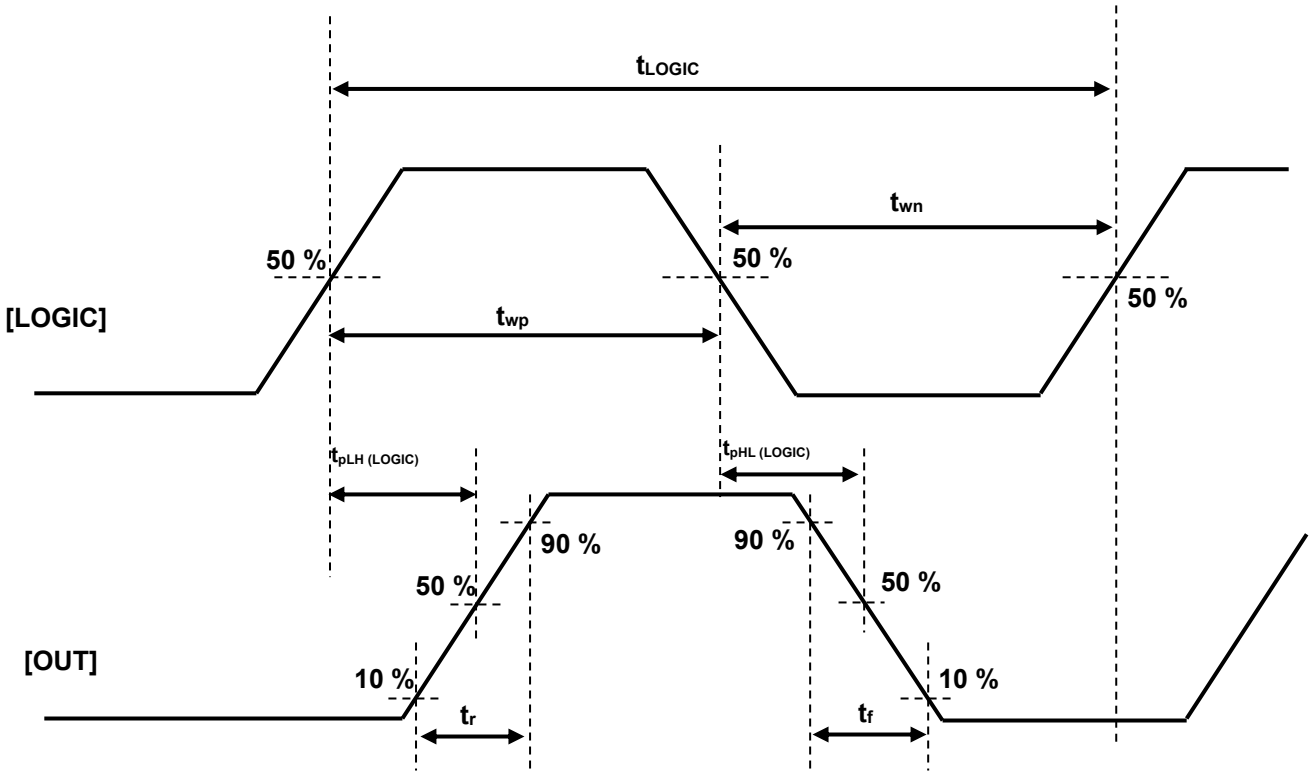

Figure15 AC characteristics timing chart

Note: Please note that the timing charts or constants may be omitted or simplified for explanatory.

16. P_D-Ta graph (for reference)

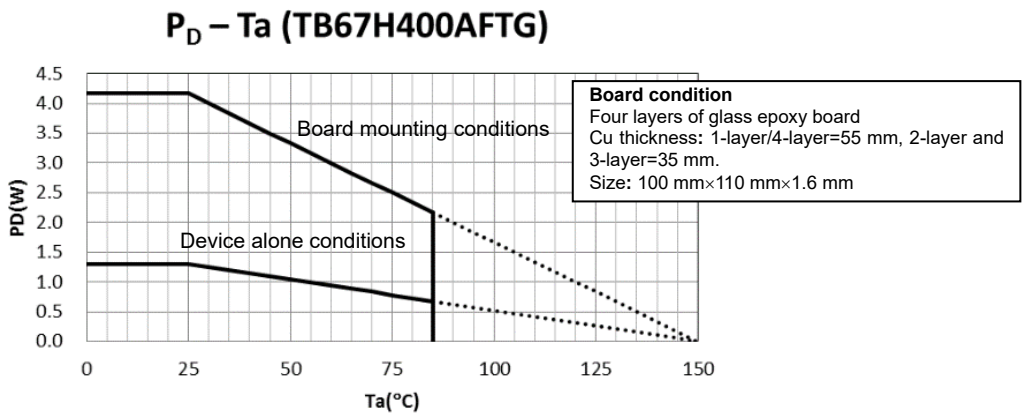

Figure16 P_D-Ta graph

This value is dependent on a substrate pattern and mounting conditions. Moreover, when ambient temperature is high, permissible power consumption becomes small.

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17. Package dimensions

P-WQFN48-0707-0.50-003

Unit: mm

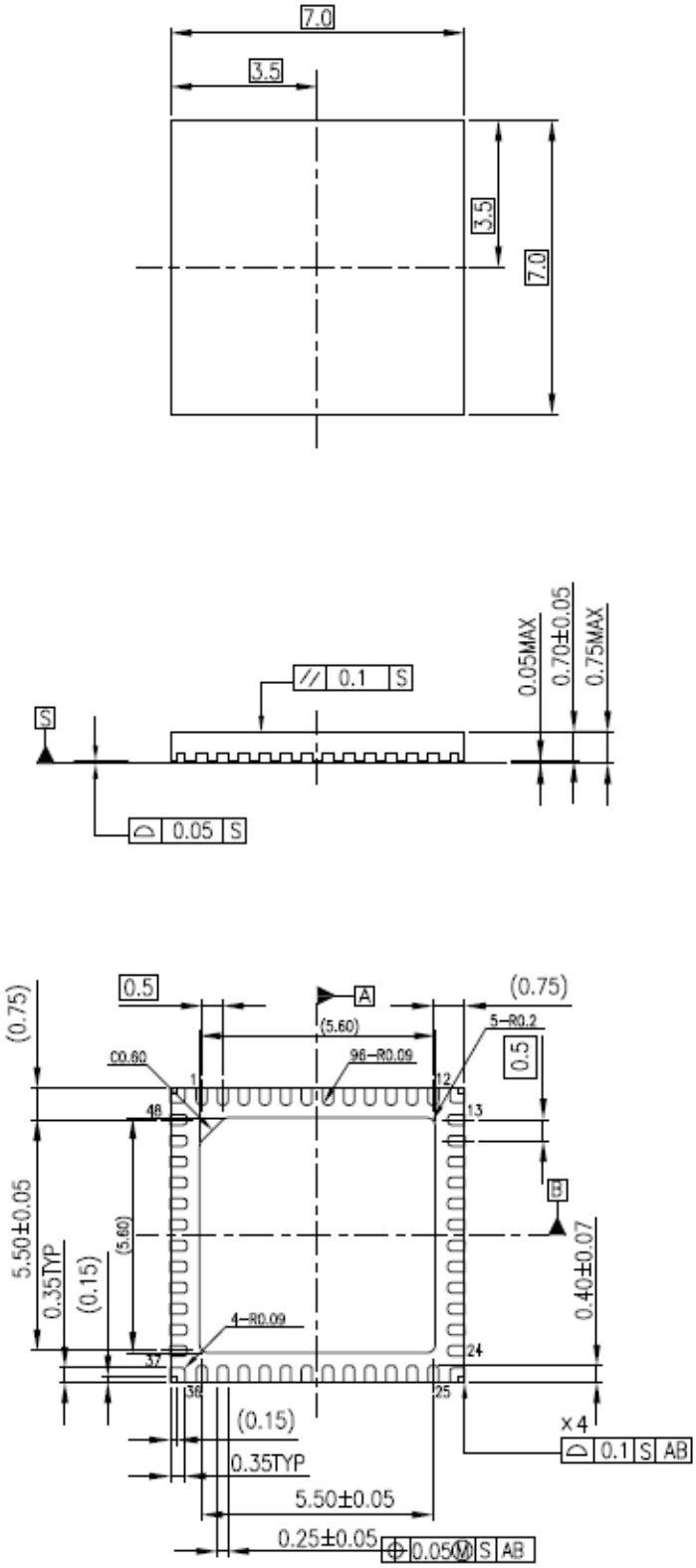

Figure17 Package Dimensions

Weight 0.10 g (Typ.)

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18. Notes on Contents

Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Timing Charts

Timing charts may be simplified for explanatory purposes.

Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

19. IC Usage Considerations

19.1. Notes on handling of ICs

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. In addition, do not use any device that has been inserted incorrectly.

Please take extra care when selecting external components (such as power amps and regulators) or external devices (for instance, speakers). When large amounts of leak current occur from capacitors, the DC output level may increase. If the output is connected to devices such as speakers with low resist voltage, overcurrent or IC failure may cause smoke or ignition. (The over-current may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

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19.2. Points to remember on handling of ICs

(1) Over current detection circuit

Over current detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current detection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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