

MOSFETs Silicon N-channel MOS (U-MOS X-H)

# TPH1100CQ5

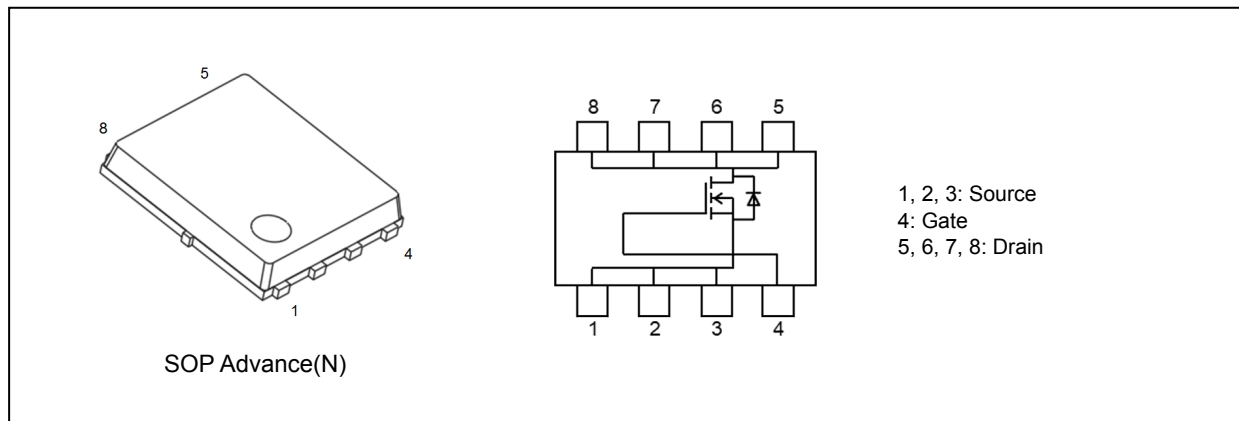
## 1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- Motor Drivers

## 2. Features

- (1) Fast reverse recovery time :  $t_{rr} = 38 \text{ ns}$  (typ.)
- (2) Small reverse recovery charge :  $Q_{rr} = 32 \text{ nC}$  (typ.)
- (3) Small gate charge:  $Q_{SW} = 9.9 \text{ nC}$  (typ.)
- (4) Low drain-source on-resistance:  $R_{DS(ON)} = 9 \text{ m}\Omega$  (typ.) ( $V_{GS} = 10 \text{ V}$ )
- (5) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = 150 \text{ V}$ )
- (6) Enhancement mode:  $V_{th} = 3.1 \text{ to } 4.5 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 0.8 \text{ mA}$ )

## 3. Packaging and Internal Circuit



Start of commercial production  
2024-03

## 4. Absolute Maximum Ratings (Note) ( $T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

| Characteristics                                                    | Symbol    | Rating     | Unit               |
|--------------------------------------------------------------------|-----------|------------|--------------------|
| Drain-source voltage                                               | $V_{DS}$  | 150        | V                  |
| Gate-source voltage                                                | $V_{GS}$  | $\pm 20$   |                    |
| Drain current (DC) ( $T_c = 25\text{ }^{\circ}\text{C}$ ) (Note 1) | $I_D$     | 49         | A                  |
| Drain current (DC) (Silicon limit) (Note 1), (Note 2)              | $I_D$     | 90         |                    |
| Drain current (pulsed) ( $t = 100\text{ }\mu\text{s}$ ) (Note 1)   | $I_{DP}$  | 220        |                    |
| Power dissipation ( $T_c = 25\text{ }^{\circ}\text{C}$ )           | $P_D$     | 180        | W                  |
| Power dissipation (Note 3)                                         | $P_D$     | 3          |                    |
| Power dissipation (Note 4)                                         | $P_D$     | 0.96       |                    |
| Single-pulse avalanche energy (Note 5)                             | $E_{AS}$  | 159        | mJ                 |
| Single-pulse avalanche current (Note 5)                            | $I_{AS}$  | 49         | A                  |
| Channel temperature                                                | $T_{ch}$  | 175        | $^{\circ}\text{C}$ |
| Storage temperature                                                | $T_{stg}$ | -55 to 175 |                    |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note: This product is not designed for radiation resistance or cosmic ray resistance, and these natural environmental factors may affect reliability.

In addition, radiation from the constituent materials of the product also becomes a natural environmental factor, which may affect reliability.

## 5. Thermal Characteristics

| Characteristics                                                                       | Symbol         | Max | Unit                 |
|---------------------------------------------------------------------------------------|----------------|-----|----------------------|
| Channel-to-case thermal resistance ( $T_c = 25\text{ }^{\circ}\text{C}$ )             | $R_{th(ch-c)}$ | 0.8 | $^{\circ}\text{C/W}$ |
| Channel-to-ambient thermal resistance ( $T_a = 25\text{ }^{\circ}\text{C}$ ) (Note 3) | $R_{th(ch-a)}$ | 50  |                      |
| Channel-to-ambient thermal resistance ( $T_a = 25\text{ }^{\circ}\text{C}$ ) (Note 4) | $R_{th(ch-a)}$ | 156 |                      |

Note 1: Ensure that the channel temperature does not exceed  $175\text{ }^{\circ}\text{C}$ .

Note 2: Limited by silicon chip capability.

Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5:  $V_{DD} = 120\text{ V}$ ,  $T_{ch} = 25\text{ }^{\circ}\text{C}$  (initial),  $L = 51\text{ }\mu\text{H}$ ,  $I_{AS} = 49\text{ A}$

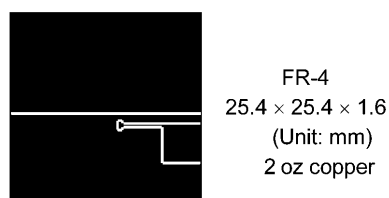


Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

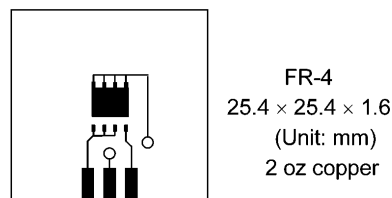


Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

## 6. Electrical Characteristics

### 6.1. Static Characteristics ( $T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

| Characteristics                         | Symbol        | Test Condition                                     | Min | Typ. | Max       | Unit             |
|-----------------------------------------|---------------|----------------------------------------------------|-----|------|-----------|------------------|
| Gate leakage current                    | $I_{GSS}$     | $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$ | —   | —    | $\pm 0.1$ | $\mu\text{A}$    |
| Drain cut-off current                   | $I_{DSS}$     | $V_{DS} = 150\text{ V}$ , $V_{GS} = 0\text{ V}$    | —   | —    | 10        |                  |
| Drain-source breakdown voltage          | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}$ , $V_{GS} = 0\text{ V}$       | 150 | —    | —         | V                |
| Drain-source breakdown voltage (Note 6) | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}$ , $V_{GS} = -20\text{ V}$     | 130 | —    | —         |                  |
| Gate threshold voltage                  | $V_{th}$      | $V_{DS} = 10\text{ V}$ , $I_D = 0.8\text{ mA}$     | 3.1 | —    | 4.5       |                  |
| Drain-source on-resistance              | $R_{DS(ON)}$  | $V_{GS} = 8\text{ V}$ , $I_D = 21\text{ A}$        | —   | 9.7  | 13.6      | $\text{m}\Omega$ |
|                                         |               | $V_{GS} = 10\text{ V}$ , $I_D = 24.5\text{ A}$     | —   | 9    | 11.1      |                  |

Note 6: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

### 6.2. Dynamic Characteristics ( $T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

| Characteristics                | Symbol    | Test Condition                                                      | Min | Typ. | Max  | Unit        |
|--------------------------------|-----------|---------------------------------------------------------------------|-----|------|------|-------------|
| Input capacitance              | $C_{iss}$ | $V_{DS} = 75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ | —   | 2830 | 4400 | $\text{pF}$ |
| Reverse transfer capacitance   | $C_{rss}$ |                                                                     | —   | 15   | 50   |             |
| Output capacitance             | $C_{oss}$ |                                                                     | —   | 560  | —    |             |
| Gate resistance                | $r_g$     | —                                                                   | —   | 1.5  | 2.3  | $\Omega$    |
| Switching time (rise time)     | $t_r$     | See Figure 6.2.1                                                    | —   | 13   | —    | ns          |
| Switching time (turn-on time)  | $t_{on}$  |                                                                     | —   | 33   | —    |             |
| Switching time (fall time)     | $t_f$     |                                                                     | —   | 14   | —    |             |
| Switching time (turn-off time) | $t_{off}$ |                                                                     | —   | 40   | —    |             |

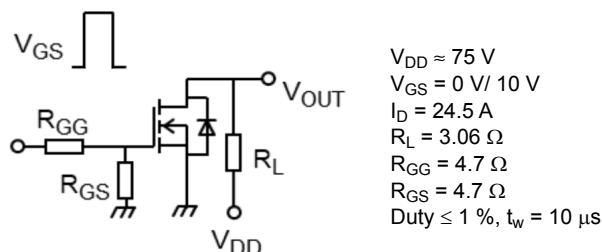


Fig. 6.2.1 Switching Time Test Circuit

### 6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

| Characteristics                                 | Symbol    | Test Condition                                                                | Min | Typ. | Max | Unit        |
|-------------------------------------------------|-----------|-------------------------------------------------------------------------------|-----|------|-----|-------------|
| Total gate charge (gate-source plus gate-drain) | $Q_g$     | $V_{DD} \approx 75\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 24.5\text{ A}$ | —   | 38   | —   | $\text{nC}$ |
|                                                 |           | $V_{DD} \approx 75\text{ V}$ , $V_{GS} = 8\text{ V}$ , $I_D = 21\text{ A}$    | —   | 31   | —   |             |
| Gate-source charge 1                            | $Q_{gs1}$ | $V_{DD} \approx 75\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 24.5\text{ A}$ | —   | 16.6 | —   |             |
| Gate-drain charge                               | $Q_{gd}$  |                                                                               | —   | 4.9  | —   |             |
| Gate switch charge                              | $Q_{SW}$  |                                                                               | —   | 9.9  | —   |             |
| Output charge                                   | $Q_{oss}$ | $V_{DS} = 75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$           | —   | 70   | —   |             |

6.4. Source-Drain Characteristics (T<sub>a</sub> = 25 °C unless otherwise specified)

| Characteristics                         | Symbol           | Test Condition                                                                       | Min | Typ. | Max  | Unit |
|-----------------------------------------|------------------|--------------------------------------------------------------------------------------|-----|------|------|------|
| Reverse drain current (pulsed) (Note 7) | I <sub>DRP</sub> | (t = 100 μs)                                                                         | —   | —    | 220  | A    |
| Diode forward voltage                   | V <sub>DSF</sub> | I <sub>DR</sub> = 24.5 A, V <sub>GS</sub> = 0 V                                      | —   | —    | -1.2 | V    |
| Reverse recovery time (Note 8)          | t <sub>rr</sub>  | I <sub>DR</sub> = 12.3 A, V <sub>GS</sub> = 0 V,<br>-dI <sub>DR</sub> /dt = 100 A/μs | —   | 38   | 57   | ns   |
| Reverse recovery charge (Note 8)        | Q <sub>rr</sub>  |                                                                                      | —   | 32   | 75   | nC   |

Note 7: Ensure that the channel temperature does not exceed 175 °C.

Note 8: Defined by design.

7. Marking

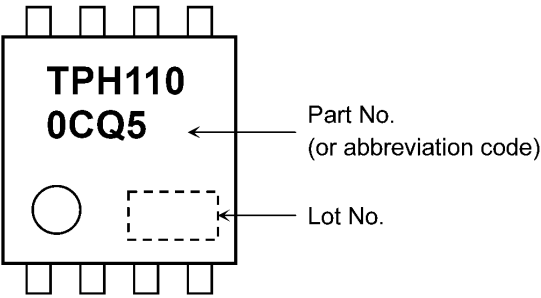


Fig. 7.1 Marking

8. Characteristics Curves (Note)

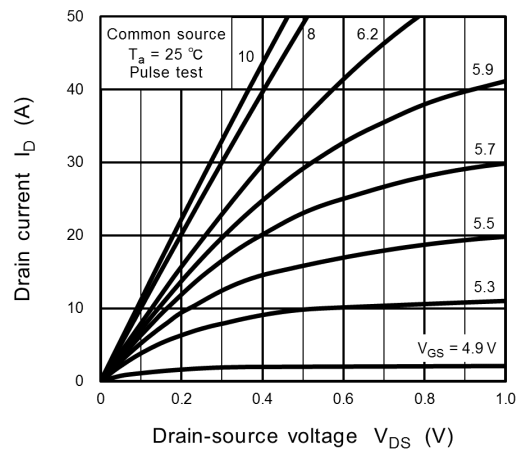


Fig. 8.1  $I_D - V_{DS}$

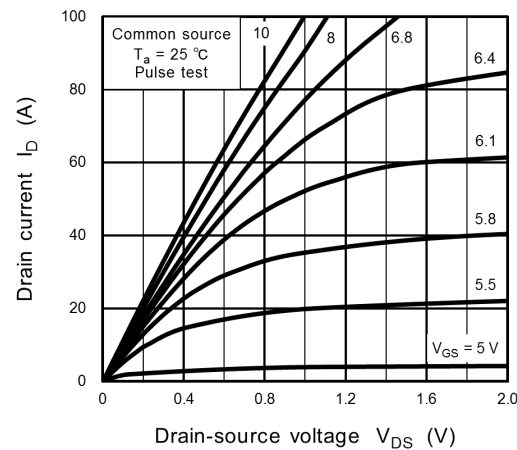


Fig. 8.2  $I_D - V_{DS}$

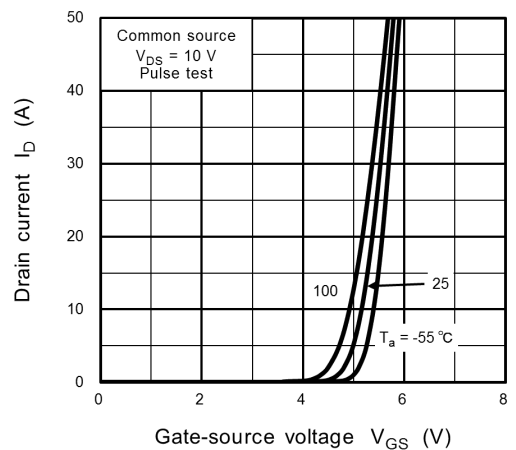


Fig. 8.3  $I_D - V_{GS}$

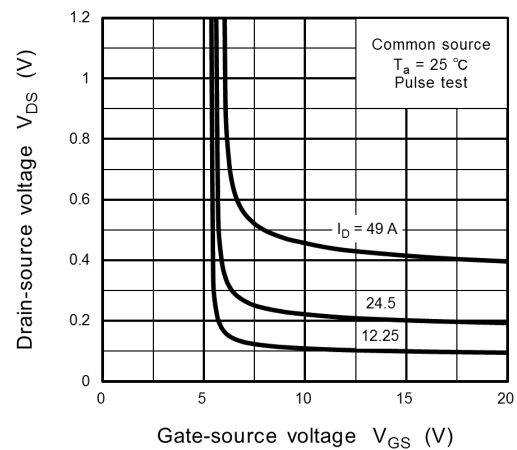


Fig. 8.4  $V_{DS} - V_{GS}$

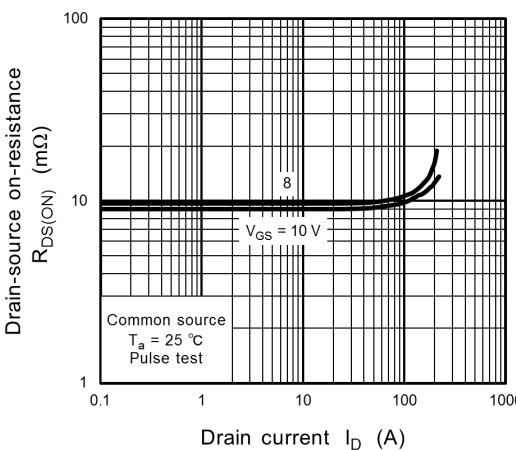


Fig. 8.5  $R_{DS(ON)} - I_D$

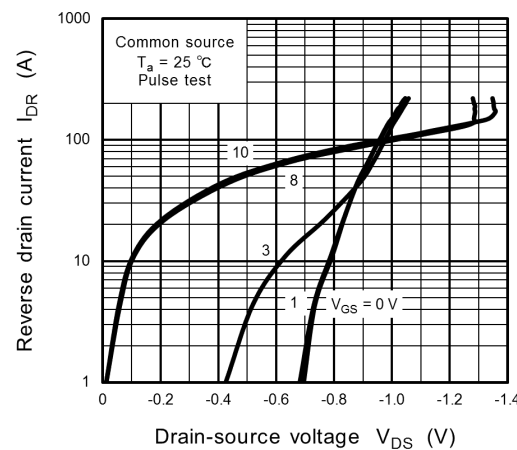


Fig. 8.6  $I_{DR} - V_{DS}$

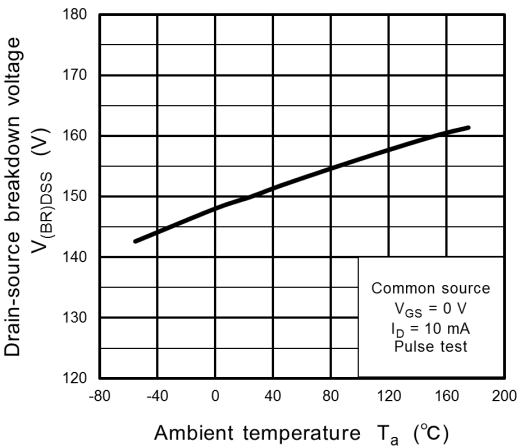


Fig. 8.7  $V_{(BR)DSS} - T_a$

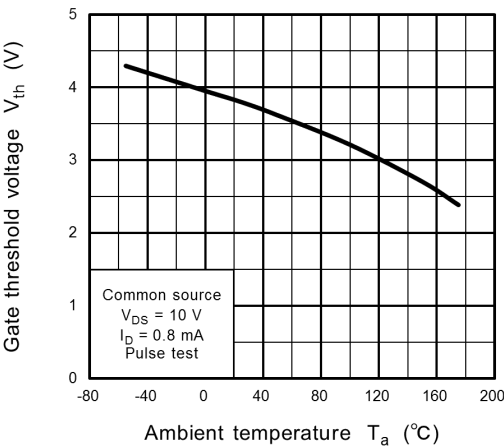


Fig. 8.8  $V_{th} - T_a$

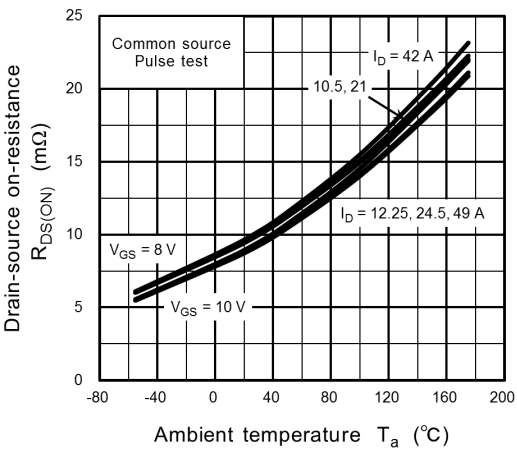


Fig. 8.9  $R_{DS(ON)} - T_a$

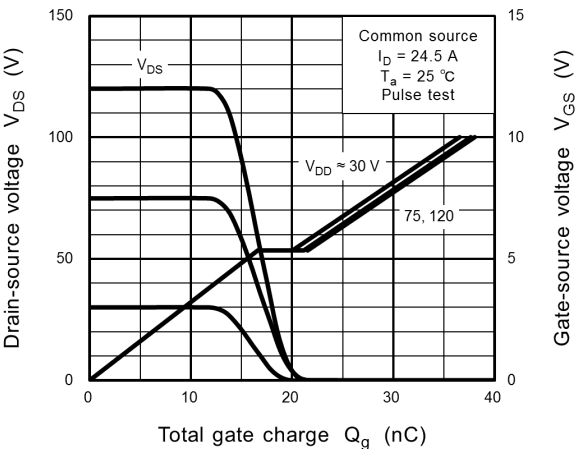


Fig. 8.10 Dynamic Input/Output Characteristics

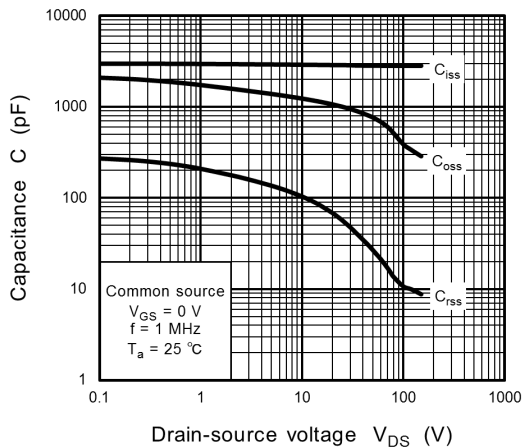


Fig. 8.11 Capacitance -  $V_{DS}$

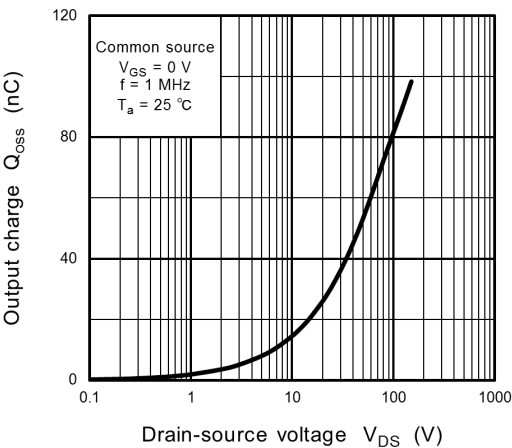


Fig. 8.12  $Q_{oss} - V_{DS}$

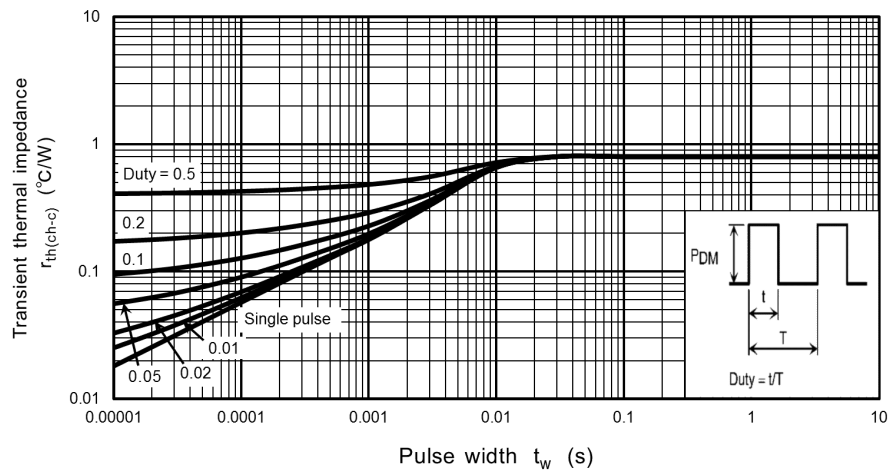


Fig. 8.13  $r_{th} - t_w$   
(Guaranteed Maximum)

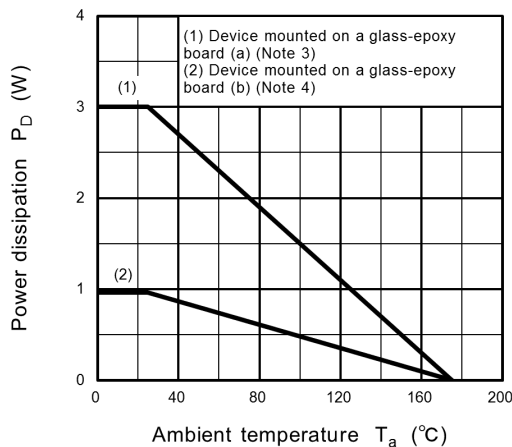


Fig. 8.14  $P_D - T_a$   
(Guaranteed Maximum)

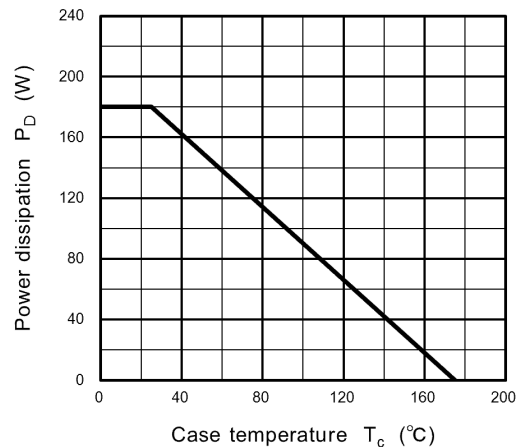


Fig. 8.15  $P_D - T_c$   
(Guaranteed Maximum)

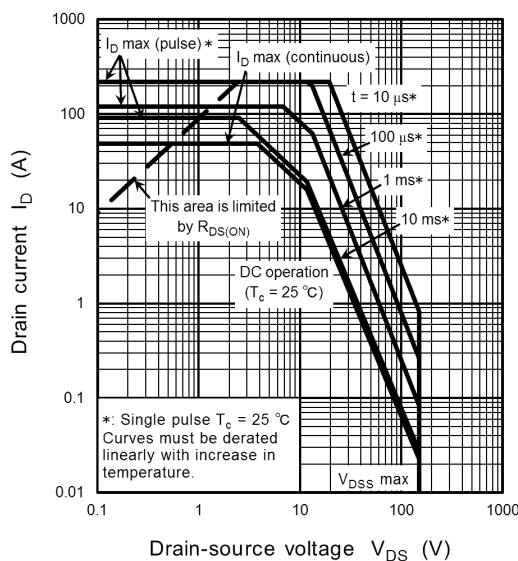
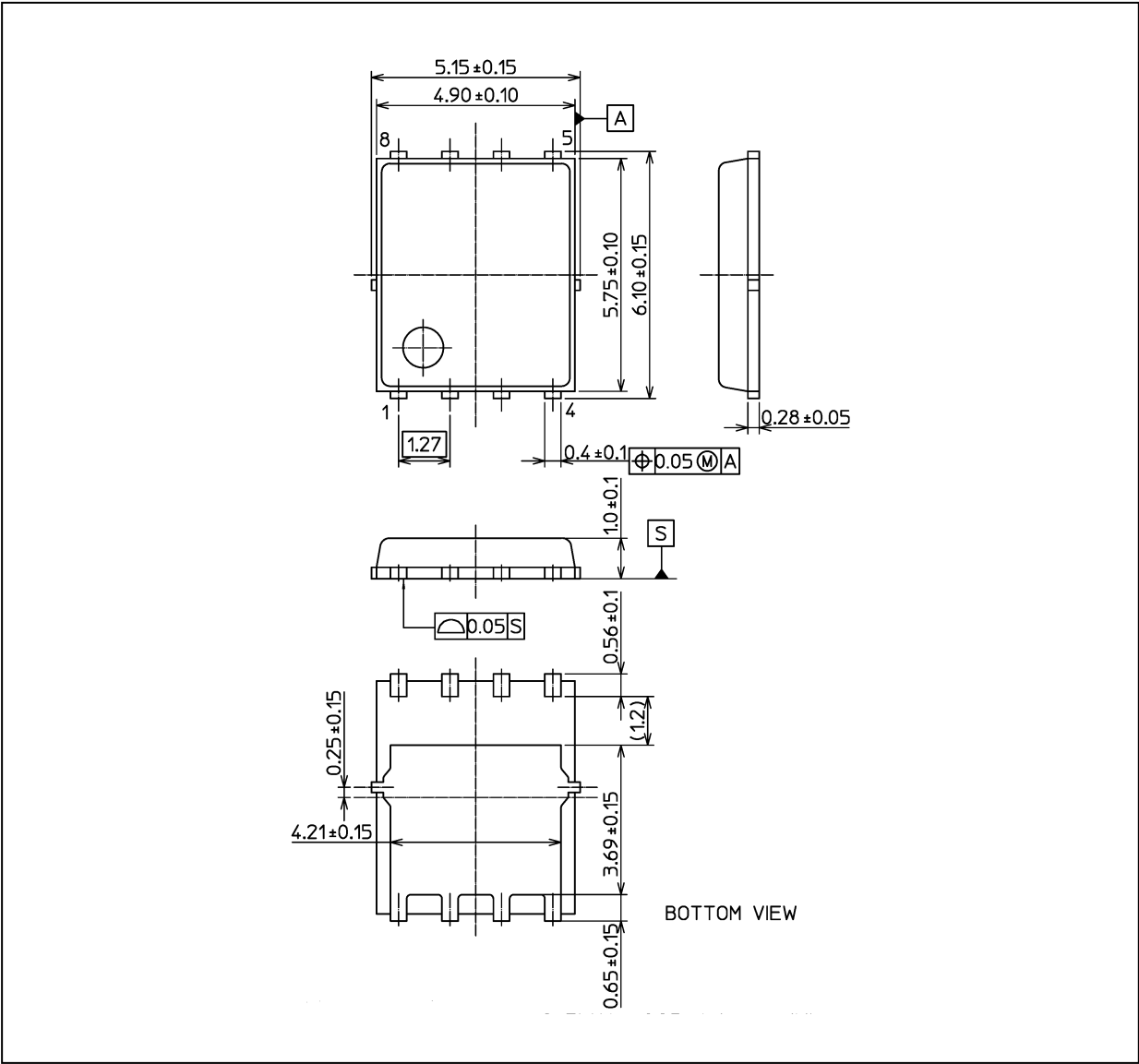


Fig. 8.16 Safe Operating Area  
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.108 g (typ.)

| Package Name(s)          |
|--------------------------|
| TOSHIBA: 2-5W1A          |
| Nickname: SOP Advance(N) |

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