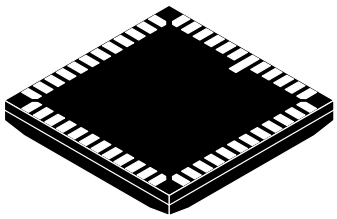
1/2.5-Inch 5 Mp CMOS Digital Image Sensor

MT9P001



ILCC48 10x10
CASE 847AA

The 5 Mp CMOS image sensor features **onsemi**'s breakthrough low−noise CMOS imaging technology that achieves CCD image quality (based on signal−to−noise ratio and low−light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The **onsemi** MT9P001 is a 1/2.5−inch CMOS active−pixel digital image sensor with an active imaging pixel array of 2592 H x 1944 V. It incorporates sophisticated camera functions on−chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two−wire serial interface.

Table 1. KEY PERFORMANCE PARAMETERS

Parameter		Value
Optical Format		1/2.5−inch (4:3)
Active Imager Size		5.70 mm (H) x 4.28 mm (V) 7.13 mm Diagonal
Active Pixels		2592 H x 1944 V
Pixel Size		2.2 x 2.2 μm
Color Filter Array		RGB Bayer Pattern
Shutter Type		Global Reset Release (GRR), Snapshot Only Electronic Rolling Shutter (ERS)
Maximum Data Rate / Master Clock		96 Mp/s at 96 MHz (2.8 V I/O) 48 Mp/s at 48 MHz (1.8 V I/O)
Frame Rate	Full Resolution	Programmable up to 15 fps
	VGA (640 x 480, with Binning)	Programmable up to 70 fps
ADC Resolution		12−bit, On−chip
Responsivity		1.4 V/lux−sec (550nm)
Pixel Dynamic Range		70.1 dB
SNR_{MAX}		38.1 dB
Supply Voltage	I/O	1.7−3.1 V
	Digital	1.7−1.9 V (1.8 V Nominal)
	Analog	2.6−3.1 V (2.8 V Nominal)
Power Consumption		381 mW at 15 fps Full Resolution
Operating Temperature		−30°C to +70°C
Packaging		48−pin iLCC, Die

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

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Features

- High Frame Rate
- Superior Low−light Performance
- Low Dark Current
- Global Reset Release, which Starts the Exposure of All Rows Simultaneously
- Bulb Exposure Mode, for Arbitrary Exposure Times
- Snapshot Mode to Take Frames on Demand
- Horizontal and Vertical Mirror Image
- Column and Row Skip Modes to Reduce Image Size without Reducing Field−of−view (FOV)
- Column and Row Binning Modes to Improve Image Quality when Resizing
- Simple Two−wire Serial Interface
- Programmable Controls: Gain, Frame Rate, Frame Size, Exposure
- Automatic Black Level Calibration
- On−chip Phase−Locked Loop (PLL)

Applications

- Digital Still Cameras
- Digital Video Cameras
- PC Cameras
- Converged DSCs/Camcorders
- Cellular Phones
- PDAs

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ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
MT9P001I12STC−B−DR	5 MP 1/2.5” CIS	Dry Pack without Protective Film

DISCONTINUED (Note 1)

MT9P001I12−N4005−DR	5 MP 1/2.5” CIS	Dry Pack without Protective Film

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

DESCRIPTION

The MT9P001 sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a full resolution image at 15 frames per second (fps).

An on−chip analog−to−digital converter (ADC) provides 12 bits per pixel. FRAME_VALID (FV) and LINE_VALID (LV) signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

The MT9P001 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of consumer and industrial applications, including cell phones, digital still cameras, and digital video cameras, and PC cameras.

FUNCTIONAL OVERVIEW

The MT9P001 is a progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase−locked loop (PLL) to generate all internal clocks from a single master input clock running between 6 and 27 MHz. The maximum pixel rate is 96 Mp/s, corresponding to a clock rate of 96 MHz. Figure 1 illustrates a block diagram of the sensor.

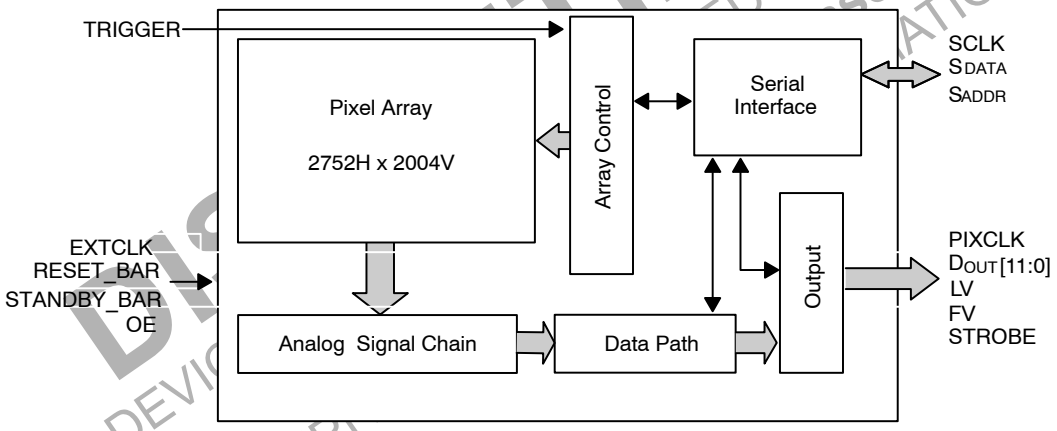


Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 5 Mp active−pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an ADC. The output from the ADC is a 12−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 96 Mp/s, in addition to frame and line synchronization signals.

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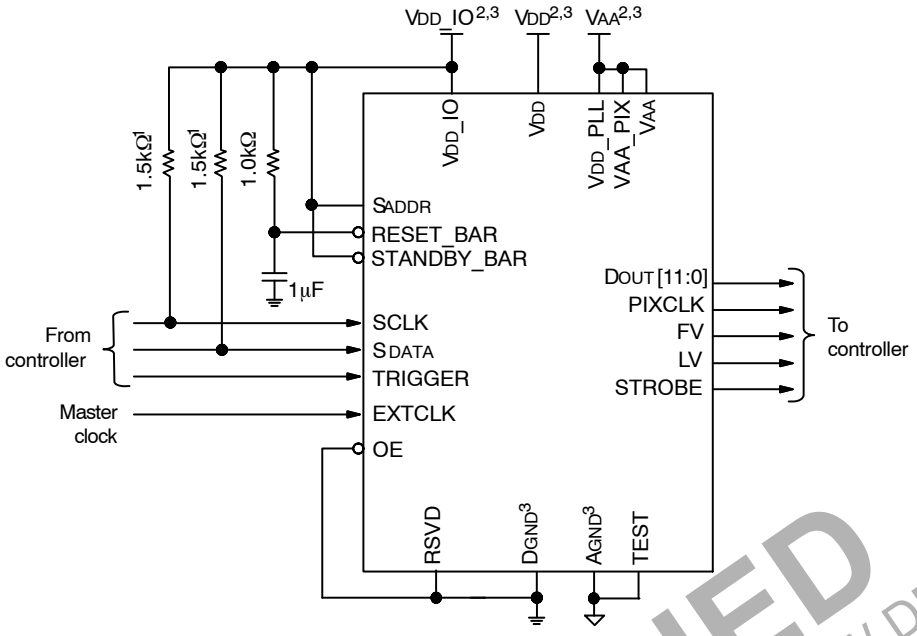


Figure 2. Typical Configuration (Connection)

1. A resistor value of 1.5 kΩ is recommended, but may be greater for slower two−wire speed.
2. All power supplies should be adequately decoupled.
3. All DGND pins must be tied together, as must all AGND pins, all VDD_IO pins, and all VDD pins.

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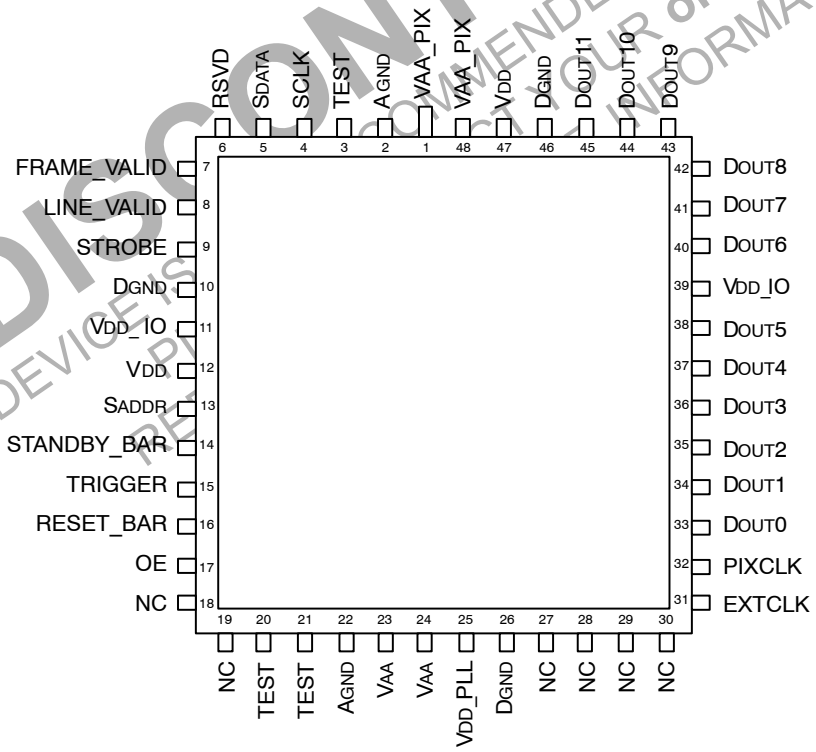


Figure 3. 48−Pin iLCC 10 x 10 Package Pinout Diagram (Top View)

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Table 3. PIN DESCRIPTION

Name	Type	Description
RESET_BAR	Input	When LOW, the MT9P001 asynchronously resets. When driven HIGH, it resumes normal operation with all configuration registers set to factory defaults.
EXTCLK	Input	External input clock.
SCLK	Input	Serial clock. Pull to VDD_IO with a 1.5 kΩ resistor.
OE	Input	When HIGH, the PIXCLK, DOUT, FV, LV, and STROBE outputs enter a High−Z. When driven LOW, normal operation resumes.
STANDBY_BAR	Input	Standby. When LOW, the chip enters a low−power standby mode. It resumes normal operation when the pin is driven HIGH.
TRIGGER	Input	Snapshot trigger. Used to trigger one frame of output in snapshot modes, and to indicate the end of exposure in bulb exposure modes.
SADDR	Input	Serial address. When HIGH, the MT9P001 responds to device ID $(BA)_H$. When LOW, it responds to serial device ID $(90)_H$.
SDATA	I/O	Serial data. Pull to VDD_IO with a 1.5 kΩ resistor.
PIXCLK	Output	Pixel clock. The DOUT, FV, LV, and STROBE outputs should be captured on the falling edge of this signal.
DOUT[11:0]	Output	Pixel data. Pixel data is 12−bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
FRAME_VALID	Output	Frame valid. Driven HIGH during active pixels and horizontal blanking of each frame and LOW during vertical blanking.
LINE_VALID	Output	Line valid. Driven HIGH with active pixels of each line and LOW during blanking periods.
STROBE	Output	Snapshot strobe. Driven HIGH when all pixels are exposing in snapshot modes.
VDD	Supply	Digital supply voltage. Nominally 1.8 V.
VDD_IO	Supply	IO supply voltage. Nominally 1.8 or 2.8 V.
DGND	Supply	Digital ground.
VAA	Supply	Analog supply voltage. Nominally 2.8 V.
VAA_PIX	Supply	Pixel supply voltage. Nominally 2.8 V, connected externally to VAA.
AGND	Supply	Analog ground.
VDD_PLL	Supply	PLL supply voltage. Nominally 2.8 V, connected externally to VAA.
TEST	–	Tie to AGND for normal device operation (factory use only).
RSVD	–	Tie to DGND for normal device operation (factory use only).
NC	–	No connect.

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PIXEL DATA FORMAT

Pixel Array Structure

The MT9P001 pixel array consists of a 2752−column by 2004−row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper−right corner of the entire array, looking at the sensor, as shown in Figure 4.

The array consists of a 2592−column by 1944−row active region in the center representing the default output image, surrounded by a boundary region (also active), surrounded by a border of dark pixels (see Tables 4 and 5). The boundary region can be used to avoid edge effects when doing color processing to achieve a 2592 x 1944 result image, while the optically black column and rows can be used to monitor the black level.

Pixels are output in a Bayer pattern format consisting of four “colors”−GreenR, GreenB, Red, and Blue (Gr, Gb, R, B)−representing three filter colors. When no mirror modes are enabled, the first row output alternates between Gr and R pixels, and the second row output alternates between B and Gb pixels. The Gr and Gb pixels have the same color filter, but they are treated as separate colors by the data path and analog signal chain.

Table 4. PIXEL TYPE BY COLUMN

Column	Pixel Type
0–9	Dark (10)
10–15	Active boundary (6)
16–2607	Active image (2592)
2608–2617	Active boundary (10)
2618–2751	Dark (134)

Table 5. PIXEL TYPE BY ROW

Column	Pixel Type
0– 49	Dark (50)
50–53	Active boundary (4)
54–1997	Active image (1944)
1998–2001	Active boundary (3)
2002–2003	Dark (2)

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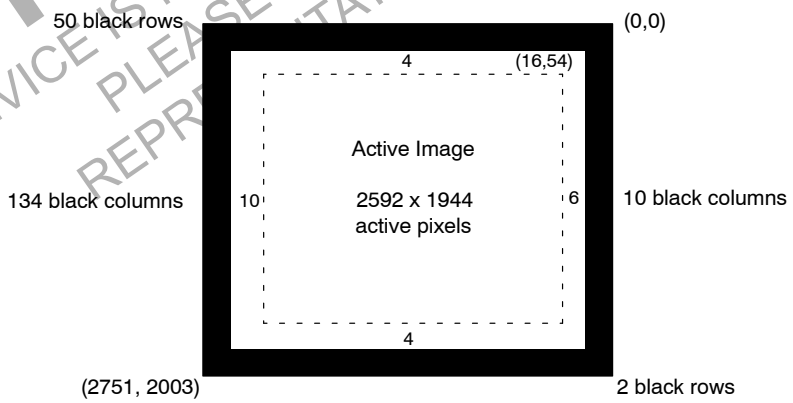


Figure 4. Pixel Array Description

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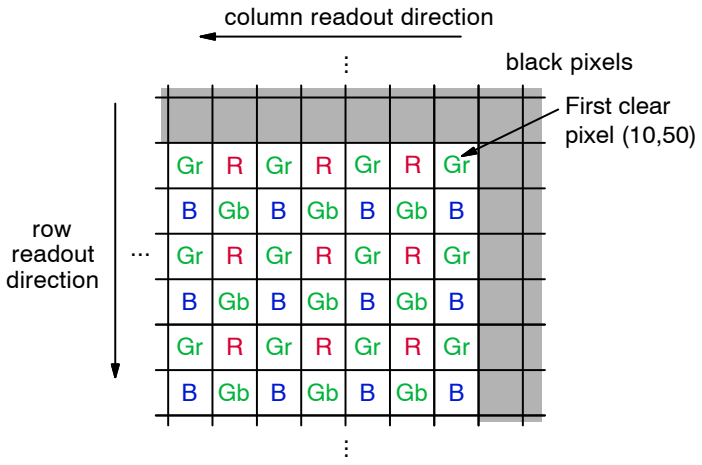


Figure 5. Pixel Color Pattern Detail (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 4). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (16, 54).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 6. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 6.

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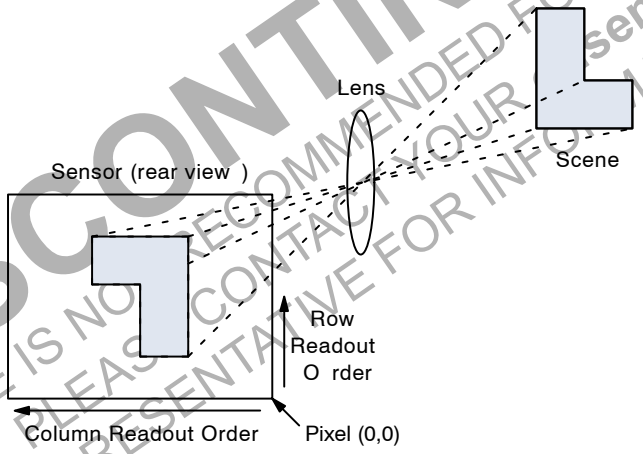


Figure 6. Imaging a Scene

Output Data Format (Default Mode)

The MT9P001 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 7. LV is HIGH during the shaded region of the figure. FV timing is described in “Output Data Timing”.

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$P_{0,0}$ $P_{0,1}$ $P_{0,2}$ ..... $P_{0,n-1}$ $P_{0,n}$ $P_{1,0}$ $P_{1,1}$ $P_{1,2}$ ..... $P_{1,n-1}$ $P_{1,n}$ VALID IMAGE $P_{m-1,0}$ $P_{m-1,1}$ ..... $P_{m-1,n-1}$ $P_{m-1,n}$ $P_{m,0}$ $P_{m,1}$ ..... $P_{m,n-1}$ $P_{m,n}$	00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 HORIZONTAL BLANKING 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00
00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 VERTICAL BLANKING 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00	00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00 VERTICAL/HORIZONTAL BLANKING 00 00 00 ..... 00 00 00 00 00 00 ..... 00 00 00

Figure 7. Spatial Illustration of Image Readout

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Readout Sequence

Typically, the readout window is set to a region including only active pixels. The user has the option of reading out dark regions of the array, but if this is done, consideration must be given to how the sensor reads the dark regions for its own purposes.

Row Readout

Rows are read from the array in the following order:

1. Dark rows:
   If Show_Dark_Rows is set, or if Manual_BLC is clear, dark rows on the top of the array are read out. The set of rows sampled are adjusted based on the Row_Bin setting such that there are eight rows after binning, as shown in the Table 6. The Row_Skip setting is ignored for the dark row region.
   If Show_Dark_Rows is clear and Manual_BLC is set, no dark rows are read from the array as part of this step, allowing all rows to be part of the active image. This does not change the frame time, as H_{DR} is included in the vertical blank period.
2. Active image:
   The rows defined by the row start, row size, bin, skip, and row mirror settings are read out. If this set of rows includes rows read out above, those rows are re−sampled, meaning that the data is invalid.

Table 6. DARK ROWS SAMPLED AS A FUNCTION OF ROW_BIN

Row_Bin	H_{DR} (Dark Rows After Binning)
0	8
1	8
3	8

Column Readout

Columns are read out in the following order:

1. Dark columns: If either Show_Dark_Columns or Row_BLC is set, dark columns on the left side of the image are read out followed by those on the right side. The set of columns read is shown in Table 7. The Column_Skip setting is ignored for the dark columns.
   If neither Show_Dark_Columns nor Row_BLC is set, no dark columns are read, allowing all columns to be part of the active image. This does not change the row time, as W_{DC} is included in the vertical blank period.
2. Active image: The columns defined by column start, column size, bin, skip, and column mirror settings are read out. If this set of columns includes the columns read out above, these columns are resampled, meaning the data is invalid.

Table 7. DARK COLUMNS SAMPLED AS A FUNCTION OF COLUMN_BIN

Column_Bin	W_{DC} (Dark Columns After Binning)
0	80
1	40
3	20

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OUTPUT DATA TIMING

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 1944 rows of 2592 columns each. The FV and LV signals indicate the boundaries between frames and lines, respectively. PIXCLK can be used as a clock to latch the data. For each PIXCLK cycle, one 12−bit pixel datum outputs on the DOUT pins. When both FV and LV are asserted, the pixel is valid. PIXCLK cycles that occur when FV is negated are called vertical blanking. PIXCLK cycles that occur when only LV is negated are called horizontal blanking.

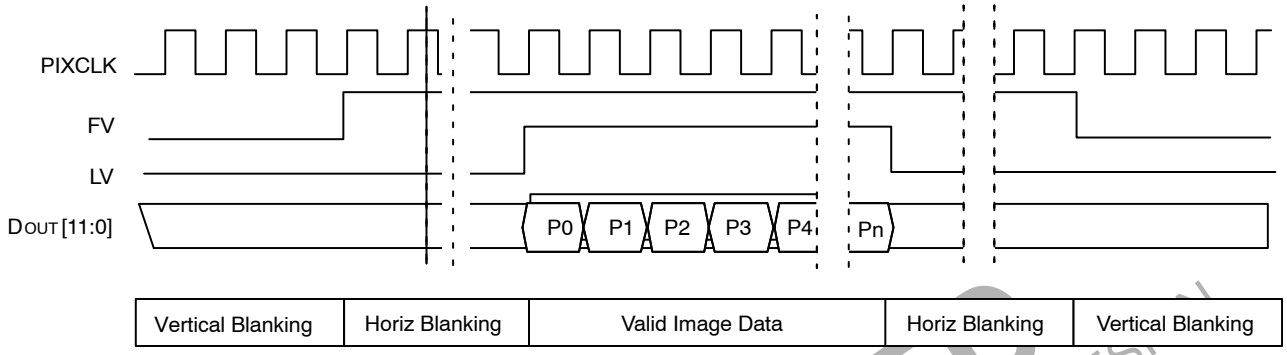


Figure 8. Default Pixel Output Timing

LV and FV

The timing of the FV and LV outputs is closely related to the row time and the frame time.

FV will be asserted for an integral number of row times, which will normally be equal to the height of the output image. If Show_Dark_Rows is set, the dark sample rows will be output before the active image, and FV will be extended to include them. In this case, FV's leading edge happens at time 0.

LV will be asserted during the valid pixels of each row. The leading edge of LV will be offset from the leading edge of FV by 609 PIXCLKs. If Show_Dark_Columns is set, the dark columns will be output before the image pixels, and LV will be extended back to include them; in this case, the first pixel of the active image still occurs at the same position relative to the leading edge of FV. Normally, LV will only be asserted if FV is asserted; this is configurable as described below.

LV Format Options

The default situation is for LV to be negated when FV is negated. The other option available is shown in Figure 9. If Continuous_LV is set, LV is asserted even when FV is not, with the same period and duty cycle. If XOR_Line_Valid is set, but not Continuous_Line_Valid, the resulting LV will be the XOR of FV and the continuous LV.

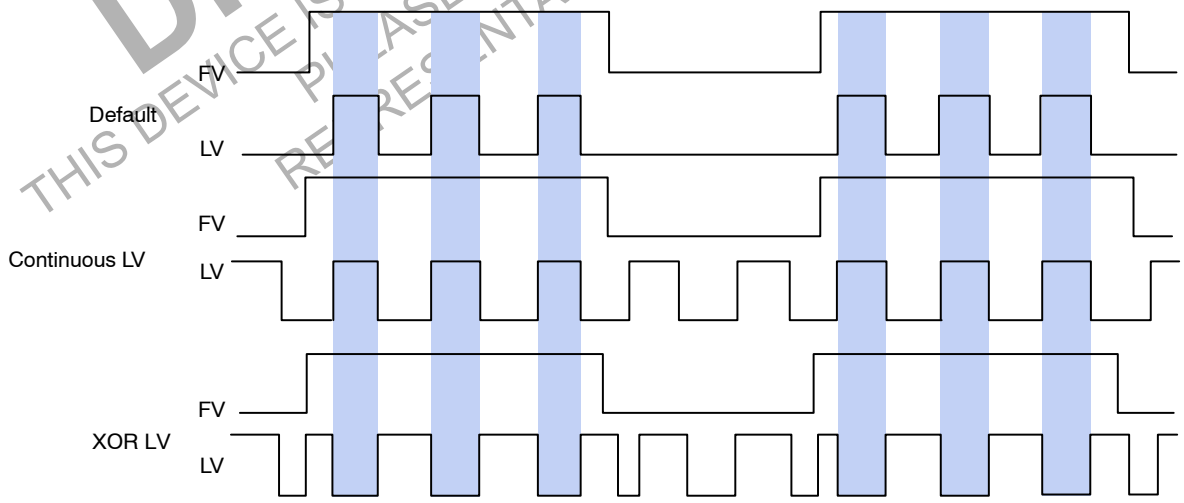


Figure 9. LV Format Options

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The timing of an entire frame is shown in Figure 10.

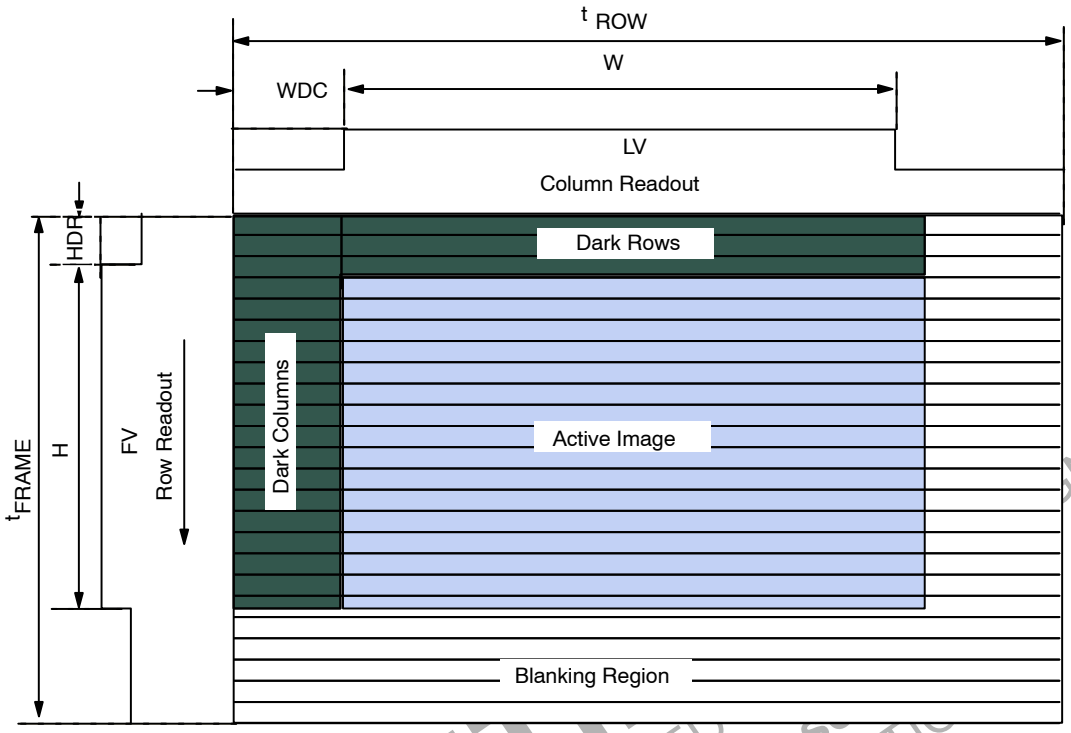


Figure 10. Frame Timing

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Frame Time

The pixel clock (PIXCLK) represents the time needed to sample 1 pixel from the array, and is typically equal to 1 EXTCLK period. The sensor outputs data at the maximum rate of 1 pixel per PIXCLK. One row time (t_{ROW}) is the period from the first pixel output in a row to the first pixel output in the next row. The row time and frame time are defined by equations in Table 8.

Table 8. FRAME TIME

Parameters	Name	Equation	Default Timing at EXTCLK = 96 MHz
fps	Frame Rate	$1/^{t}$FRAME	14
^{t}FRAME	Frame Time	(H + max(VB, VBMIN)) × ^{t}ROW	71.66 ms
^{t}ROW	Row Time	2 × ^{t}PIXCLK x max(((W/2) + max(HB, HBMIN)), (41 + 346 x (Row_Bin+1) + 99))	36.38 μs
^{t}ROW_Default	Row Time	2 × ^{t}PIXCLK x max(((W/2) + max(HB, HBMIN)), (41 + 346 x (Row_Bin+1) + 99))	36.38 μs
^{t}ROW_HDTV	Row Time	2 × ^{t}PIXCLK x max(((W/2) + max(HB, HBMIN)), (41 + 186 x (Row_Bin+1) + 99))	24.4 μs
W	Output Image Width	2 × ceil((Column_Size + 1) / (2 × (Column_Skip + 1)))	2592 PIXCLK
H	Output Image Height	2 × ceil((Row_Size + 1) / (2 × (Row_Skip + 1)))	1944 rows
SW	Shutter Width	max (1, (2 * 16 × Shutter_Width_Upper) + Shutter_Width_Lower)	1943 rows
HB	Horizontal Blanking	Horizontal_Blank + 1	1 PIXCLK
VB	Vertical Blanking	Vertical_Blank + 1	26 rows
HBMIN	Minimum Horizontal Blanking	346 × (Row_Bin + 1) + 64 + (WDC / 2)	450 PIXCLK
VBMIN	Minimum Vertical Blanking	max (8, SW – H) + 1	9 rows
^{t}PIXCLK	Pixclk Period	$1/^{f}$PIXCLK	10.42 ns

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The minimum horizontal blanking (HBMIN) values for various Row_Bin and Column_Bin settings are shown in Table 9.

Table 9. HB_{MIN} VALUES FOR ROW_BIN VS. COLUMN_BIN SETTINGS

	Column_bin (W_{DC})			
Row_bin		0	1	3
	0	450	430	420
	1	796	776	766
	3	1488	1468	1458

Frame Rates at Common Resolutions

Tables 10 and 11 show examples of register settings to achieve common resolutions and their frame rates. Frame rates are shown both with subsampling enabled and disabled.

Table 10. STANDARD RESOLUTIONS

Resolution	Frame Rate	Sub-sampling Mode	Column_ Size (R0x04)	Row_ Size (R0x03)	Shutter_ Width_ Lower (R0x09)	Row_ Bin (R0x22 [5:4])	Row_ Skip (R0x22 [2:0])	Column_ Bin (R0x23 [5:4])	Column_ Skip (R0x23 [2:0])
2592 x 1944 (Full Resolution)	14	N/A	2591	1943	<1943	0	0	0	0
2048 x 1536 QXGA	21	N/A	2047	1535	<1535	0	0	0	0
1600 x 1200 UXGA	31	N/A	1599	1199	<1199	0	0	0	0
1280 x 1024 SXGA	42	N/A	1279	1023	<1023	0	0	0	0
1024 x 768 XGA	63	N/A	1023	767	<767	0	0	0	0
	63	skipping	2047	1535		0	1	0	1
	47	binning	2047	1535		1	1	1	1
800 x 600 SVGA	90	N/A	799	599	<599	0	0	0	0
	90	skipping	1599	1199		0	1	0	1
	65	binning	1599	1199		1	1	1	1
640 x 480 VGA	123	N/A	639	479	<479	0	0	0	0
	123	skipping	2559	1919		0	3	0	3
	53	binning	2559	1919		3	3	3	3

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Table 11. WIDE SCREEN (16:9) RESOLUTIONS

Resolution	Frame Rate	Sub-sampling Mode	Column_ Size (R0x04)	Row_ Size (R0x03)	Shutter_ Width_ Lower (R0x09)	Row_ Bin (R0x22 [5:4])	Row_ Skip (R0x22 [2:0])	Column_ Bin (R0x23 [5:4])	Column_ Skip (R0x23 [2:0])
1920 x 1080 HDTV	31	N/A	1919	1079	<1079	0	0	0	0
1280 x 720 HDTV	59	N/A	1279	719	<719	0	0	0	0
	59	skipping	2559	1439	<719	0	1	0	1
	45	binning	2559	1439	<719	1	1	1	1

2. It is assumed that the minimum horizontal blanking and the minimum vertical blanking conditions are met, and that all other registers are set to default values.

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SERIAL BUS DESCRIPTION

Registers are written to and read from the MT9P001 through the two−wire serial interface bus. The MT9P001 is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9P001 through the serial data (SDATA) line. The SDATA line is pulled up to VDD_IO off−chip by a 1.5 kΩ resistor. Either the slave or master device can pull the SDATA line LOW−the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two−wire serial defines several different transmission codes, as follows:

1. a start bit
2. the slave device 8−bit address
3. an (a no) acknowledge bit
4. an 8−bit message
5. a stop bit

Sequence

A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8−bit address. The last bit of the address determines if the request is a READ or a WRITE, where a "0" indicates a WRITE and a "1" indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request is a WRITE, the master then transfers the 8−bit register address to which a WRITE should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The MT9P001 uses 16−bit data for its internal registers, thus requiring two 8−bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write−mode slave address and 8−bit register address, just as in the WRITE request. The master then sends a start bit and the read−mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8−bit transfer. The register address is automatically−incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH−to−LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW−to−HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8−bit address of a two−wire serial interface device consists of 7 bits of address and 1 bit of direction. A "0" in the LSB (least significant bit) of the address indicates write mode (0xBA), and a "1" indicates read mode (0xBB).

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two−wire serial interface clock−it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No−Acknowledge Bit

The no−acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no−acknowledge bit is used to terminate a read sequence.

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TWO−WIRE SERIAL INTERFACE SAMPLE WRITE AND READ SEQUENCES

16−Bit WRITE Sequence

A typical WRITE sequence for writing 16 bits to a register is shown in Figure 11. A start bit given by the master, followed by the write address, starts the sequence. The image sensor then gives an acknowledge bit and expects the register address to come first, followed by the 16−bit data. After each 8−bit transfer, the image sensor sends an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

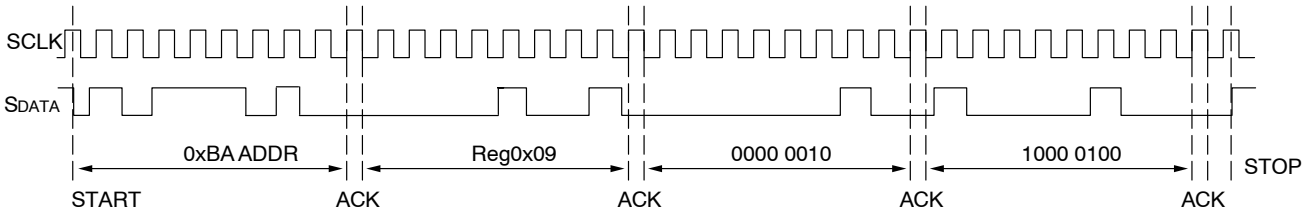


Figure 11. Timing Diagram Showing a WRITE to Reg0x09 with the Value 0x0284

16−Bit READ Sequence

A typical READ sequence is shown in Figure 12. First the master has to write the register address, as in a WRITE sequence. Then a start bit and the read address specifies that a READ is about to happen from the register. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8−bit transfer. The register address is incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

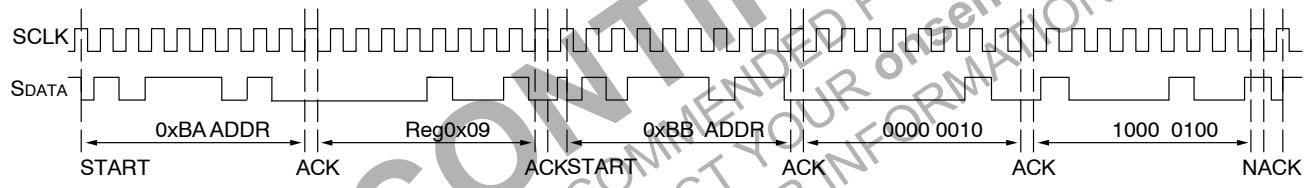


Figure 12. Timing Diagram Showing a READ to Reg0x09 with the Value 0x0284

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FEATURES

Reset

The MT9P001 may be reset by using RESET_BAR (active LOW) or the reset register.

Hard Reset

Assert (LOW) RESET_BAR, it is not necessary to clock the device. All registers return to the factory defaults. When the pin is negated (HIGH), the chip resumes normal operation.

Soft Reset

Set the Reset register field to “1” (R0x0D[0] = 1). All registers except the following will be reset:

- Chip_Enable
- Synchronize_Changes
- Reset
- Use_PLL
- Power_PLL
- PLL_m_Factor
- PLL_n_Divider
- PLL_p1_Divider

When the field is returned to “0,” the chip resumes normal operation.

$$f_{PIXCLK} = \begin{cases} f_{EXTCLK} & \text{if Divide_Pixel_Clock} = 0 \\ f_{EXTCLK} / (2 \times \text{Divide_Pixel_Clock}) & \text{otherwise} \end{cases}$$

The DOUT, LV, FV, and STROBE outputs are launched on the rising edge of PIXCLK, and should be captured on the falling edge of PIXCLK. The specific relationship of PIXCLK to these other outputs can be adjusted in two ways. If Invert_Pixel_Clock is set, the sense of PIXCLK is inverted from that shown in Figure 8. In addition, if the pixel clock has been divided by Divide_Pixel_Clock, it can be shifted relative to the other outputs by setting Shift_Pixel_Clock.

PLL−Generated Master Clock

The PLL contains a prescaler to divide the input clock applied on EXTCLK, a VCO to multiply the prescaler output, and another divider stage to generate the output clock. The clocking structure is shown in Figure 13. PLL control registers can be programmed to generate desired master clock frequency.

NOTE: The PLL control registers must be programmed while the sensor is in the software Standby state. The effect of programming the PLL divisors while the sensor is in the streaming state is undefined.

Power Up and Power Down

When first powering on the MT9P001, follow this sequence:

1. Ensure RESET_BAR is asserted (LOW).
2. Bring up the supplies. If both the analog and the digital supplies cannot be brought up simultaneously, ensure the digital supply comes up first.
3. Negate RESET_BAR (HIGH) to bring up the sensor.

When powering down, be sure to follow this sequence to ensure that I/Os do not load any buses that they are connected to.

1. Assert RESET_BAR.
2. Remove the supplies.

Clocks

The MT9P001 requires one clock (EXTCLK), which is nominally 96 MHz. By default, this results in pixels being output on the DOUT pins at a maximum data rate of 96 Mp/s. With V_{DD}_IO = 1.8 V, maximum master clock and maximum data rate become 48 MHz and 48 Mp/s, respectively. The EXTCLK clock can be divided down internally by setting Divide_Pixel_Clock to a non−zero value. This slows down the operation of the chip as though EXTCLK had been divided externally.

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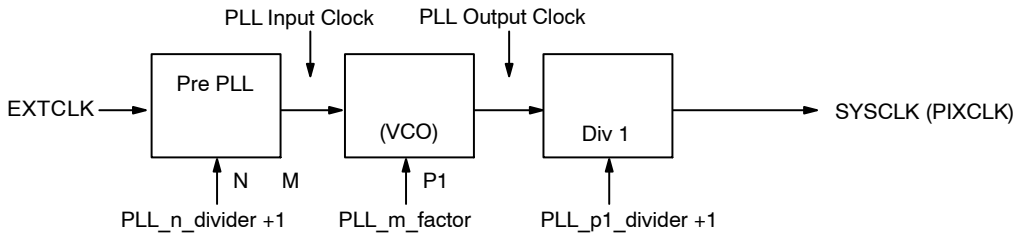


Figure 13. PLL−Generated Master Clock

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PLL Setup

The MT9P001 has a PLL which can be used to generate the pixel clock internally.

To use the PLL:

1. Bring the MT9P001 up as normal, make sure that ^{f}EXTCLK is between 6 and 27 MHz and then power on the PLL by setting Power_PLL (R0x10[0] = 1).
2. Set PLL_m_Factor, PLL_n_Divider, and PLL_p1_Divider based on the desired input (^{f}EXTCLK) and output (^{f}PIXCLK) frequencies. Determine the M, N, and P1 values to achieve the desired ^{f}PIXCLK using this formula:

   fPIXCLK = (fEXTCLK × M) / (N × P1)
   where
   M = PLL_m_Factor
   N = PLL_n_Divider + 1
   P1 = PLL_p1_Divider + 1
   2 MHz < ^{f}EXTCLK / N < 13.5 MHz
   180 MHz < (^{f}EXTCLK × M) / N < 360 MHz

NOTE: If P1 is odd (that is, PLL_p1_Divider is even), the duty cycle of the internal system clock will not be 50:50. In this case, it is important that either a slower clock is used or all clock enable bits are set in R101.
It is desirable to keep (fEXTCLK / n) as large as possible within the limits. Also, "m" must be between 16 and 255, inclusive.

3. Wait 1 ms to ensure that the VCO has locked.
4. Set Use_PLL (R0x10[1] = 1) to switch from EXTCLK to the PLL-generated clock.

Standby and Chip Enable

The MT9P001 can be put in a low−power Standby state by either method below:

1. Hard Standby: By pulling STANDBY_BAR LOW, or
2. Soft Standby: By clearing the Chip_Enable register field (R0x07[1] = 0).

When the sensor is put in standby, all internal clocks are gated, and analog circuitry is put in a state that it draws minimal power. The two−wire serial interface remains minimally active so that the Chip_Enable bit can subsequently be cleared. READs cannot be performed and only the Chip_Enable and Invert_Standby registers are writable.

If the sensor was in continuous mode when put in standby, it resumes from where it was when standby was deactivated. Naturally, this frame and the next frame are corrupted, though the sensor itself does not realize this. As this could affect automatic black level calibration, it is recommended that either the chip be paused (by setting Restart_Pause) before being put in standby mode, or it be restarted (setting Restart) upon resumption of operation.

For maximum power savings in standby mode, EXTCLK should not be toggling.

When standby mode is entered, either by clearing Chip_Enable or by asserting STANDBY_BAR, the PLL is disabled automatically or powered down. It must be manually re−enabled when leaving standby as needed.

Full−Array Readout

The entire array, including dark pixels, can be read out without digital processing or automatic black level adjustments. This can be accomplished as follows:

1. Set Row_Start and Column_Start to 0.
2. Set Row_Size to 2003.
3. Set Column_Size to 2751.
4. Set Manual_BLC to 1.
5. Set Row_BLC to 0.
6. Set Row_Black_Default_Offset to 0.
7. Set Show_Dark_Rows and Show_Dark_Columns to 0.

If automatic analog (coarse) BLC is desired, but no digital processing, modify the above settings as follows:

1. Set Row_Start to 12.
2. Set Row_Size to 1993.
3. Set Manual_BLC to 0.

These settings result in the same array layout as above, but only 22 dark rows are available at the top of the array; the first eight are used in the black level algorithm, and there should be a two−row buffer between the black region and the active region.

Window Control

The output image window of the pixel (the FOV) is defined by four register fields. Column_Start and Row_Start define the X and Y coordinates of the upper−left corner of the FOV. Column_Size defines the width of the FOV, and Row_Size defines the height of the FOV in array pixels.

The Column_Start and Row_Start fields must be set to an even number. The Column_Size and Row_Size fields must be set to odd numbers (resulting in an even size for the FOV). The Row_Start register should be set no lower than 12 if either Manual_BLC is clear or Show_Dark_Rows is set.

If no special resolution modes are set (see below), the width of the output image, W, is Column_Size + 1 and the height, H, is Row_Size + 1.

Readout Modes

Subsampling

By default, the resolution of the output image is the full width and height of the FOV as defined in "Window Control". The output resolution can be reduced by two methods: Skipping and Binning.

Row and column skip modes use subsampling to reduce the output resolution without reducing FOV. The MT9P001 also has row and column binning modes, which can reduce the impact of aliasing introduced by the use of skip modes. This is achieved by the averaging of 2 or 3 adjacent rows and columns (adjacent same−color pixels). Both 2X and 4X binning modes are supported. Rows and columns can be binned independently.

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Skipping

Skipping reduces resolution by using only selected pixels from the FOV in the output image. In skip mode, entire rows and columns of pixels are not sampled, resulting in a lower resolution output image. A skip 2X mode skips one Bayer pair of pixels for every pair output. Skip 3X skips two pairs for each one pair output. Rows and columns are always read out in pairs. If skip 2X mode is enabled with otherwise default sensor settings, the columns in the output image correspond to the pixel array columns 16, 17, 20, 21, 24, 25... .

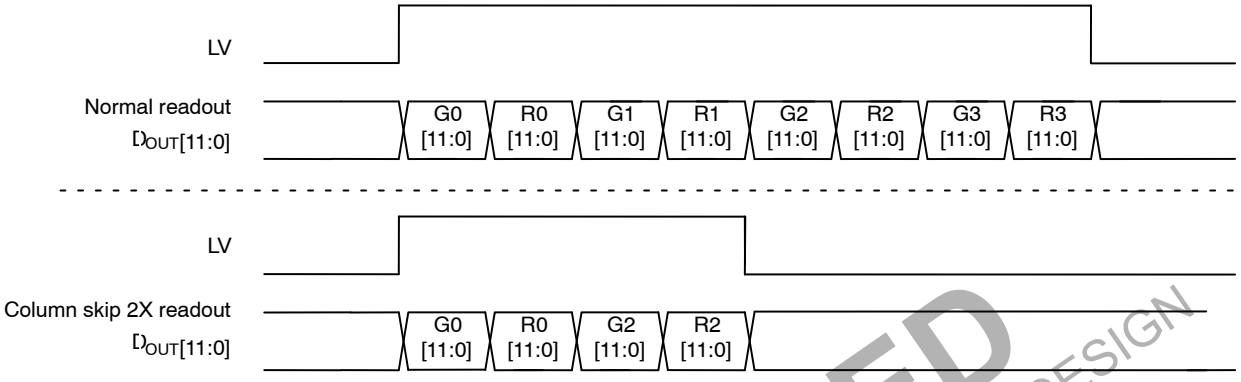


Figure 14. Eight Pixels in Normal and Column Skip 2X Readout Modes

Skipping can be enabled separately for rows and columns. To enable skip mode, set either or both of Row_Skip and Column_Skip to the number of pixel pairs that should be skipped for each pair used in the output image. For example, to set column skip 2X mode, set Column_Skip to "1."

The size of the output image is reduced by the skip mode as shown in the following two equations:

$$W = 2 \times \text{ceil}((\text{Column_Size} + 1))/(2 \times (\text{Column_Skip} + 1))) \quad \text{(eq. 1)}$$

$$H = 2 \times \text{ceil}((\text{Row_Size} + 1))/(2 \times (\text{Row_Skip} + 1))) \quad \text{(eq. 2)}$$

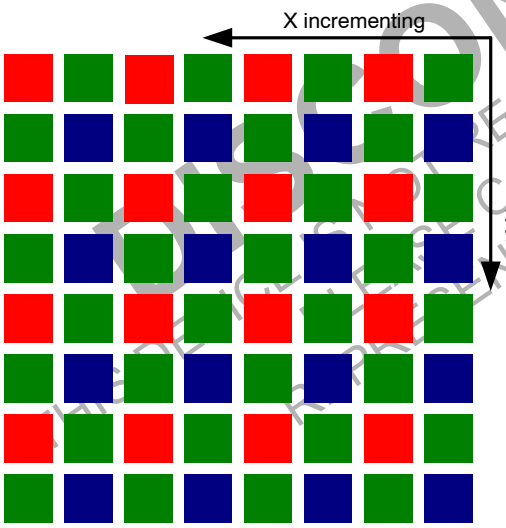


Figure 15. Pixel Readout (no skipping)

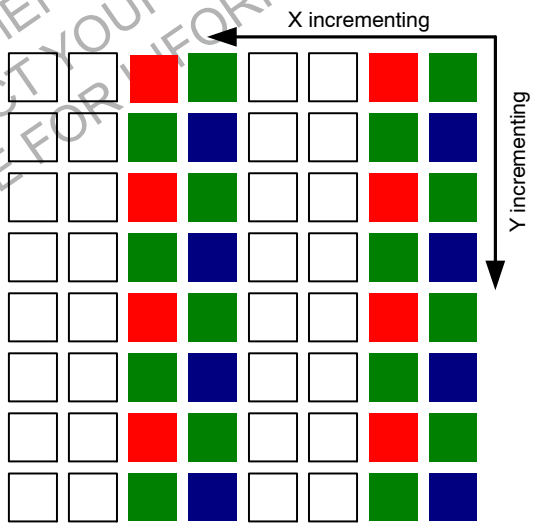


Figure 16. Pixel Readout (Column Skip 2X)

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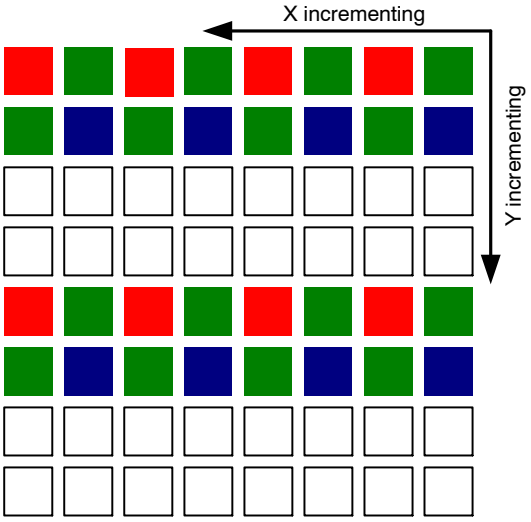


Figure 17. Pixel Readout (Row Skip 2X)

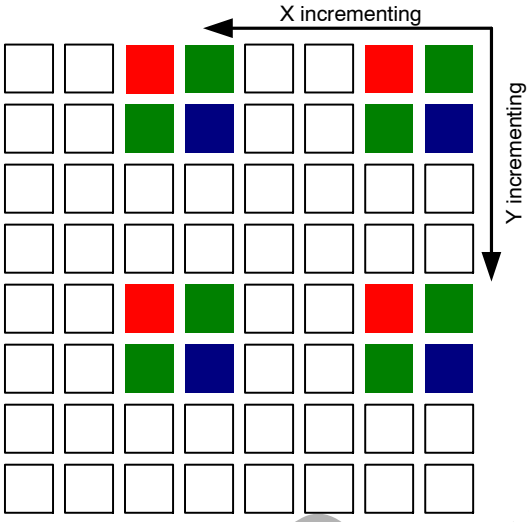


Figure 18. Pixel Readout
(Column Skip 2X, Row Skip 2X)

Binning

Binning reduces resolution by combining adjacent same−color imager pixels to produce one output pixel. All of the pixels in the FOV contribute to the output image in bin mode. This can result in a more pleasing output image with reduced subsampling artifacts. It also improves low−light performance. For columns, the combination step can be either an averaging or summing operation. Depending on lighting conditions, one or the other may be desirable. In low−light conditions, summing produces a gain roughly equivalent to the column bin factor. Column summing may be enabled by setting Column_Sum.

Binning works in conjunction with skipping. Pixels that would be skipped because of the Column_Skip and Row_Skip settings can be averaged instead by setting Column_Bin and Row_Bin to the number of neighbor pixels to be averaged with each output pixel. For example, to set bin 2X mode, set Column_Skip and Column_Bin to 1. Additionally, Column_Start must be a multiple of (2 * (Column_Bin + 1)) and Row_Start must be a multiple of (2 * (Row_Bin + 1)).

Only certain combinations of binning and skipping are allowed.

These are shown in Table 12. If an illegal skip value is selected for a bin mode, a legal value is selected instead.

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Table 12. LEGAL VALUES FOR COLUMN_SKIP BASED ON COLUMN_BIN

Column_Bin	Legal Values for Column_Skip
0 (no binning)	0, 1, 2, 3, 4, 5, 6
1 (Bin 2X)	1, 3, 5
3 (Bin 4X)	3

3. Ensure that Column_Start (R0x02) is set in the form shown below, where n is an integer:

	Mirror Column = 0	Mirror Column = 1
no bin	4n	4n + 2
Bin 2X	8n	8n + 4
Bin 4X	16n	16n + 8

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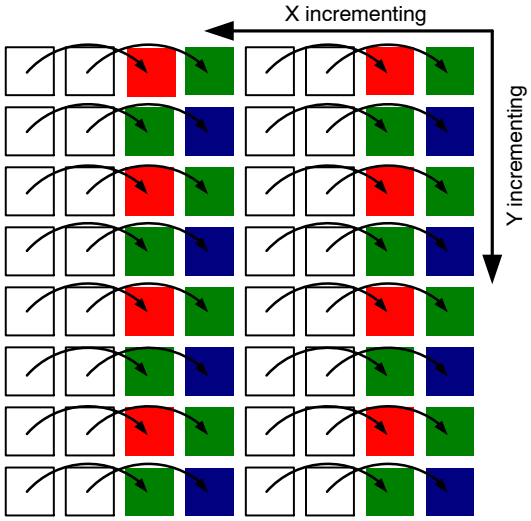


Figure 19. Pixel Readout (Column Bin 2X)

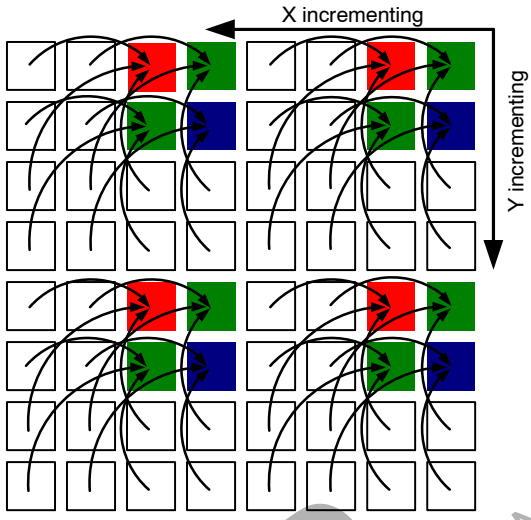


Figure 20. Pixel Readout (Column Bin 2X, Row Bin 2X)

Mirror

Column Mirror Image

By setting R0x20[14] = 1, the readout order of the columns is reversed, as shown in Figure 21. The starting color, thus Bayer pattern, is preserved when mirroring the columns.

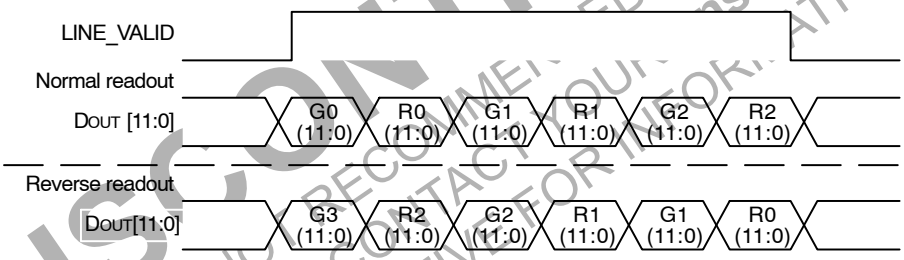


Figure 21. Six Pixels in Normal and Column Mirror Readout Modes

Row Mirror Image

By setting R0x20[15] = 1, the readout order of the rows is reversed as shown in Figure 22. The starting color, thus Bayer pattern, is preserved when mirroring the rows.

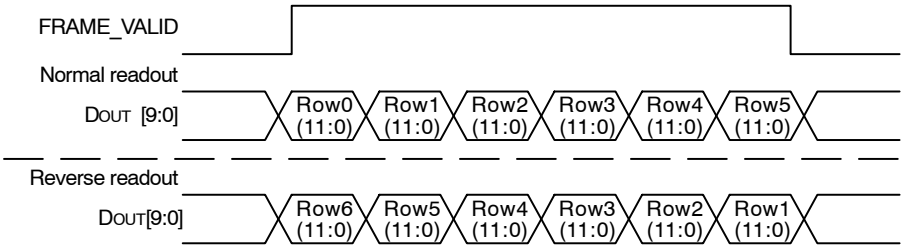


Figure 22. Six Pixels in Normal and Column Mirror Readout Modes

By default, active pixels in the resulting image are output in row−major order (an entire row is output before the next row is begun), from lowest row/column number to highest. If desired, the output (and sampling) order of the rows and columns can be reversed. This affects only pixels in the active region defined above, not any pixels read out as dark rows or dark columns. When the readout direction is reversed, the color order is reversed as well (red, green, red, and so on, instead of green, red, green, and so on, for example).

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If row binning is combined with row mirroring, the binning is still done in the positive direction. Therefore, if the first output row in bin 2X + row mirror was 1997, pixels on rows 1997 and 1999 would be averaged together. The next pixel output would be from rows 1996 and 1998, followed by the average of 1993 and 1995.

For column mirroring plus binning, the span of pixels used should be the same as with non−mirror mode.

Maintaining a Constant Frame Rate

Maintaining a constant frame rate while continuing to have the ability to adjust certain parameters is the desired scenario. This is not always possible, however, because register updates are synchronized to the read pointer, and the shutter pointer for a frame is usually active during the readout of the previous frame. Therefore, any register changes that could affect the row time or the set of rows sampled causes the shutter pointer to start over at the beginning of the next frame.

By default, the following register fields cause a "bubble" in the output rate (that is, the vertical blank increases for one frame) if they are written in continuous mode, even if the new value would not change the resulting frame rate:

- Row_Start
- Row_Size
- Column_Size
- Horizontal_Blank
- Vertical_Blank
- Shutter_Delay
- Mirror_Row
- Row_Bin
- Row_Skip
- Column_Skip

The size of this bubble is (SW × t_{ROW}), calculating the row time according to the new settings.

The Shutter_Width_Lower and Shutter_Width_Upper fields may be written without causing a bubble in the output rate under certain circumstances. Because the shutter sequence for the next frame often is active during the output of the current frame, this would not be possible without special provisions in the hardware. Writes to these registers take effect two frames after the frame they are written, which allows the shutter width to increase without interrupting the output or producing a corrupt frame (as long as the change in shutter width does not affect the frame time).

Synchronizing Register Writes to Frame Boundaries

Changes to most register fields that affect the size or brightness of an image take effect on the frame after the one during which they are written. These fields are noted as "synchronized to frame boundaries" in Table 1 in the MT9P0901 register reference. To ensure that a register update takes effect on the next frame, the write operation must be completed after the leading edge of FV and before the trailing edge of FV.

As a special case, in Snapshot modes (see "Operating Modes"), register writes that occur after FV but before the next trigger will take effect immediately on the next frame, as if there had been a Restart. However, if the trigger for the next frame in ERS Snapshot mode occurs during FV, register writes take effect as with continuous mode.

Additional control over the timing of register updates can be achieved by using synchronize_changes. If this bit is set, writes to certain register fields that affect the brightness of the output image do not take effect immediately. Instead, the new value is remembered internally. When synchronize_changes is cleared, all the updates simultaneously take effect on the next frame (as if they had all been written the instant synchronize_changes was cleared). Register fields affected by this bit are identified in Table 2.

Fields not identified as being frame−synchronized or affected by synchronize_changes are updated immediately after the register write is completed. The effect of these registers on the next frame can be difficult to predict if they affect the shutter pointer.

Restart

To restart the MT9P001 at any time during the operation of the sensor, write a "1" to the restart register (R0x0B[0] = 1). This has two effects: first, the current frame is interrupted immediately. Second, any writes to frame−synchronized registers and the shutter width registers take effect immediately, and a new frame starts (in continuous mode). Register updates being held by synchronize_changes do not take effect until that bit is cleared. The current row and one following row complete before the new frame is started, so the time between issuing the Restart and the beginning of the next frame can vary by about t_{ROW}.

If Pause_Restart is set, rather than immediately beginning the next frame after a restart in continuous mode, the sensor pauses at the beginning of the next frame until Pause_Restart is cleared. This can be used to achieve a deterministic time period from clearing the Pause_Restart bit to the beginning of the first frame, meaning that the controller does not need to be tightly synchronized to LV or FV.

NOTE: When Pause_Restart is cleared, be sure to leave Restart set to "1" for proper operation. The Restart bit will be cleared automatically by the device.

Image Acquisition Modes

The MT9P001 supports two image acquisition modes (Shutter Types) (see "Operating Modes"), electronic rolling shutter and global reset release.

Electronic Rolling Shutter

The ERS modes take pictures by scanning the rows of the sensor twice in the order described in "Full−Array Readout". On the first scan, each row is released from reset, starting the exposure. On the second scan, the row is sampled, processed, and returned to the reset state. The exposure for

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any row is therefore the time between the first and second scans. Each row is exposed for the same duration, but at slightly different point in time, which can cause a shear in moving subjects.

Whenever the mode is changed to an ERS mode (even from another ERS mode), and before the first frame following reset, there is an anti−blooming sequence where all rows are placed in reset. This sequence must complete before continuous readout begins. This delay is:

tALLRESET = 16 × 2004 × tACLK

Global Reset Release

The GRR modes attempt to address the shearing effect by starting all rows' exposures at the same time. Instead of the first scan used in ERS mode, the reset to each row is released simultaneously. The second scan occurs as normal, so the exposure time for each row would different. Typically, an external mechanical shutter would be used to stop the exposure of all rows simultaneously.

In GRR modes, there is a startup overhead before each frame as all rows are initially placed in the reset state (tALLRESET). Unlike ERS mode, this delay always occurs before each frame. However, it occurs as soon as possible after the preceding frame, so typically the time from trigger to the start of exposure does not include this delay. To ensure that this is the case, the first trigger must occur no sooner than tALLRESET after the previous frame is read out.

Exposure

The nominal exposure time, tEXP, is the effective shutter time in ERS modes, and is defined by the shutter width, SW, and the shutter overhead, SO, which includes the effect of Shutter_Delay. Exposure time for other modes is defined relative to this time. Increasing Shutter_Delay (SD) decreases the exposure time. Exposure times are typically specified in units of row time, although it is possible to fine−tune exposures in units of tACLKs (where tACLK is 2 * tPIXCLK).

tEXP = SW × tROW − SO × 2 × tPIXCLK

where:

SW = max(1, (2 * 16 × Shutter_Width_Upper) + Shutter_Width_Lower)

SO = 208 × (Row_Bin + 1) + 98 + min(SD, SDmax) − 94

SD = Shutter_Delay + 1

SDmax = 1232; if SW < 3
1504, otherwise

The exposure time is calculated by determining the reset time of each pixel row (with time 0 being the start of the first row time), and subtracting it from the sample time. Under normal conditions in ERS modes, every pixel should end up with the same exposure time. In global shutter release modes, or in row binning modes, the exposure times of individual pixels can vary.

In global shutter release modes (described later) exposure time starts simultaneously for all rows, but still ends as defined above. In a real system, the exposure would be stopped by a mechanical shutter, which would effectively stop the exposure to all rows simultaneously. Because this specification does not consider the effect of an external shutter, each output row's exposure time will differ by tROW from the previous row.

Global shutter modes also introduce a constant added to the shutter time for each row, because the exposure starts during the global shutter sequence, and not during any row's shutter sequence. For each additional row in a row bin, this offset will increase by the length of the shutter sequence.

In Bulb_Exposure modes (also detailed later), the exposure time is determined by the width of the TRIGGER pulse rather than the shutter width registers. In ERS bulb mode, it is still a multiple of row times, and the shutter overhead equation still applies. In GRR bulb mode, the exposure time is granular to ACLKs, and shutter overhead (and thus shutter_delay) has no effect.

Operating Modes

In the default operating mode, the MT9P001 continuously samples and outputs frames. It can be put in "snapshot" or triggered mode by setting snapshot, which means that it samples and outputs a frame only when triggered. To leave snapshot mode, it is necessary to first clear Snapshot then issue a restart.

When in snapshot mode, the sensor can use the ERS or the GRR. The exposure can be controlled as normal, with the shutter_width_lower and shutter_width_upper registers, or it can be controlled using the external TRIGGER signal. The various operating modes are summarized in Table 13.

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Table 13. OPERATING MODE

Mode	Settings	Description
ERS Continuous	Default	Frames are output continuously at the frame rate defined by ^{t}FRAME. ERS is used, and the exposure time is electronically controlled to be ^{t}EXP.
ERS Snapshot	Snapshot = 1	Frames are output one at a time, with each frame initiated by a trigger. ERS is used, and the exposure time is electronically controlled to be ^{t}EXP.
ERS Bulb	Snapshot = 1; Bulb_Exposure = 1	Frames are output one at a time, with each frame's exposure initiated by a trigger. ERS is used. End of exposure and readout are initiated by a second trigger.

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Table 13. OPERATING MODE (continued)

Mode	Settings	Description
GRR Snapshot	Snapshot = 1; Global_Reset = 1	Frames are output one at a time, with each frame initiated by a trigger. GRR is used. Readout is electronically triggered based on SW.
GRR Bulb	Snapshot = 1; Bulb_Exposure = 1; Global_Reset = 1	Frames are output one at a time, with each frame initiated by a trigger. GRR is used. Readout is initiated by a second trigger.

4. In ERS bulb mode, SW must be greater than 4 (use trigger wider than tROW * 4).

All operating modes share a common set of operations:

1. Wait for the first trigger, then start the exposure.
2. Wait for the second trigger, then start the readout.

The first trigger is by default automatic, producing continuous images. If snapshot is set, the first trigger can either be a low level on the TRIGGER pin or writing a “1” to the trigger register field. If Invert_Trigger is set, the first trigger is a high level on TRIGGER pin (or a “1” written to trigger register field). Because TRIGGER is level−sensitive, multiple frames can be output (with a frame rate of tFRAME) by holding TRIGGER pin at the triggering level.

The second trigger is also normally automatic, and generally occurs SW row times after the exposure is started. If Bulb_Exposure is set, the second trigger can either be a high level on TRIGGER or a write to Restart. If Invert_Trigger is set, the second trigger is a low level on TRIGGER (or a Restart). In bulb modes, the minimum possible exposure time depends on the mechanical shutter used.

After one frame has been output, the chip will reset step 1, above, eventually waiting for the first trigger again. The next trigger may be issued after ((VB − 8) x tROW) in ERS modes or tALLREST in GRR modes.

The choice of shutter type is made by Global_Reset. If it is set, the GRR shutter is used; otherwise, ERS is used. The two shutters are described in “Electronic Rolling Shutter” and “Global Reset Release”.

The default ERS continuous mode is shown in Figure 8. Figure 23 shows default signal timing for ERS snapshot modes, while Figure 24 shows default signal timing for GRR snapshot modes.

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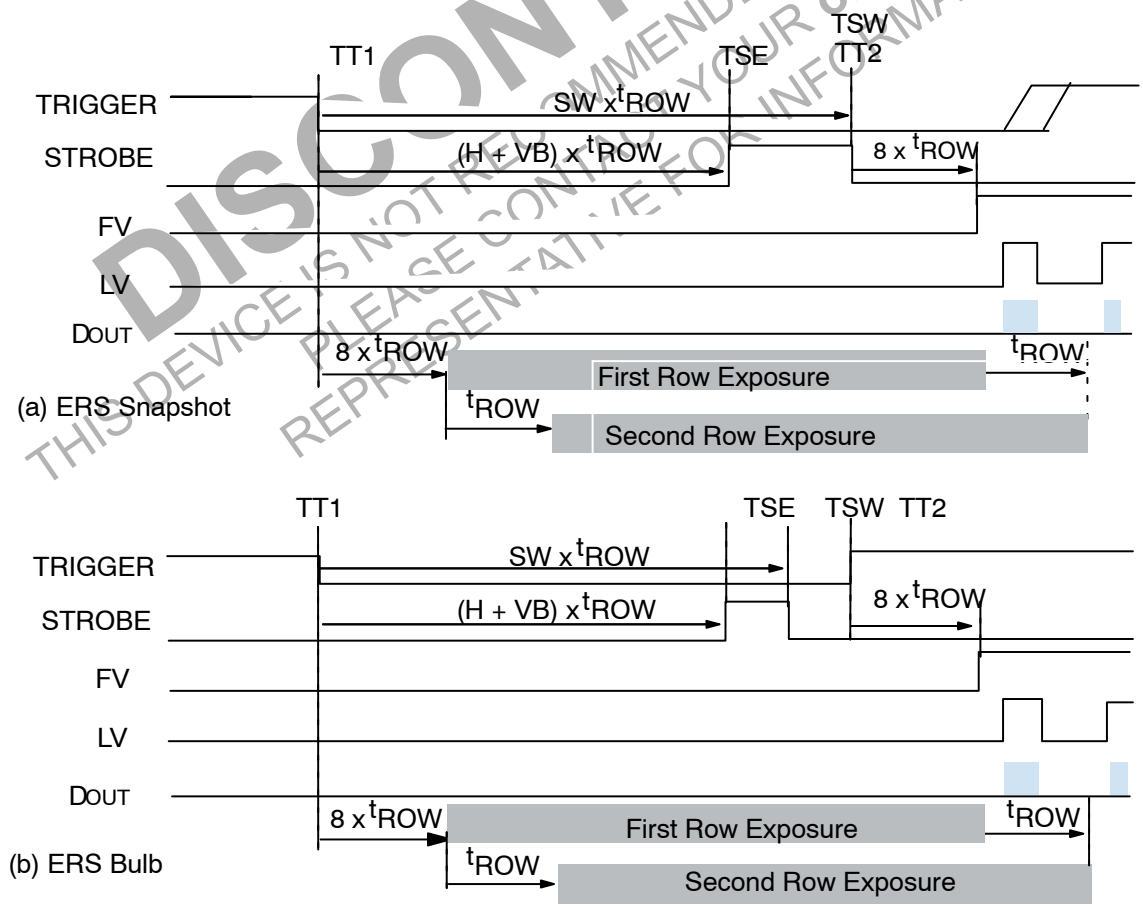


Figure 23. ERS Snapshot Timing

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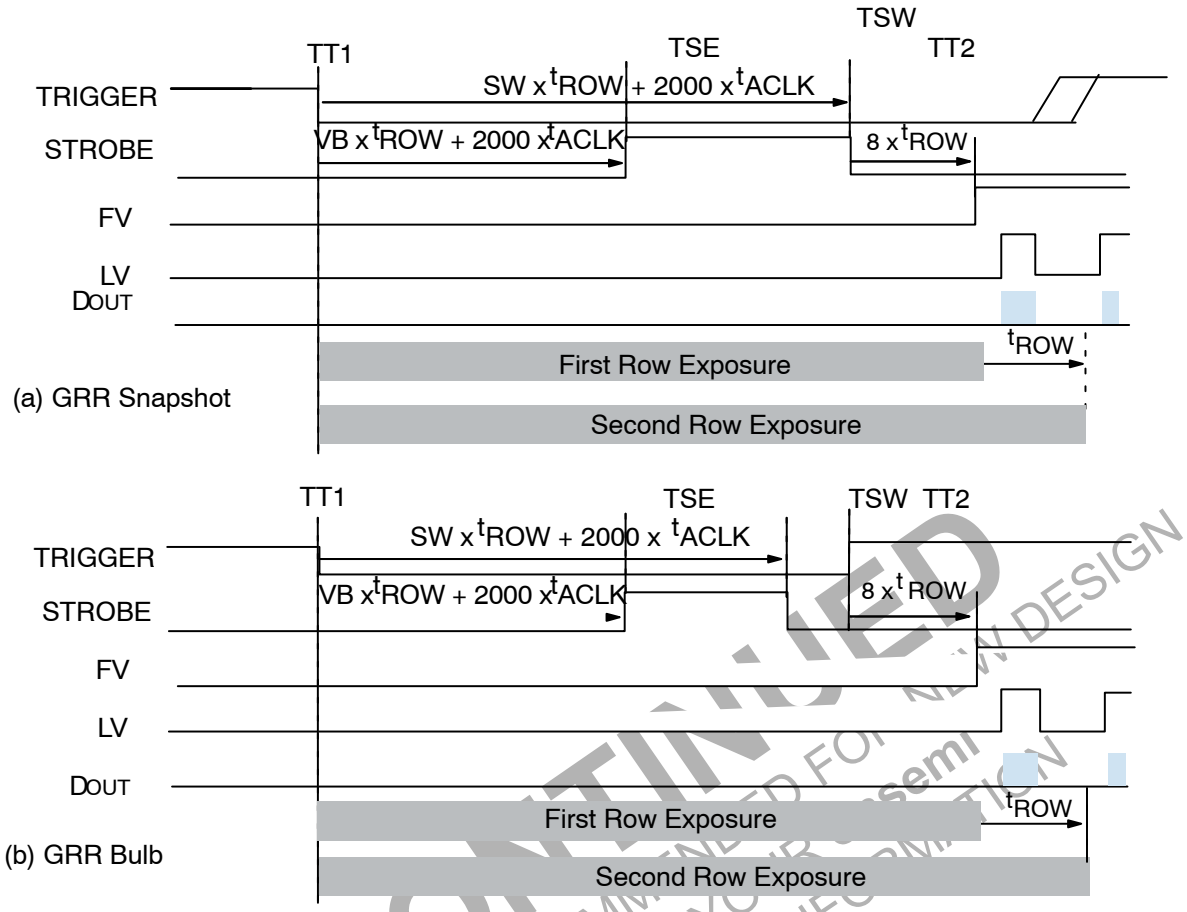


Figure 24. GRR Snapshot Timing

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Strobe Control

To support synchronization of the exposure with external events such as a flash or mechanical shutter, the MT9P001 produces a STROBE output. By default, this signal is asserted for approximately the time that all rows are simultaneously exposing, minus the vertical blanking time, as shown in Figures 23 and 24. Also indicated in these figures are the leading and trailing edges of STROBE, which an be configured to occur at one of several timepoints. The leading edge of STROBE occurs at STROBE_Start, and the trailing edge at STROBE_End, which are set to codes described in Table 14.

Table 14. STROBE TIMEPOINTS

Symbol	Timepoint	Code
TT1	Trigger 1 (start of shutter scan)	–
TSE	Start of exposure (all rows simultaneously exposing) offset by VB	1
TSW	End of shutter width (expiration of the internal shutter width counter)	2
TT2	Trigger 2 (start of readout scan)	3

If STROBE_Start and STROBE_End are set to the same timepoint, the strobe is a tROW wide pulse starting at the STROBE_Start timepoint. If the settings are such that the strobe would occur after the trailing edge of FV, the strobe may be only tACLK wide; however, because there is no concept of a row at that time. The sense of the STROBE signal can be inverted by setting Invert_Strobe (R0x1E[5] = 1. To use strobe as a flash in snapshot modes or with mechanical shutter, set the Strobe_Enable register bit field R0x1E[4] = 1.

Signal Chain and Datapath

The signal chain and datapath are shown in Figure 25. Each color is processed independently, including separate gain and offset settings. Voltages sampled from the pixel array are first passed through an analog gain stage, which can produce gain factors between 1 and 8. An analog offset is then applied, and the signal is sent through a 12−bit analog−to−digital converter. In the digital space, a digital gain factor of between 1 and 16 is applied, and then a digital

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offset of between −2048 and 2047 is added. The resulting 12−bit pixel value is then output on the DOUT[11:0] ports.

The analog offset applied is determined automatically by the black level calibration algorithm, which attempts to shift the output of the analog signal chain so that black is at a particular level. The digital offset is a fine−tuning of the analog offset.

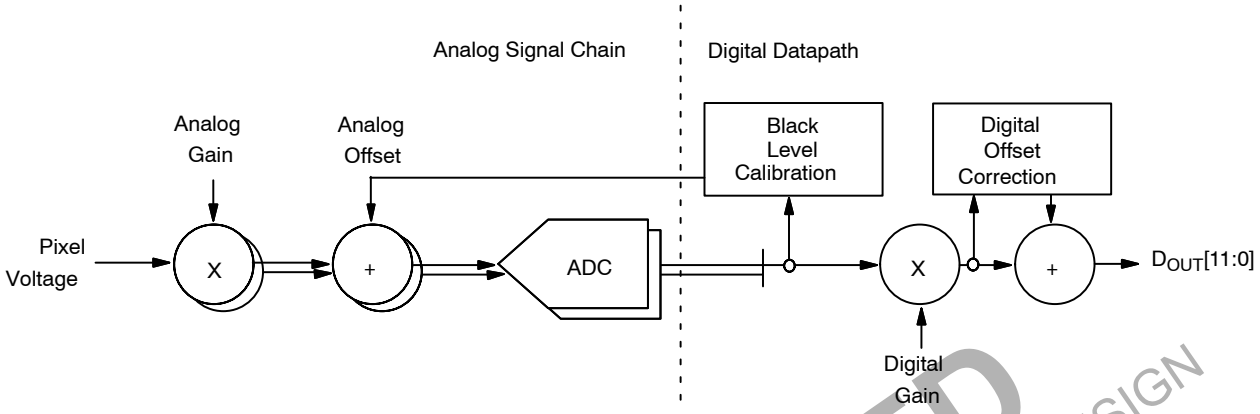


Figure 25. Signal path

Gain

There are two types of gain supported: analog gain and digital gain. Combined, gains of between 1 and 128 are possible. The recommended gain settings are shown in Table 15.

Table 15. GAIN INCREMENT SETTINGS

Gain Range	Increments	Digital Gain	Analog Multipier	Analog Gain
1− 4	0.125	0	0	8−32
4.25−8	0.25	0	1	17−32
9−128	1	1−120	1	32

5. Analog gain should be maximized before applying digital gain.

The combined gain for a color C is given by:

$G_C = AG_C \times DG_C$.

Analog Gain

The analog gain is specified independently for each color channel. There are two components, the gain and the multiplier. The gain is specified by Green1_Analog_Gain, Red_Analog_Gain, Blue_Analog_Gain, and Green2_Analog_Gain in steps of 0.125. The analog multiplier is specified by Green1_Analog_Multiplier, Red_Analog_Multiplier, Blue_Analog_Multiplier, and Green2_Analog_Multiplier. These combine to form the analog gain for a given color C as shown in this equation:

$AG_C = (1 + C_Analog_Multiplier) \times (C_Analog_Gain / 8)$

The gain component can range from 0 to 7.875 in steps of 0.125, and the multiplier component can be either 0 or 1 (resulting in a multiplier of 1 or 2). However, it is best to keep the “gain” component between 1 and 4 for the best noise performance, and use the multiplier for gains between 4 and 8.

Digital Gain

The digital gain is specified independently for each color channel in steps of 0.125. It is controlled by the register fields Green1_Digital_Gain, Red_Digital_Gain, Blue_Digital_Gain, and Green2_Digital_Gain. The digital gain for a color C is given by:

$DG_C = 1 + (C_Digital_Gain / 8)$

Offset

The MT9P001 sensor can apply an offset or shift to the image data in a number of ways.

An analog offset can be applied on a color−wise basis to the pixel voltage as it enters the ADC. This makes it possible to adjust for offset introduced in the pixel sampling and gain stages to be removed, centering the resulting voltage swing in the ADC’s range. This offset can be automatically determined by the sensor using the automatic black level calibration (BLC) circuit, or it can be set manually by the user. It is a fairly coarse adjustment, with adjustment step sizes of 4 to 8 LSBs.

Digital offset is also added on a color−wise and line−wise basis to fine tune the black level of the output image. This offset is based on an average black level taken from each row’s dark columns, and is automatically determined by the digital row−wise black level calibration (RBLC) circuit. If

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the RBLC circuit is not used, a user−defined offset can be applied instead. This offset has a resolution of 1 LSB.

A digital offset is added on a color−wise basis to account for channel offsets that can be introduced due to “even” and “odd” pixels of the same color going through a slightly different ADC chain. This offset is automatically determined based on dark row data, but it can also be manually set.

Analog Black Level Calibration

The MT9P001 black level calibration circuitry provides a feedback control system since adjustments to the analog offset are imprecise by nature. The goal is that within the dark row region of any supported output image size, the offset should have been adjusted such that the average black level falls within the specified target thresholds.

The analog offsets normally need a major adjustment only when leaving the Reset state or when there has been a change to a color’s analog gain. Factors like shutter width and temperature have lower−order impact, and generally only require a minor adjustment to the analog offsets. The MT9P001 has various calibration modes to keep the system stable while still supporting the need for rapid offset adjustments when necessary.

The two basic steps of black level calibration are:

1. Take a sample.
2. If necessary, adjust the analog offset.

Black level calibration is normally done separately for each color channel, and different channels can be using different sample or adjustment methods at the same time. However, because both Green1 and Green2 pixels go through the same signal chain, and Red and Blue pixels likewise go through the same signal chain, it is expected that the chosen offset for these pairs should be the same as long as the gains are the same. If Lock_Green_Calibration is set, and (Green1_Analog_Gain = Green2_Analog_Gain) and (Green1_Analog_Multiplier = Green2_Analog_Multiplier), the calculated or user−specified Green1_Offset is used for both green channels. Similarly, if Lock_Red/Blue_Calibration is set, and (Red_Analog_Gain = Blue_Analog_Gain) and (Red_Analog_Multiplier = Blue_Analog_Multiplier), the calculated or user−specified Red_Offset is used for both the red and blue channels.

The current values of the offsets can be read from the Green1_Offset, Red_Offset, Blue_Offset, and Green2_Offset registers. Writes to these registers when Manual_BLC is set change the offsets being used. In automatic BLC mode, writes to these registers are effective when manual mode is re−entered. In Manual_BLC mode, no sampling or adjusting takes place for any color.

Digital Black Level Calibration

Digital black level calibration is the final calculation applied to pixel data before it is output. It provides a precise black level to complement the coarser−grained analog black level calibration, and also corrects for black level shift introduced by digital gain. This correction applies to the active columns for all rows, including dark rows.

Test Patterns

The MT9P001 has the capability of injecting a number of test patterns into the top of the datapath to debug the digital logic. With one of the test patterns activated, any of the datapath functions can be enabled to exercise it in a deterministic fashion. Test patterns are enabled when Enable_Test_Pattern is set. Only one of the test patterns can be enabled at a given point in time by setting the Test_Pattern_Mode register according to Table 16. When test patterns are enabled the active area will receive the value specified by the selected test pattern and the dark pixels will receive the value in Test_Pattern_Green for green pixels, Test_Pattern_Blue for blue pixels, and Test_Pattern_Red for red pixels.

NOTE: **onsemi** recommends turning off black level calibration (BLC) when Test Pattern is enabled, others wise some of the test patterns will not be properly output.

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Table 16. TEST PATTERN MODES

Test_Pattern_Mode	Test Pattern Output
0	Color field (normal operation)
1	Horizontal gradient
2	Vertical gradient
3	Diagonal gradient
4	Classic test pattern
5	Walking 1s
6	Monochrome horizontal bars
7	Monochrome vertical bars
8	Vertical color bars

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Classic Test Pattern

When selected, a value from Test_Data will be sent through the digital pipeline instead of sampled data from the sensor. The value will alternate between Test_Data for even and odd columns.

Color Field

When selected, the value for each pixel is determined by its color. Green pixels will receive the value in Test_Pattern_Green, red pixels will receive the value in Test_Pattern_Red, and blue pixels will receive the value in Test_Pattern_Blue.

Vertical Color Bars

When selected, a typical color bar pattern will be sent through the digital pipeline.

Horizontal Gradient

When selected, a horizontal gradient will be produced based on a counter which increments on every active pixel.

Vertical Gradient

When selected, a vertical gradient will be produced based on a counter which increments on every active row.

Diagonal Gradient

When selected, a diagonal gradient will be produced based on the counter used by the horizontal and vertical gradients.

Walking 1s

When selected, a walking 1s pattern will be sent through the digital pipeline. The first value in each row is 1.

Monochrome Vertical Bars

When selected, vertical monochrome bars will be sent through the digital pipeline. The width of each bar can be set in Test_Pattern_Bar_Width and the intensity of each bar is set by Test_Pattern_Green for even bars and Test_Pattern_Blue for odd bars.

Monochrome Horizontal Bars

When selected, horizontal monochrome bars will be sent through the digital pipeline. The width of each bar can be set in Test_Pattern_Bar_Width and the intensity of each bar is set by Test_Pattern_Green for even bars and Test_Pattern_Blue for odd bars.

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SPECTRAL CHARACTERISTICS

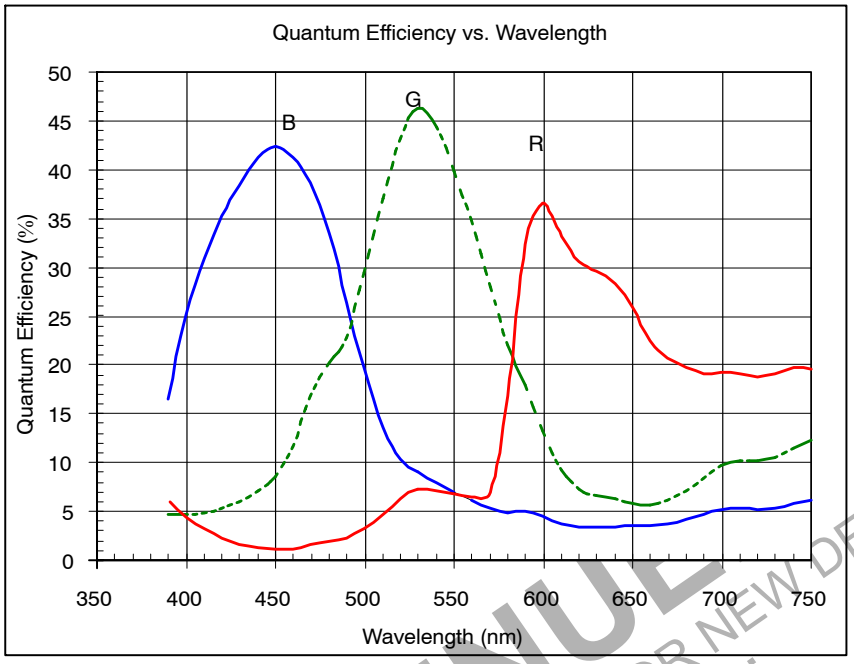


Figure 26. Typical Spectral Characteristics

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CRA vs. Image Height Plot

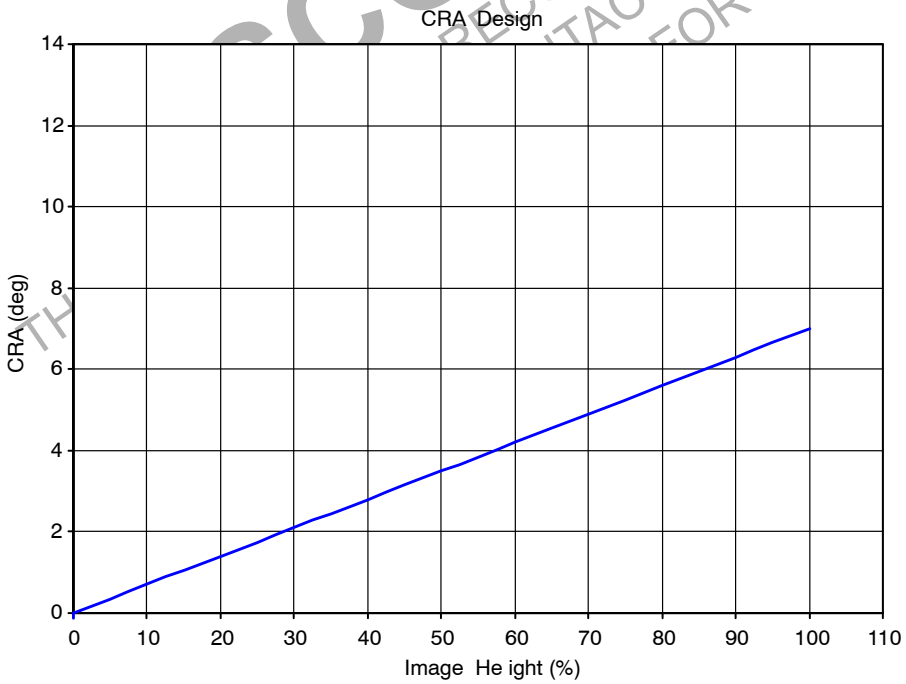


Figure 27. CRA vs. Image Height (7 deg)

Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.178	0.35
10	0.356	0.70
15	0.535	1.05
20	0.713	1.40
25	0.891	1.75
30	1.069	2.10
35	1.247	2.45
40	1.426	2.80
45	1.604	3.15
50	1.782	3.50
55	1.960	3.85
60	2.138	4.20
65	2.317	4.55
70	2.495	4.90
75	2.673	5.25
80	2.851	5.60
85	3.029	5.95
90	3.208	6.30
95	3.386	6.65
100	3.564	7.00

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ELECTRICAL SPECIFICATIONS

Two−Wire Serial Register Interface

The electrical characteristics of the two−wire serial register interface (SCLK, SDATA) are shown in Figure 29 and Table 17.

CRA vs. Image Height Plot

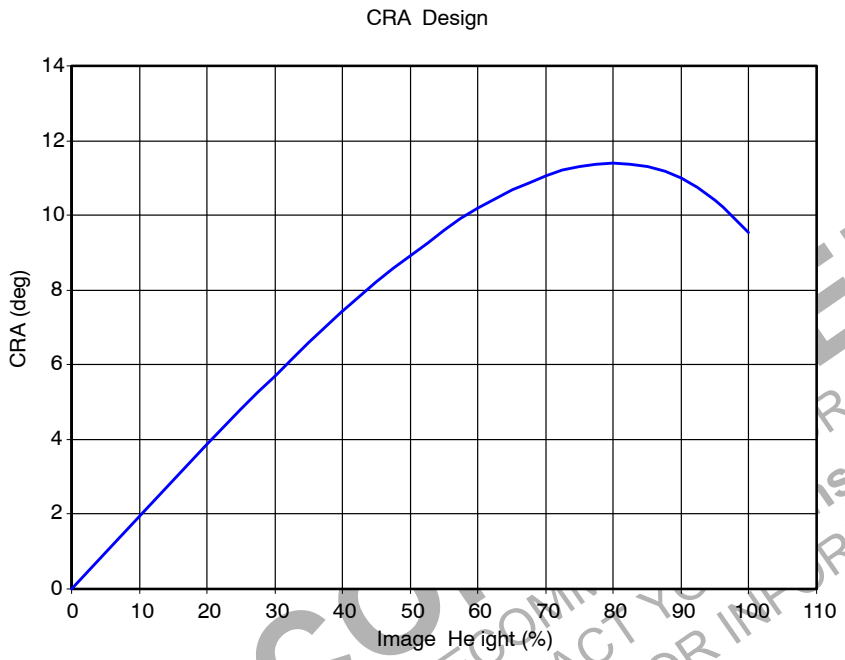


Figure 28. CRA vs. Image Height (11.4 deg)

Image Height (%)	Image Height (mm)	CRA (deg)
0	0	0
5	0.178	0.96
10	0.356	1.94
15	0.535	2.91
20	0.713	3.87
25	0.891	4.80
30	1.069	5.71
35	1.247	6.59
40	1.426	7.42
45	1.604	8.21
50	1.782	8.93
55	1.960	9.60
60	2.138	10.18
65	2.317	10.67
70	2.495	11.06
75	2.673	11.31
80	2.851	11.40
85	3.029	11.31
90	3.208	10.99
95	3.386	10.42
100	3.564	9.53

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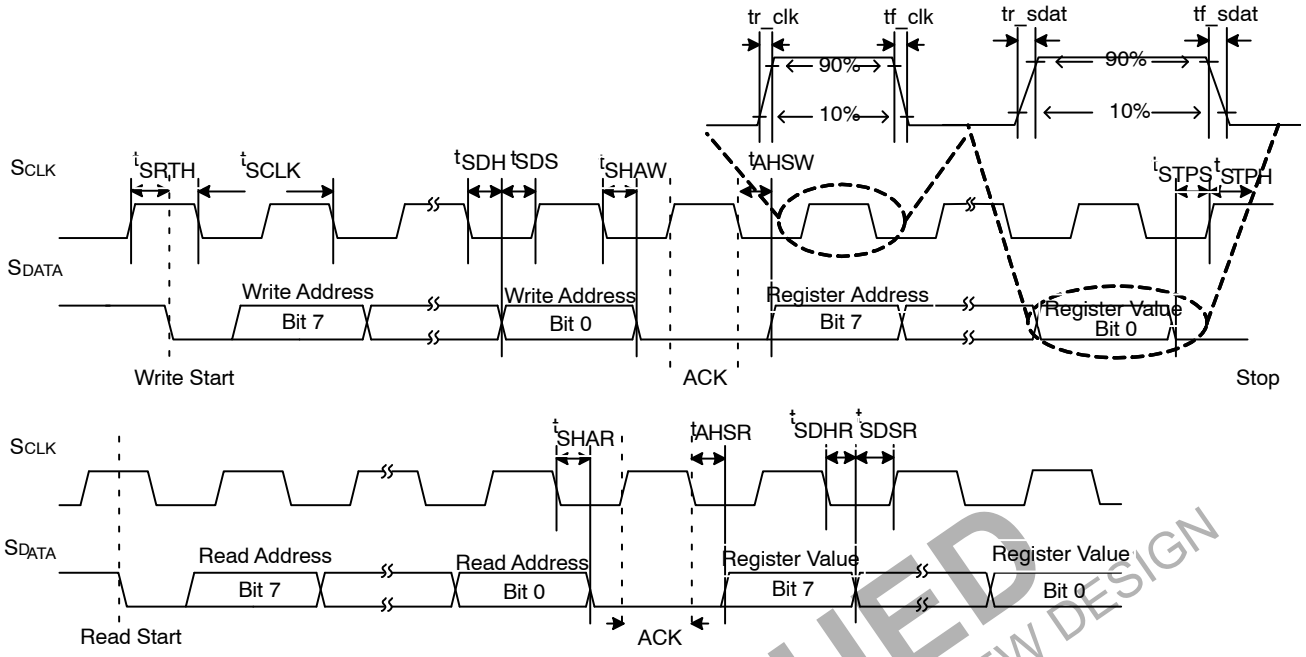


Figure 29. Two−Wire Serial Bus Timing Parameters

NOTE: Read sequence: For an 8−bit READ, read waveforms start after WRITE command and register address are issued.

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Table 17. TWO−WIRE SERIAL BUS CHARACTERISTICS

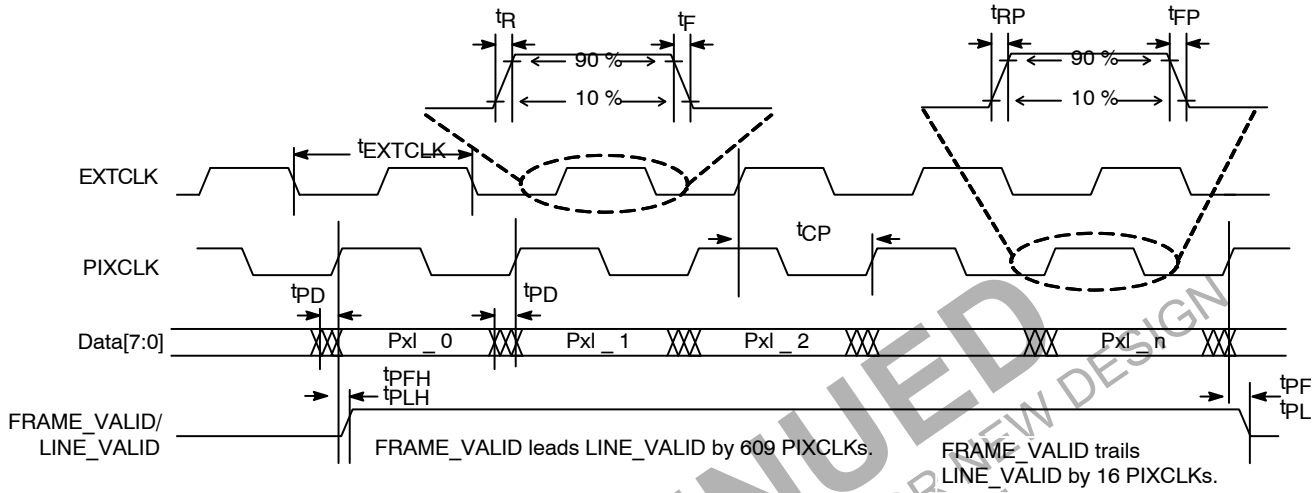
Symbol	Definition	Condition	Min	Typ	Max	Unit
^{f}SCLK	Serial interface input clock frequency	–	–	–	400	kHz
^{t}SCLK	Serial Input clock period	–	–	–	2.5	μsec
	SCLK duty cycle	–	40	50	60	%
tr_sclk	SCLK rise time		–	34	–	ns
tf_sclk	SCLK fall time		–	8	–	ns
tr_sdat	SDATA rise time		–	34	–	ns
tf_sdat	SDATA fall time		–	10	–	ns
^{t}SRTH	Start hold time	WRITE/READ	0	10	28	ns
^{t}SDH	SDATA hold	WRITE	0	0	0	ns
^{t}SDS	SDATA setup	WRITE	0	19.9	59.9	ns
^{t}SHAW	SDATA hold to ACK	WRITE	279	281	300	ns
^{t}AHSW	ACK hold to SDATA	WRITE	279	281	300	ns
^{t}STPS	Stop setup time	WRITE/READ	0	0	0	ns
^{t}STPH	Stop hold time	WRITE/READ	0	0	0	ns
^{t}SHAR	SDATA hold to ACK	READ	279	284	300	ns
^{t}AHSR	ACK hold to SDATA	READ	279	284	300	ns
^{t}SDHR	SDATA hold	READ	0	0	0	ns
^{t}SDSR	SDATA setup	READ	0	19.9	59.9	ns
C_{IN_SI}	Serial interface input pin capacitance	–	–	3.5	–	pF
C_{LOAD_SD}	SDATA max load capacitance	–	–	15	–	pF
R_{SD}	SDATA pull−up resistor	–	–	1.5	–	kΩ

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I/O Timing

By default, the MT9P001 launches pixel data, FV and LV with the rising edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV and LV using the falling edge of PIXCLK.

See Figure 30 and Table 18 for I/O timing (AC) characteristics.



*PLL disabled for t CP

Figure 30. I/O Timing Diagram

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Table 18. I/O TIMING CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
fEXTCLK1	Input clock frequency	PLL enabled	6	–	27	MHz
tEXTCLK1	Input clock period	PLL enabled	166	–	37	ns
fEXTCLK2	Input clock frequency	PLL disabled	6	–	96	MHz
tEXTCLK2	Input clock period	PLL disabled	125	–	10.4	ns
tR	Input clock rise time		0.03	–	1	V/ns
tF	Input clock fall time		0.03	–	1	V/ns
tRP	Pixclk rise time		0.03	–	1	V/ns
tFP	Pixclk fall time		0.03	–	1	V/ns
	Clock duty cycle		40	50	60	%
t(PIX JITTER)	Jitter on PIXCLK		–	–	1.03	ns
tJITTER1	Input clock jitter 48 MHz		–	300	–	ps
tJITTER2	Input clock jitter 96 MHz		–	220	–	ps
tCP	EXTCLK to PIXCLK propagation delay	Nominal voltages	11.5	17.7	19.1	ns
fPIXCLK	PIXCLK frequency	VDD_IO = 1.8 V	6	–	48	MHz
fPIXCLK	PIXCLK frequency	VDD_IO = 2.8 V	6	–	96	MHz
tPD	PIXCLK to data valid	Default	0.8	2.1	3.9	ns
tPFH	PIXCLK to FV HIGH	Default	2.8	4.3	5.9	ns
tPLH	PIXCLK to LV HIGH	Default	2.2	3.5	5.9	ns
tPFL	PIXCLK to FV LOW	Default	2.4	4.2	5.9	ns
tPLL	PIXCLK to LV LOW	Default	2.6	4.1	5.9	ns
CLOAD	Output load capacitance		–	<10	–	pF
CIN	Input pin capacitance		–	2.5	–	pF

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DC ELECTRICAL CHARACTERISTICS

The DC electrical characteristics are shown in Table 19.

Table 19. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		1.7	1.8	1.9	V
V_{DD_IO}	I/O digital voltage		1.7	1.8/2.8	3.1	V
V_{AA}	Analog voltage		2.6	2.8	3.1	V
V_{AA_PIX}	Pixel supply voltage		2.6	2.8	3.1	V
V_{DD_PLL}	PLL supply voltage		2.6	2.8	3.1	V
V_{IH}	Input HIGH voltage	V_{DD_IO} = 2.8 V	2	–	3.3	V
		V_{DD_IO} = 1.8 V	1.3	–	2.3	V
V_{IL}	Input LOW voltage	V_{DD_IO} = 2.8 V	–0.3	–	0.8	V
		V_{DD_IO} = 1.8 V	–0.3	–	0.5	V
I_{IN}	Input leakage current	No pull–up resistor; V_{IN} = V_{DD_IO} or D_{GND}	–	<10	–	µA
V_{OH}	Output HIGH voltage	V_{DD_IO} = 1.8 V	1.3	–	1.82	V
		V_{DD_IO} = 2.8 V	1.9	–	–	V
V_{OL}	Output LOW voltage	V_{DD_IO} = 2.8 V	0.16	–	0.35	V
		V_{DD_IO} = 2.8 V	–	–	0.6	V
I_{OH}	Output HIGH current	At specified V_{OH} = V_{DD_IO} – 400 mv at 1.7 V V_{DD_IO}	8.9	–	22.3	mA
I_{OL}	Output LOW current	At specified V_{OL} = 400mv at 1.7 V V_{DD_IO}	2.6	–	5.1	mA
I_{OZ}	Tri–state output leakage current	V_{IN} = V_{DD_IO} or GND	–	–	2	µA
I_{DD1}	Digital operating current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	–	28	35	mA
I_{DD_IO1}	I/O digital operating current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	–	38.6	50	mA
I_{AA1}	Analog operating current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	–	72	80	mA
I_{AA_PIX1}	Pixel supply current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	–	2.4	6	mA
I_{DD_PLL1}	PLL supply current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	–	5	6	mA
I_{DD2}	Digital operating current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	–	15	35	mA
I_{DD_IO2}	I/O digital operating current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	–	6.4	50	mA
I_{AA2}	Analog operating current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	–	69	80	mA
I_{AA_PIX2}	Pixel supply current	Parallel mode 96 MHz 4X binning nominal voltage, PLL Enabled	–	3.4	6	mA
I_{DD_PLL2}	PLL supply current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	–	5	6	mA
I_{STBY1}	Hard standby current PLL enabled	EXTCLK enabled	–	<500	–	µA
I_{STBY2}	Hard standby current PLL disabled	EXTCLK disabled	–	<50	–	µA

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Table 19. DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Definition	Condition	Min	Typ	Max	Unit
I_{STBY3}	Soft standby current PLL enabled	EXTCLK enabled (PLL enabled)	–	<500	–	μA
I_{STBY4}	Soft standby current PLL disabled	EXTCLK enabled (PLL disabled)	–	<500	–	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 20. POWER CONSUMPTION

Mode	Full Resolution (15 fps)	4X Binning	Unit
Streaming	381	262	mW

WARNING: Stresses greater than those listed in Table 21 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Table 21. ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Condition	Min	Max	Unit
V_{DD}_MAX	Core digital voltage		–0.3	1.9	V
V_{DD_IO}_MAX	I/O digital voltage		–0.3	3.1	V
V_{AA}_MAX	Analog voltage		–0.3	3.1	V
V_{AA_PIX}_MAX	Pixel supply voltage		–0.3	3.1	V
V_{DD_PLL}_MAX	PLL supply voltage		–0.3	3.1	V
V_{IN}_MAX	Input voltage		–0.3	3.4	V
I_{DD}_MAX	Digital operating current		–	35	mA
I_{DD_IO}_MAX	I/O digital operating current		–	100	mA
I_{AA}_MAX	Analog operating current		–	95	mA
I_{AA_PIX}_MAX	Pixel supply current		–	6	mA
I_{DD_PLL}_MAX	PLL supply current		–	6	mA
T_{OP}	Operating temperature	Measure at junction	–30	70	°C
T_{ST}	Storage temperature		–40	125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
7. To keep dark current and shot noise artifacts from impacting image quality, care should be taken to keep T_{OP} at a minimum.

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APPENDIX A – POWER–ON AND STANDBY TIMING

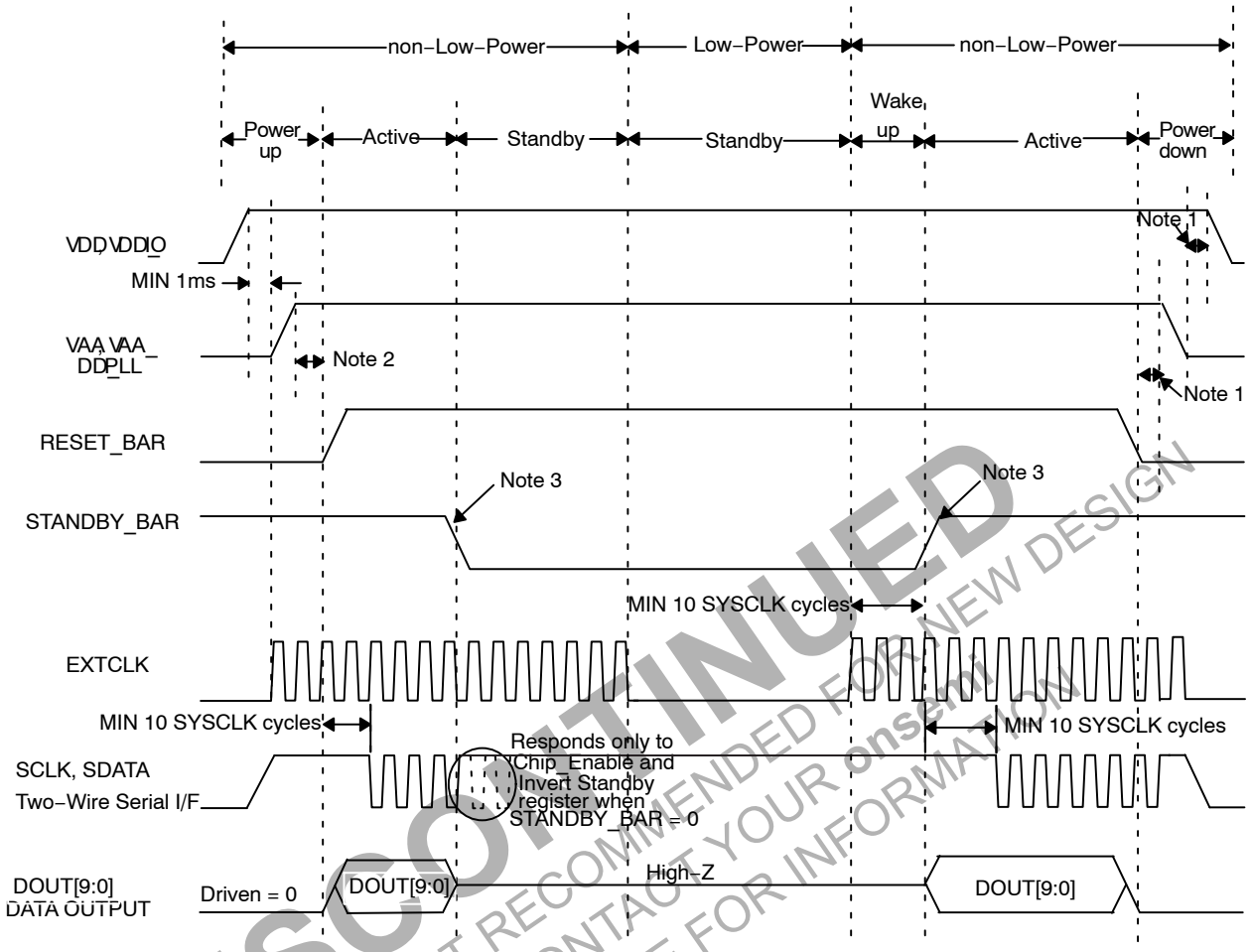


Figure 31. Power–On and Standby Timing Diagram

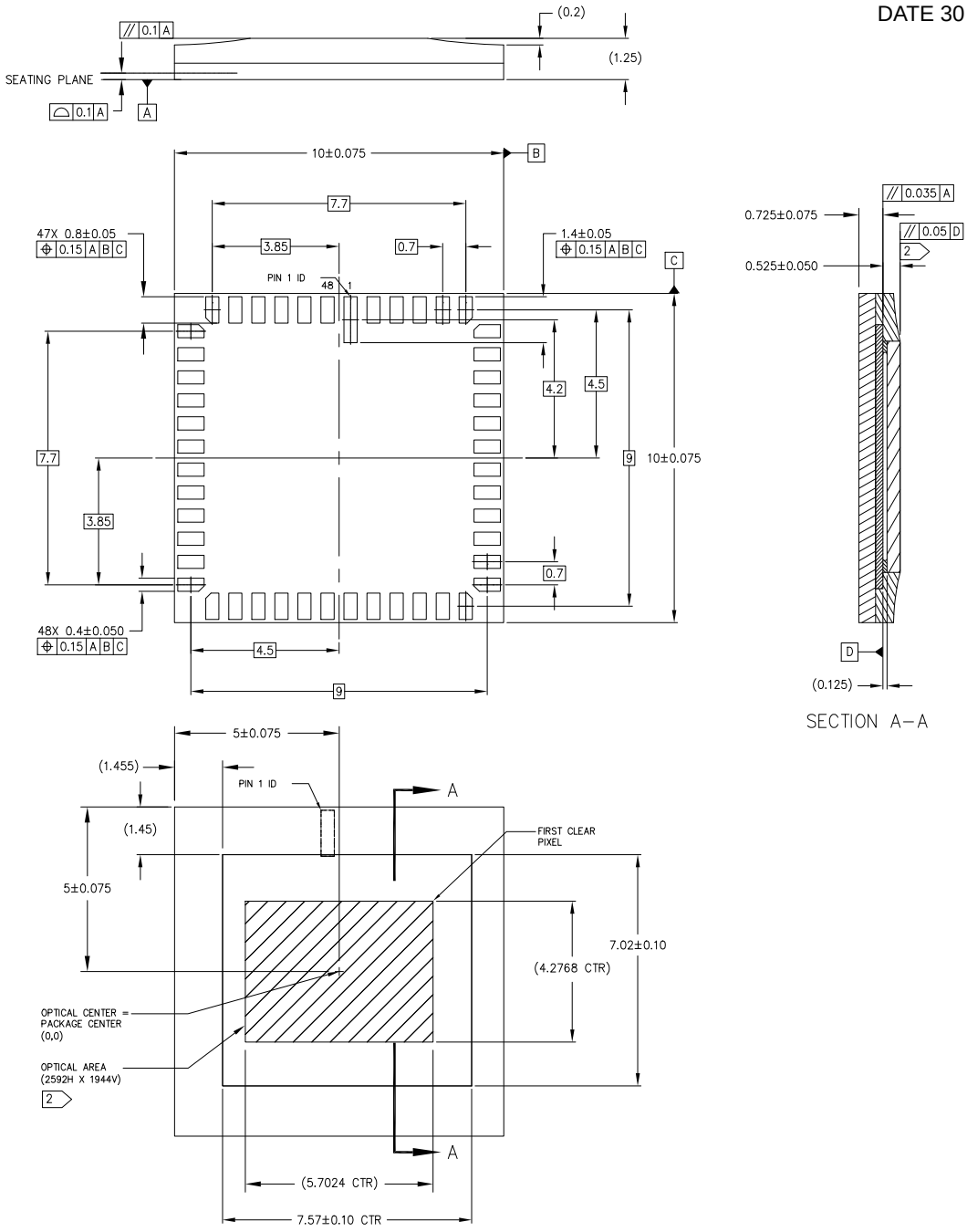
1. **onsemi** recommends 1 ms.
2. V_{AA} must stabilize before RESET_BAR goes HIGH.
3. **onsemi** recommends that the chip is paused (RESTART_Pause register) prior to STANDBY_BAR = 0 or restarted (Restart register) on resumption of operation.

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ILCC48 10x10
CASE 847AA
ISSUE O

DATE 30 DEC 2014



NOTES	
1	DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.
2	MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°. MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SUBSTRATE PLANE A : 35 MICRONS. MAXIMUM TILT OF COVER GLASS RELATIVE TO OPTICAL AREA PLANE D : 50 MICRONS.

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