M24C32-A125

Datasheet

Automotive 32-Kbit serial I²C bus EEPROM with 1 MHz clock



SO8N (MN)

150 mil width



TSSOP8

169 mil width



WFDFPN8 (MF)

DFN8 2 x 3 mm

Product status
M24C32-A125

Product label
LONGEVITY 15 YEARS COMMITMENT

Features

Grade

- AEC-Q100 qualified

I²C interface

- Compatible with all I²C bus modes
  - 1 MHz (Fast-mode Plus)
  - 400 kHz (Fast-mode)
  - 100 kHz (Standard-mode)

Memory

- 32 Kbit (4 Kbyte) of EEPROM
- Page size: 32 byte
- Additional 32-byte lockable identification page

Supply voltage

- Voltage range: 1.7 V to 5.5 V

Temperature

- Operating temperature range: -40 °C to +125 °C

Fast write cycle time

- Byte and page write within 4 ms (typically 3.1 ms)

Write cycle performance

- 4 million write cycles at 25 °C
- 1.2 million write cycles at 85 °C
- 600 k write cycles at 125 °C

Data retention performance

- 50 years at 125 °C
- 100 years at 25 °C

Advanced features

- Enhanced ESD/latch-up protection
- ESD protection (human body model) 4000 V
- Schmitt trigger inputs for noise filtering
- Hardware write protection of the whole memory array
- Random and sequential read modes

Package

- SO8N, TSSOP8, and UFDFPN8 (RoHS-compliant and Halogen-free)

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1 Description

The M24C32-A125 is a 32-Kbit serial EEPROM automotive grade device operating up to 125 °C. The M24C32-A125 is compliant with the very high level of reliability defined by the automotive standard AEC-Q100 grade 1.

The device is accessed by a simple serial I^2C compatible interface running up to 1 MHz.

The memory array is based on advanced true EEPROM technology (electrically erasable programmable memory). The M24C32-A125 is byte-alterable memories (4096 K × 8 bits) organized as 128 pages of 32 byte in which the data integrity is significantly improved with an embedded error correction code logic.

The M24C32-A125 offers an additional identification page (32 byte) in which the ST device identification can be read. This page can also be used to store sensitive application parameters which can be later permanently locked in read-only mode.

Figure 1. Logic diagram

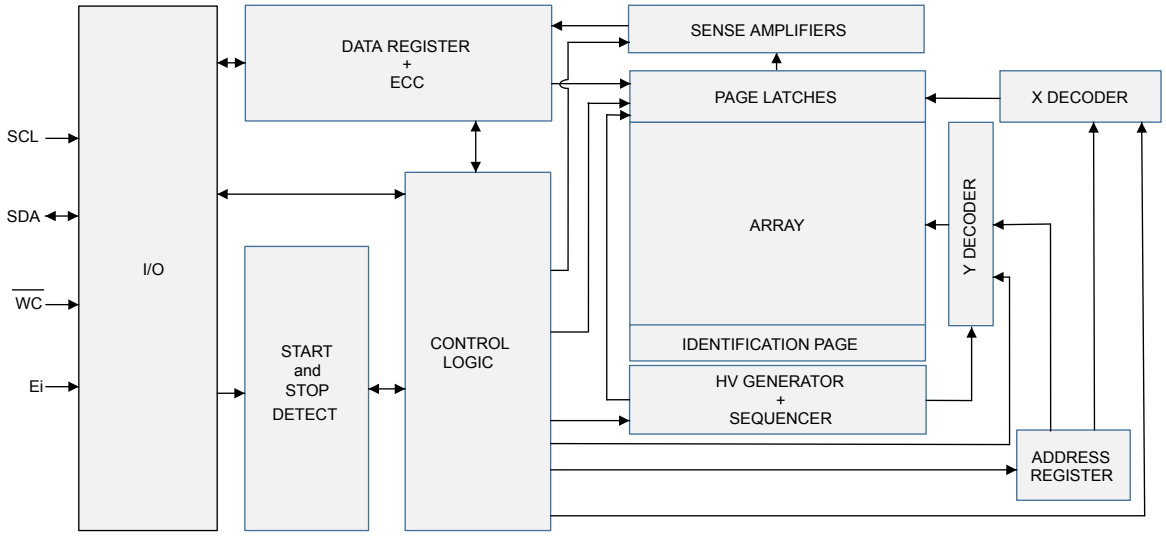
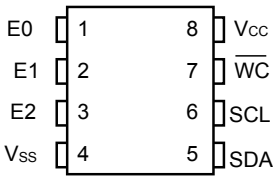


Table 1. Signal names

Signal name	Function	Direction
E2, E1, E0	Chip enable	Input
SDA	Serial data	I/O
SCL	Serial clock	Input
$\overline{WC}$	Write control	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

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Figure 2. 8-pin package connections



DT01845fV1

1. See Section 9: Package information for package dimensions, and how to identify pin 1.

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2 Signal description

2.1 Serial clock (SCL)

The signal applied on this input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

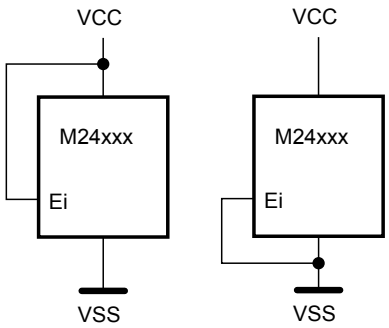
2.2 Serial data (SDA)

SDA is an input/output used to transfer data in or out of the device. SDA(out) is an open drain output that may be wired-AND with other open drain or open collector signals on the bus. A pull up resistor must be connected between SDA and V_{CC} (Figure 10 and Figure 11 indicate how to calculate the value of the pull-up resistor).

2.3 Chip Enable (E2, E1, E0)

(E2,E1,E0) input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code (see Table 2). These inputs must be tied to V_{CC} or V_{SS}, as shown in Figure 3. When not connected (left floating), these inputs are read as low (0).

Figure 3. Device select code



2.4 Write control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when write control ($\overline{WC}$) is driven high. Write operations are enabled when write control ($\overline{WC}$) is either driven low or left floating.

When write control ($\overline{WC}$) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

V_{CC} is the supply voltage pin.

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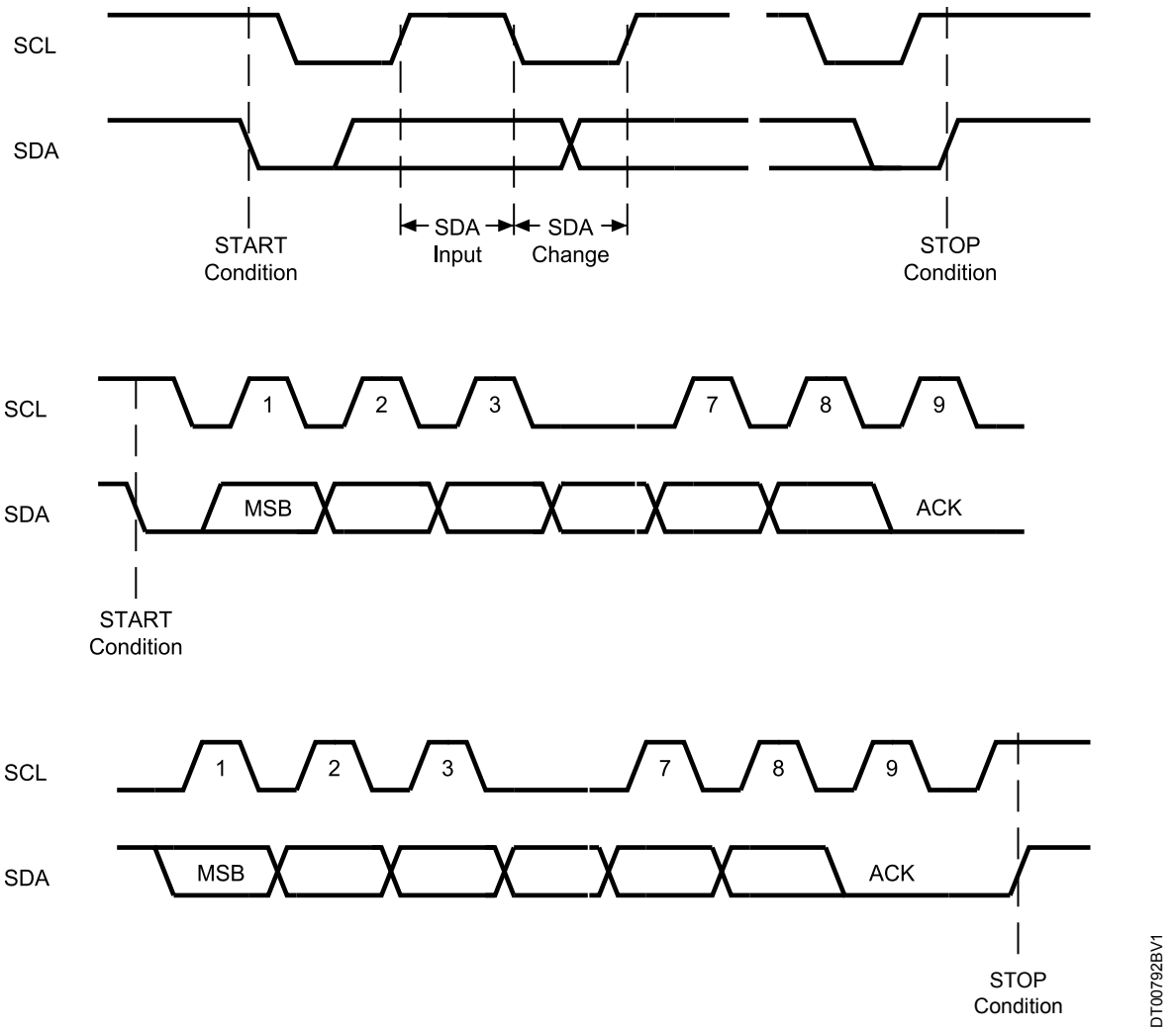
3 Device operation

The device supports the I²C protocol (see Figure 4).

The I²C bus is controlled by the bus master and the device is always a slave in all communications.

The device (bus master or a slave) that sends data on to the bus is defined as a transmitter; the device (bus master or a slave) is defined as a receiver when reading the data.

Figure 4. I²C bus protocol



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3.1 Start condition

Start is identified by a falling edge of serial data (SDA) while serial clock (SCL) is stable in the high state. A start condition must precede any data transfer instruction. The device continuously monitors (except during a write cycle) serial data (SDA) and serial clock (SCL) for a start condition.

3.2 Stop condition

Stop is identified by a rising edge of serial data (SDA) while serial clock (SCL) is stable in the high state. A stop condition terminates communication between the device and the bus master.

A stop condition at the end of a write instruction triggers the internal write cycle.

3.3 Data input

During data input, the device samples serial data (SDA) on the rising edge of serial clock (SCL). For correct device operation, serial data (SDA) must be stable during the rising edge of serial clock (SCL), and the serial data (SDA) signal must change only when serial clock (SCL) is driven low.

3.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases serial data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls serial data (SDA) low to acknowledge the receipt of the eight data bits.

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3.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a start condition. Following this, the bus master sends the device select code, as shown in Table 2.

The device select code consists of a 4-bit device type identifier and a 3-bit chip enable address (E2, E1, E0). A device select code handling any value other than 1010b (to select the memory) or 1011b (to select the identification page) is not acknowledged by the memory device.

Up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on the chip enable (E2, E1, E0) inputs. When the device select code is received, the memory device only responds if the chip enable address is the same as the value decoded on the E2, E1, E0 inputs.

The 8th bit is the read/write bit ($\overline{RW}$). This bit is set to 1 for read and 0 for write operations.

Table 2. Device select code

	Device type identifier (1)				Chip Enable address (2)			$\overline{RW}$
-	b7	b6	b5	b4	b3	b2	b1	b0
When accessing the memory	1	0	1	0	E2	E1	E0	$\overline{RW}$
When accessing the Identification page	1	0	1	1	E2	E1	E0	$\overline{RW}$

1. *The most significant bit, b7, is sent first.*
2. *E0, E1 and E2 bits are compared with the value read on input pins E0,E1,E2.*

If a match occurs on the device select code, the corresponding memory device gives an acknowledgement on serial data (SDA) during the 9th bit time. If the memory device does not match the device select code, it deselects itself from the bus, and goes into standby mode.

Once the memory device has acknowledged the device select code (Table 2), the memory device waits for the master to send two address bytes (most significant address byte sent first, followed by the least significant address byte (Table 3). The memory device responds to each address byte with an acknowledge bit.

Table 3. Significant bits within the two address bytes

		Memory		Identification page			
		Random Address Read	Write	Read identification page	Write identification page	Lock identification page	Read lock status
Most significant address byte	b15	X	X	X	X	X	X
	b14	X	X	X	X	X	X
	b13	X	X	X	X	X	X
	b12	X	X	X	X	X	X
	b11	A11	A11	X	X	X	X
	b10	A10	A10	X	0	1	0
	b9	A9	A9	X	X	X	X
	b8	A8	A8	X	X	X	X
Least significant address byte	b7	A7	A7	X	X	X	X
	b6	A6	A6	X	X	X	X
	b5	A5	A5	X	X	X	X
	b4	A4	A4	A4	A4	X	X
	b3	A3	A3	A3	A3	X	X
	b2	A2	A2	A2	A2	X	X
	b1	A1	A1	A1	A1	X	X
	b0	A0	A0	A0	A0	X	X

Note: A: significant address bit.
X: bit is don't Care.

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3.6 Identification page

The M24C32-A125 offers an identification page (32 byte) in addition to the 32 Kbit memory.

The identification page contains two fields:

- Device identification code: the first three bytes are programmed by STMicroelectronics with the device identification code, as shown in Table 4.
- Application parameters: the bytes after the device identification code are available for application specific data.

Note: If the end application does not need to read the device identification code, this field can be overwritten and used to store application-specific data. Once the application-specific data are written in the identification page, the whole identification page should be permanently locked in read-only mode.

The instructions read, write and lock identification page are detailed in Section 4: Instructions.

Table 4. Device identification code

Address in identification page	Content	Value
00h	ST manufacturer code	20h
01h	I^2C family code	E0h
02h	Memory density code	0Ch (32 Kbit)

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4 Instructions

4.1 Write operations

For a write operation, the bus master sends a start condition followed by a device select code with the R/W bit reset to 0. The device acknowledges this, as shown in Figure 5, and waits for the master to send two address bytes (most significant address byte sent first, followed by the least significant address byte (Table 3). The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a stop condition immediately after a data byte ACK bit (in the "10^{th} bit" time slot), either at the end of a byte write or a page write, the internal write cycle t_W is then triggered. A stop condition at any other time slot does not trigger the internal write cycle.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests.

After the successful completion of an internal write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

If the Write control input ($\overline{WC}$) is driven high, the write instruction is not executed and the accompanying data bytes are not acknowledged, as shown in Figure 6.

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4.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is write-protected, by write control ($\overline{WC}$) being driven high, the device replies with NoACK, and the location is not modified (see Figure 6). If, instead, the addressed location is not write-protected, the device replies with ACK. The bus master terminates the transfer by generating a stop condition, as shown in Figure 5.

Figure 5. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



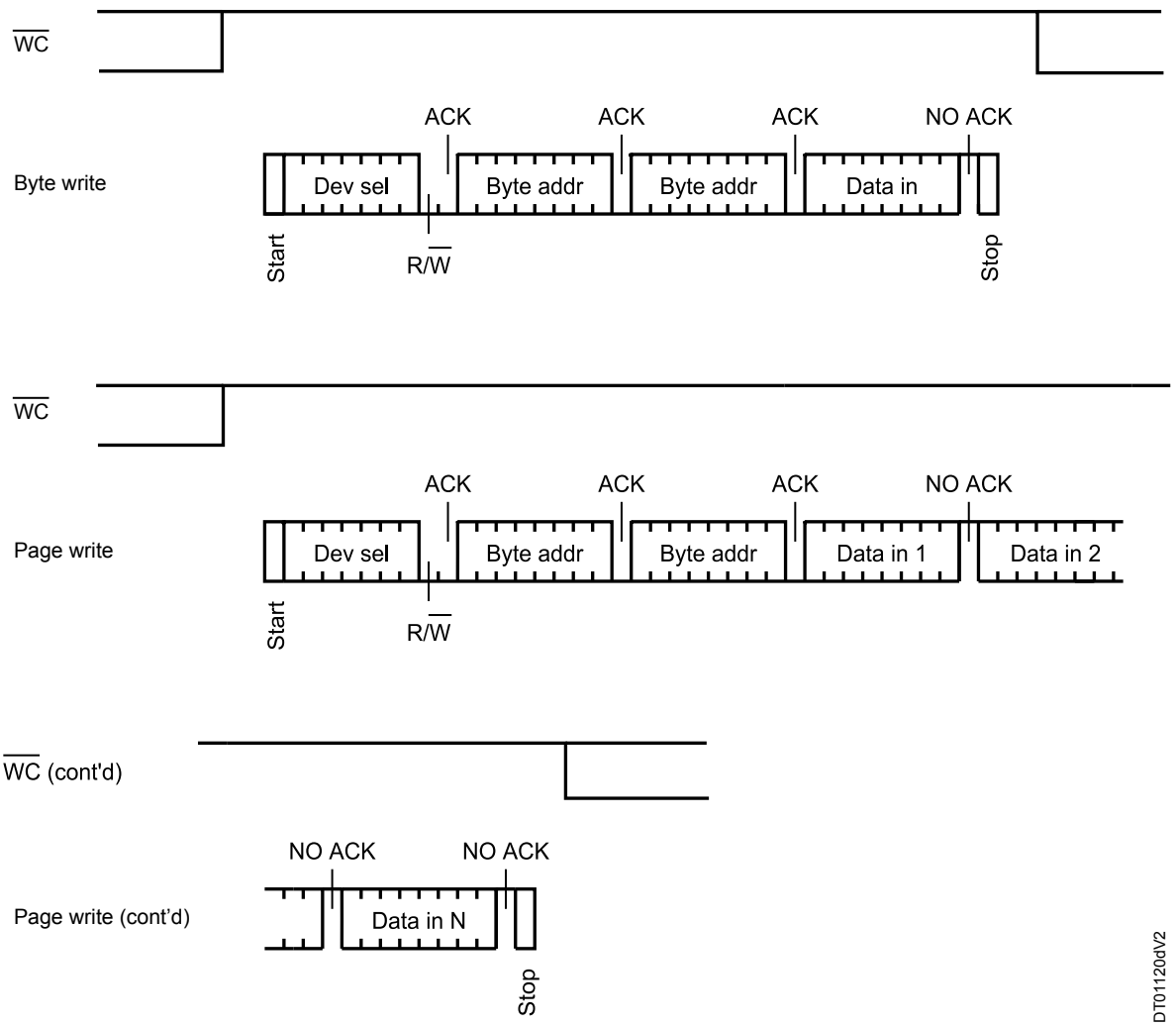
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4.1.2 Page Write

The page write mode allows up to N (N is the number of bytes in a page) bytes to be written in a single write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A15/A5, are the same. If more bytes are sent than will fit up to the end of the page, a condition known as “roll-over” occurs. In case of roll-over, the first bytes of the page are overwritten.

The bus master sends from 1 to N bytes of data, each of which is acknowledged by the device if write control ($\overline{WC}$) is low. If write control ($\overline{WC}$) is high, the contents of the addressed memory location are not modified, and each data byte received by the device is not acknowledged, as shown in Figure 6. After each byte is transferred, the internal byte address counter is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 6. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



4.1.3 Write identification page

The identification page (32 byte) is an additional page which can be written and (later) permanently locked in read-only mode. It is written by issuing the write identification page instruction. This instruction uses the same protocol and format as page write (into memory array), except for the following differences:

- Device type identifier = 1011b
- Most significant address bits A15/A5 are don't care, except for address bit A10 which must be “0”. Least significant address bits A4/A0 define the byte location inside the identification page.

If the identification page is locked, the data bytes transferred during the write identification page instruction are not acknowledged (NoACK).

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4.1.4 Lock identification page

The lock identification page instruction (lock ID) permanently locks the identification page in read-only mode. The lock ID instruction is similar to byte write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be ‘1’; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

4.1.5 Minimizing write delays by polling on ACK

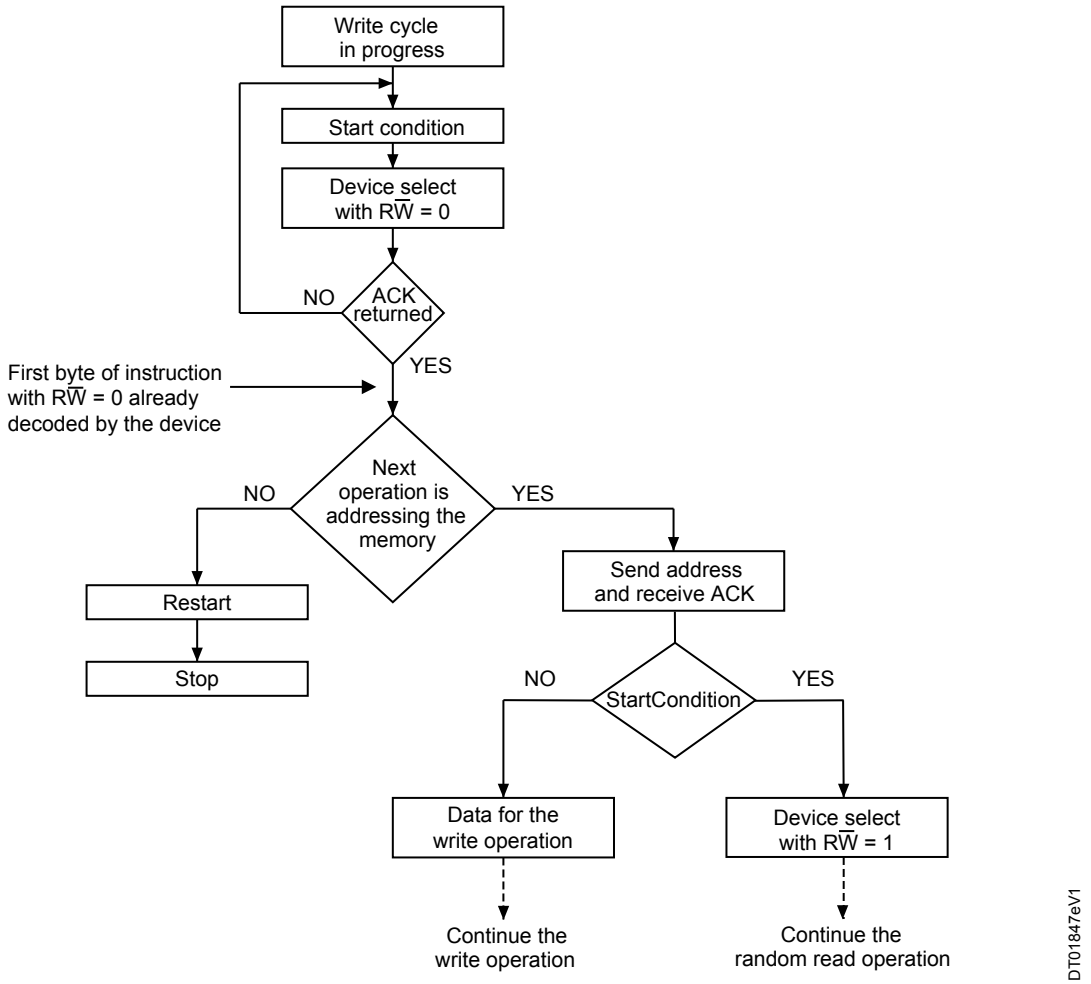
The maximum write time (t_w) is shown in AC characteristics of Table 11 and Table 12 in Section 8: DC and AC parameters, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in Figure 7, is:

- Initial condition: a write cycle is in progress.
- Step 1: the bus master issues a start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal write cycle, noACK is returned and the bus master goes back to step 1. If the device has terminated the internal write cycle, it responds with an ACK, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during step 1).

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Figure 7. Write cycle polling flowchart using ACK



1. *The seven most significant bits of the device select code of a random read (bottom right box in the Figure 7) must be identical to the seven most significant bits of the device select code of the write (polling instruction in the Figure 7).*

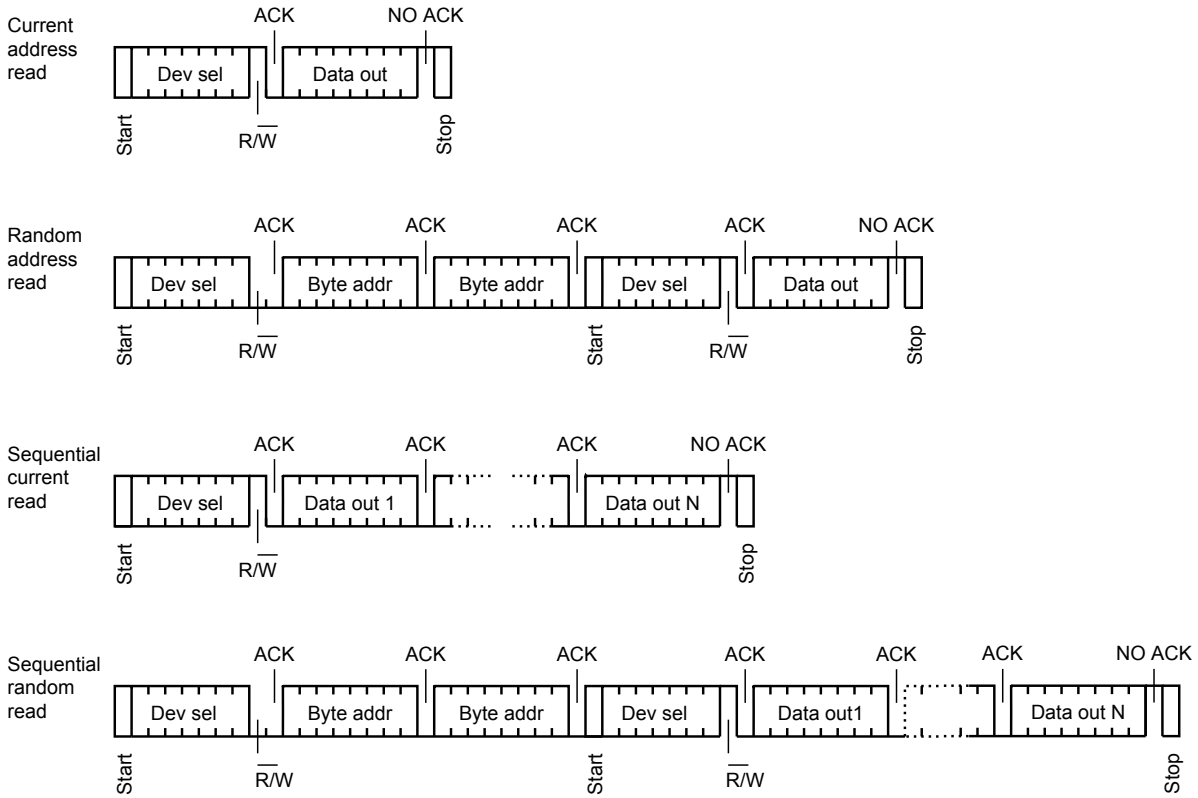
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4.2 Read operations

Read operations are performed independently of the state of the write control ($\overline{WC}$) signal.

After the successful completion of a read operation, the device internal address counter is incremented by one, to point to the next byte address.

Figure 8. Read mode sequences



Note: The seven most significant bits of the first device select code of a random read must be identical to the seven most significant bits of the device select code of the write.

4.2.1 Random address read

The random address read is a sequence composed of a truncated write sequence (to define a new address pointer value, see Table 3) followed by a current read.

The random address read sequence is therefore the sum of [start + device select code with R$\overline{W}$=0 + two address bytes] (without stop condition, as shown in Figure 8)] and [start condition + device select code with R$\overline{W}$=1]. The memory device acknowledges the sequence and then outputs the contents of the addressed byte. To terminate the data transfer, the bus master does not acknowledge the last data byte and then issues a stop condition.

4.2.2 Current address read

For the current address read operation, following a start condition, the bus master only sends a device select code with the R/W bit set to 1. The device acknowledges this, and outputs the byte pointed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a stop condition, as shown in Figure 8, without acknowledging the byte.

Note that the address counter value is defined by instructions accessing either the memory or the identification page. When accessing the identification page, the address counter value is loaded with the identification page byte location, when accessing the memory, it is safer to always use the random address read instruction (this instruction loads the address counter with the byte location to read in the memory) instead of the current address read instruction.

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4.2.3 Sequential read

A sequential read can be used after a current address read or a random address read.

After a read instruction, the device can continue to output the next byte(s) in sequence if the bus master sends additional clock pulses and if the bus master does acknowledge each transmitted data byte. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a stop condition, as shown in Figure 8.

The sequential read is controlled with the device internal address counter which is automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

4.2.4 Read identification page

The identification page can be read by issuing a read identification page instruction. This instruction uses the same protocol and format as the random address read (from memory array) with device type identifier defined as 1011b. The most significant address bits A15/A5 are don't care and the least significant address bits A4/A0 define the byte location inside the identification page. The number of bytes to read in the ID page must not exceed the page boundary.

4.2.5 Read the lock status

The locked/unlocked status of the identification page can be checked by transmitting a specific truncated command [identification page write instruction + one data byte] to the device. The device returns an acknowledge bit after the data byte if the identification page is unlocked, otherwise a NoACK bit if the identification page is locked.

Right after this, it is recommended to transmit to the device a start condition followed by a stop condition, so that:

- Start: the truncated command is not executed because the start condition resets the device internal logic,
- Stop: the device is then set back into standby mode by the stop condition.

4.2.6 Acknowledge in read mode

For all read instructions, the device waits, after each byte sent out, for an acknowledgement during the 9th bit time. If the bus master does not send the ACK (the master drives SDA high during the 9th bit time), the device terminates the data transfer and enters its standby mode.

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5 Application design recommendations

5.1 Supply voltage

5.1.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

5.1.2 Power-up conditions

When the power supply is turned on, the V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage.

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} reaches the internal threshold voltage.

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- in the standby power mode
- deselected

As soon as the V_{CC} voltage has reached a stable value within the [V_{CC}(min), V_{CC}(max)] range, the device is ready for operation.

5.1.3 Power-down

During power-down (continuous decrease in the V_{CC} supply voltage below the minimum V_{CC} operating voltage, the device must be in standby power mode (that is after a stop condition or after the completion of the write cycle t_W if an internal write cycle is in progress).

5.2 Cycling with error correction code (ECC)

The error correction code (ECC) is an internal logic function which is transparent for the I^2C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes (a group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer). Inside a group, if a single bit out of the four bytes happens to be erroneous during a read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group (a group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer). As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the four byte of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in Table 6.

Example 1: maximum cycling limit reached with 1 million cycles per byte

Each byte of a group can be equally cycled 1 million times (at 25 °C) so that the group cycling budget is 4 million cycles.

Example 2: maximum cycling limit reached with unequal byte cycling

Inside a group, byte0 can be cycled 2 million times, byte1 can be cycled 1 million times, byte2 and byte3 can be cycled 500,000 times, so that the group cycling budget is 4 million cycles.

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6 Delivery state

The device is delivered as follows:

- The memory array is set to all 1s (each byte = FFh).
- Identification page: the first three bytes define the device identification code (value defined in Table 4). The content of the following bytes is "Don't Care".

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7 Maximum rating

Stressing the device outside the ratings listed in Table 5 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
-	Ambient operating temperature	-40	130	°C
T_{STG}	Storage temperature	-65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
V_{IO}	Input or output range	-0.50	6.5	V
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{CC}	Supply voltage	-0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body model) (2)	-	4000	V

1. *Compliant with JEDEC Standard J-STD-020 (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions of Hazardous Substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on pin pairs, according to AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001, C1=100 pF, R1=1500 Ω, R2=500 Ω).*

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8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 6. Cycling performance by groups of four bytes

Symbol	Parameter	Test condition	Min.	Max.	Unit
Ncycle	Write cycle endurance (1)	TA ≤ 25 °C, 1.7 V < V_{CC} < 5.5 V	-	4,000,000	Write cycle (2)
		TA = 85 °C, 1.7 V < V_{CC} < 5.5 V	-	1,200,000	
		TA = 125 °C, 1.7 V < V_{CC} < 5.5 V	-	600,000	

1. *The write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer, or for the status register byte (refer also to Section 5.2: Cycling with error correction code (ECC)). The write cycle endurance is defined by characterization and qualification.*
2. *A write cycle is executed when either a page write, a byte write, a write identification page or a lock identification page instruction is decoded. When using those write instructions, refer also to Section 5.2: Cycling with error correction code (ECC).*

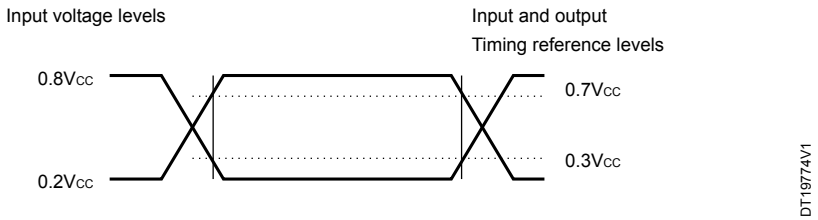
Table 7. Operating conditions (voltage range R, device grade 3)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	–40	125	°C

Table 8. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	-	100	pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 9. AC measurement I/O waveform



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Table 9. Input parameters

Symbol	Parameter (1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	-	8	pF
C_{IN}	Input capacitance (other pins)	-	-	6	pF
Z_L	Input impedance (E2, E1, E0, $\overline{WC}$) (2)	$V_{IN} < 0.3\ V_{CC}$	30	-	kΩ
Z_H		$V_{IN} > 0.7\ V_{CC}$	500	-	kΩ

1. *Evaluated by characterization - not tested in production.*
2. *E2, E1, E0 input impedance when the memory is selected (after a Start condition).*

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Table 10. DC characteristics

Symbol	Parameter	Test conditions (in addition to those in Table 7 and Table 8)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	f_C = 400 kHz, V_{CC} = 5.5 V	-	2	mA
		f_C = 400 kHz, V_{CC} = 2.5 V	-	2	
		f_C = 400 kHz, V_{CC} = 1.7 V	-	1	
		f_C = 1 MHz, V_{CC} = 5.5 V	-	2	
		f_C = 1 MHz, V_{CC} = 2.5 V	-	2	
		f_C = 1 MHz, V_{CC} = 1.7 V	-	2	
I_{CC0}	Supply current (Write)	During t_W	-	2	mA
I_{CC1}	Standby supply current	Device not selected(1), t° = 85 °C, $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.7 V	-	1	µA
		Device not selected(1), t° = 85 °C, $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V	-	2	
		Device not selected(1), t° = 85 °C, $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V	-	3	
		Device not selected(1), t° = 125 °C, $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.7 V	-	15	µA
		Device not selected(1), t° = 125 °C, $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V	-	15	
		Device not selected(1), t° = 125 °C, $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V	-	20	
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	-	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.7 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$, E2, E1, E0)	-	0.7 V_{CC}	V_{CC} +0.6	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V
		I_{OL} = 1 mA, V_{CC} = 1.7 V	-	0.3	
V_{RES} (2)	Internal reset threshold voltage	-	0.5	1.5	V

1. *The device is not selected after power-up, after a read instruction (after the stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write instruction).*
2. *Evaluated by characterization - not tested in production.*

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Table 11. 400 kHz AC characteristics

Symbol	Alt.	Parameter [1]	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2} [2]	t_F	SDA (out) fall time [3]	20	120	ns
t_{XH1XH2}	t_R	Input signal rise time	- [4]	- [4]	ns
t_{XL1XL2}	t_F	Input signal fall time	- [4]	- [4]	ns
t_{DXCX}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} [5]	t_{DH}	Data out hold time	100	-	ns
t_{CLQV} [6]	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_{WLDL} [2][7]	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	µs
t_W [2][8]	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Write time	-	4	ms
t_{NS} [2]	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	80	ns

1. *Test conditions (in addition to those in Table 7 and Table 8).*
2. *Evaluated by characterization - not tested in production.*
3. *With C_L = 10 pF.*
4. *There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.*
5. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.*
6. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3V_{CC} or 0.7V_{CC}, assuming that R_{bus} × C_{bus} time constant is within the values specified in Figure 10.*
7. *$\overline{WC}$ =0 set up time condition to enable the execution of a WRITE command.*
8. *$\overline{WC}$=0 hold time condition to enable the execution of a WRITE command.*

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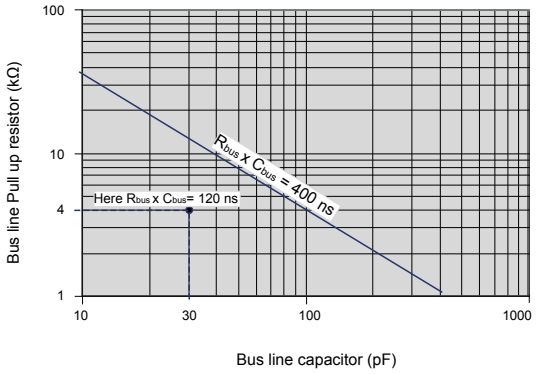
Table 12. 1 MHz AC characteristics

Symbol	Alt.	Parameter (1)	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	400	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(2)	(2)	ns
t_{XL1XL2}	t_F	Input signal fall time	(2)	(2)	ns
t_{QL1QL2} (3)	t_F	SDA (out) fall time	-	120	ns
t_{DXCX}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (4)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV} (5)	t_{AA}	Clock low to next data valid (access time)	-	450	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_{WLDL} (6) (3)	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	µs
t_{DHWH} (7) (3)	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Write time	-	4	ms
t_{NS} (3)	-	Pulse width ignored (input filter on SCL and SDA)	-	80	ns

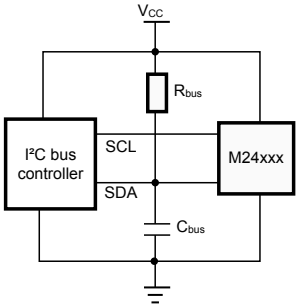
1. *Test conditions (in addition to those in Table 7 and Table 8).*
2. *There is no min. or max. values for the input signal rise and fall times. However, it is recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 120 ns when f_C < 1 MHz.*
3. *Evaluated by characterization - not tested in production.*
4. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.*
5. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the Rbus × Cbus time constant is within the values specified in Figure 11.*
6. *$\overline{WC}$ =0 set up time condition to enable the execution of a WRITE command.*
7. *$\overline{WC}$ =0 hold time condition to enable the execution of a WRITE command.*

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Figure 10. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz

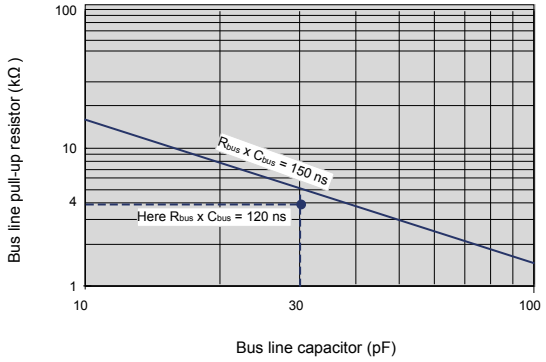


The R_{bus} x C_{bus} time constant must be below the 400 ns time constant line represented on the left

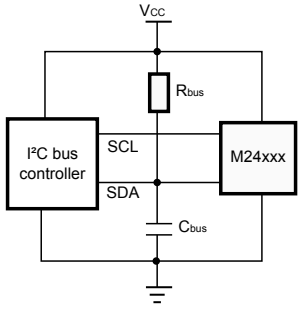


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Figure 11. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 1 MHz



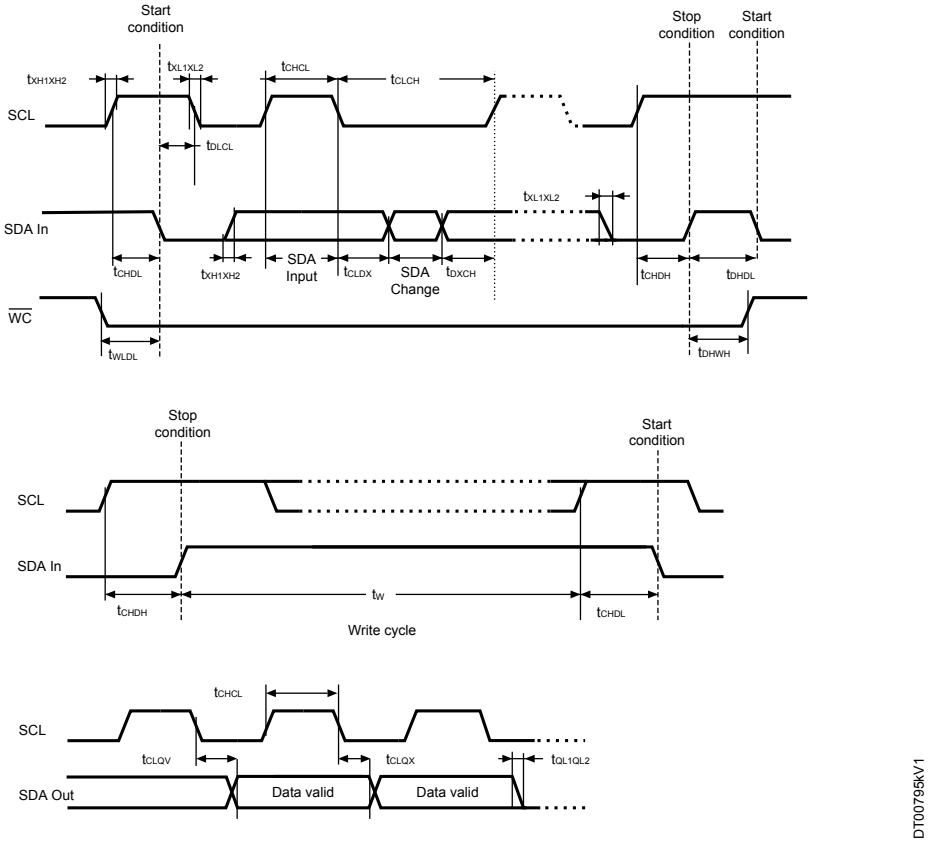
The R_{bus} x C_{bus} time constant must be below the 150 ns time constant line represented on the left



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Figure 12. AC waveforms



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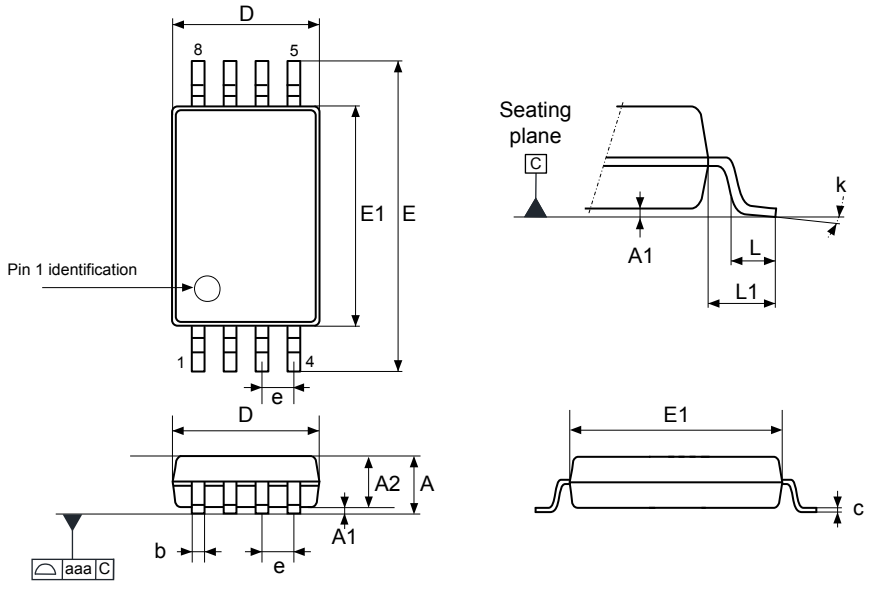
9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 TSSOP8 package information

This TSSOP is an 8-lead, 3 x 6.4 mm, 0.65 mm pitch, thin shrink small outline package.

Figure 13. TSSOP8 – Outline



1. *Drawing is not to scale.*

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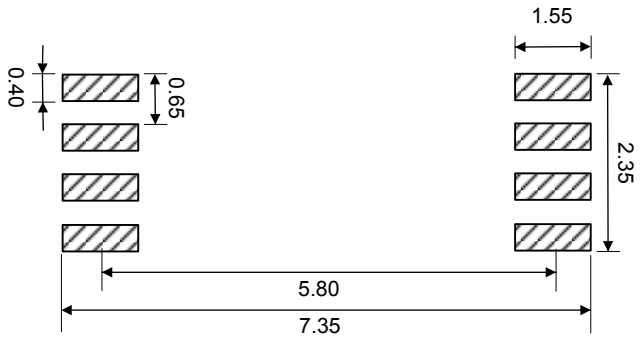
Table 13. TSSOP8 - Mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D[2]	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1[3]	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.*
3. *Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of the mold flash, tie bar burrs, gate burrs, and interleads flash, but including any mismatch between the top and bottom of the plastic body. The measurement side for the mold flash, protrusions, or gate burrs is the bottom side.

Figure 14. TSSOP8 – Footprint example



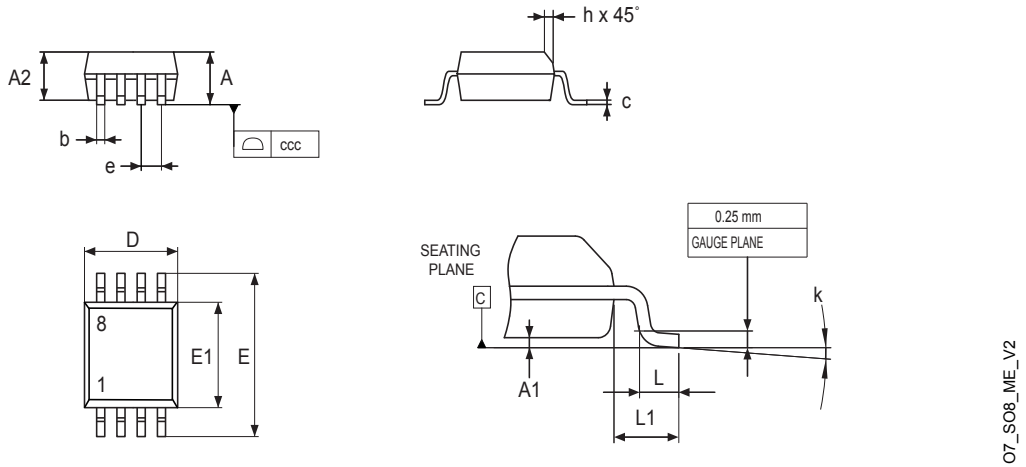
1. *Dimensions are expressed in millimeters.*

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9.2 SO8N package information

This SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mil body width package.

Figure 15. SO8N - Outline



1. *Drawing is not to scale.*

Table 14. SO8N - Mechanical data

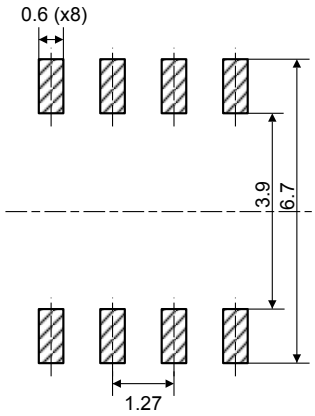
Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D[2]	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1[3]	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side*
3. *Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interleads flash, but including any mismatch between the top and bottom of the plastic body. The measurement side for mold flash, protusions, or gate burrs is the bottom side.

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Figure 16. SO8N - Footprint example



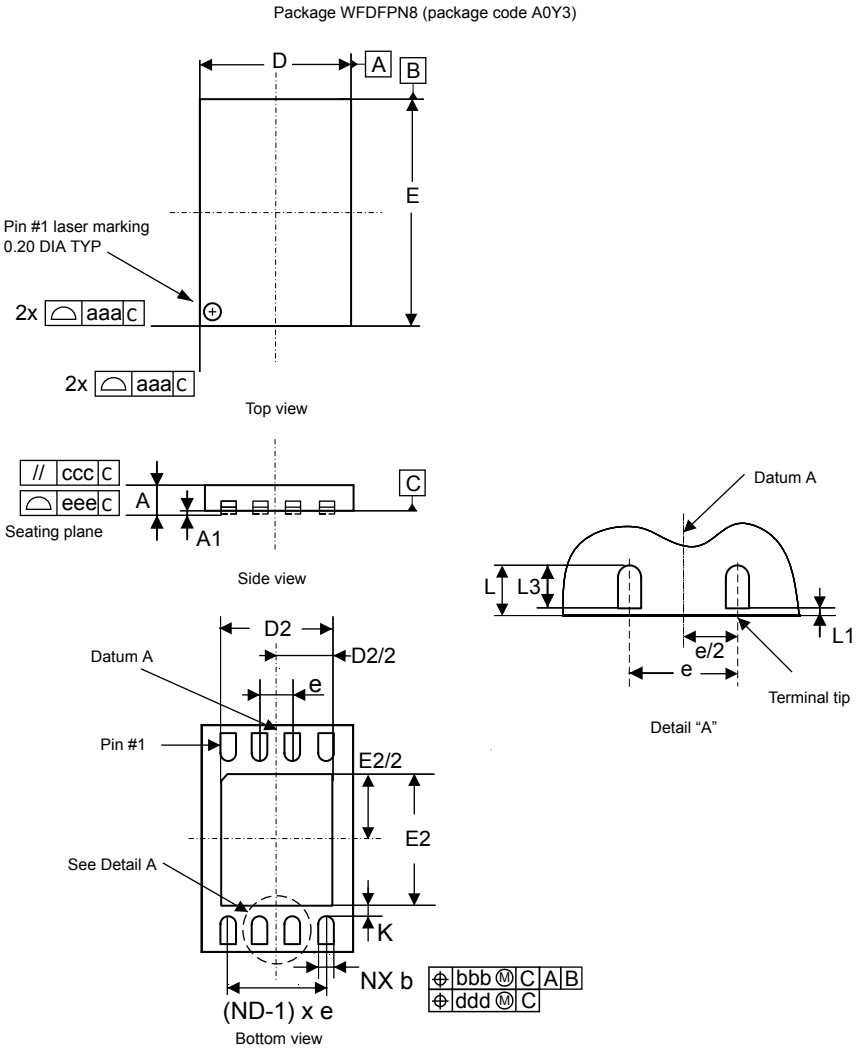
1. *Dimensions are expressed in millimeters.*

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9.3 WFDFPN8 (DFN8) package information

This WFDFPN is a 8-lead, 2 x 3 mm, 0.5 mm pitch very very thin fine pitch dual flat package.

Figure 17. WFDFPN8 (DFN8) – Outline



1. *Drawing is not to scale.*
2. *Exposed copper is not systematic and can appear partially or totally according to the cross section.*

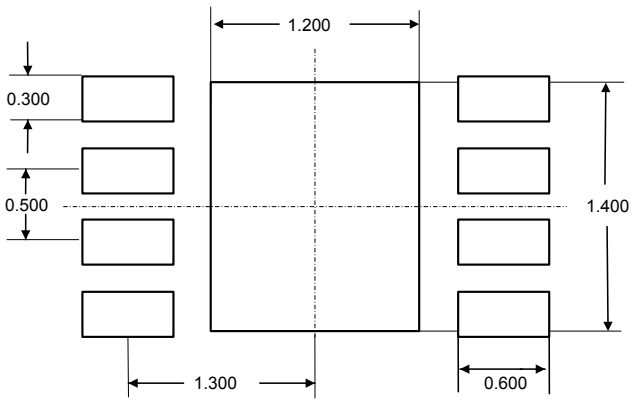
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Table 15. WFDFPN8 (DFN8) – Mechanical data

Symbol	Millimeters			Inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.700	0.750	0.800	0.0276	0.0295	0.0315
A1	0.025	0.045	0.065	0.0010	0.0018	0.0026
b[2]	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	1.900	2.000	2.100	0.0748	0.0787	0.0827
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.500	-	-	0.0197	-
L1	-	-	0.150	-	-	0.0059
L3	0.300	-	-	0.0118	-	-
D2	1.400	-	1.600	0.0551	-	0.0630
E2	1.200	-	1.400	0.0472	-	0.0551
K	0.400	-	-	0.0157	-	-
L	0.300	-	0.500	0.0118	-	0.0197
NX [3]	8					
ND [4]	4					
aaa	-	-	0.150	-	-	0.0059
bbb[5]	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee [6]	-	-	0.080	-	-	0.0031

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension b applies to plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.*
3. *NX is the number of terminals.*
4. *ND is the number of terminals on the side D.*
5. *Max package warpage is 0.05 mm.*
6. *Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.*

Figure 18. WFDFPN8 (DFN8) – Footprint example



Note: The central pad (the area E2 by D2 in the Figure 17) must be either connected to V_{SS} or left floating (not connected) in the end application.

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10 Ordering information

Table 16. Ordering information scheme

Example: M24 C32-D R MN 3 T P /K

Device type

M24 = I2C serial access EEPROM

Device function

C32-D = 32 Kbit (4096 K x 8 bits) plus identification page

Operating voltage

R = V_{CC} = 1.7 V to 5.5 V

Package(1)

MN = SO8N (150 mil width)

DW = TSSOP8 (169 mil width)

MF = WFDFPN8 (DFN8) (2 x3 mm)

Device grade

3 = -40 to 125 °C. Automotive grade.

Option

T = Tape and reel packing

blank = tube packing

Planting technology

P or G = ECOPACK2

Process

/K = Manufacturing technology code

1. *All packages are ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimonyoxide flame retardants).*

Note: For a list of available options (speed, package, etc.) or for further information on any aspect of the devices, please contact your nearest ST sales office.

Note: Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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Revision history

Table 17. **Document revision history**

Date	Revision	Changes
03-Aug-2012	1	Initial release.
05-Mar-2013	2	Document reformatted. Document status changed from “Preliminary data” to “Production data”. Updated: • Section 3.6: Identification page • Section 6: Delivery state • ICC, VIL and VRES values in Table 10: DC characteristics
25-Mar-2013	3	Updated ICC1 and VIL rows in Table 10: DC characteristics.
05-Sep-2013	4	Added WFDFPN8 (MF) package. Removed UFDFPN8 (MLP8) package. Updated: • Note (1) under Table 5: Absolute maximum ratings. • Third waveform in Figure 12: AC waveforms.
10-Feb-2014	5	Changed Data retention from “40 years at 55 °C” to “50 years at 125 °C” in Features. Updated Figure 15: WFDFPN8 (MLP8) – 8-lead, 2 x 3 mm, 0.5 mm pitch very very thin fine pitch dual flat package outline.
08-Jan-2015	6	Updated: • note 2 on Table 5. • Figure 5 • Table 20 and Table 16 Added sentence related Engineering Sample on Section 10 and note 2 on Figure 5
23-Feb-2016	7	Updated: • Features • Table 6, Table 10, Figure 15, Table 16
06-Jun-2022	8	Updated: • Section Features, Section 2.2: Serial data (SDA), Section 9.1: TSSOP8 package information, Section 9.2: SO8N package information • Figure 1. Logic diagram • Table 5. Absolute maximum ratings, Table 3. Significant bits within the two address bytes, Table 6. Cycling performance by groups of four bytes, Section 9.3: WFDFPN8 (DFN8) package information, Table 16. Ordering information scheme Added note in Figure 7 and in Figure 8
17-Jul-2026	9	Updated: • Section Features • Section 7: Maximum rating • Section 8: DC and AC parameters • Section 9.1: TSSOP8 package information • Section 9.3: WFDFPN8 (DFN8) package information • Section 10: Ordering information

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