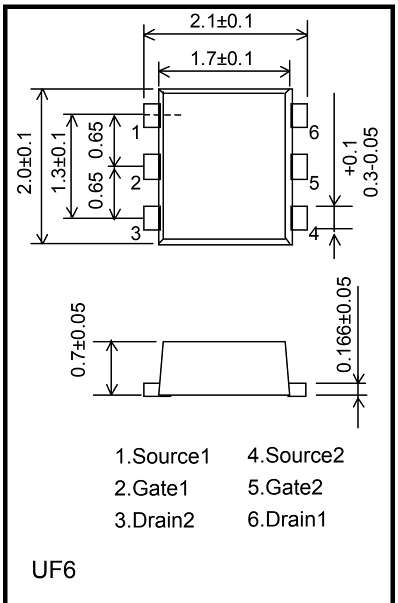
TOSHIBA Field-Effect Transistor Silicon N / P Channel MOS Type

SSM6L39TU

○ Power Management Switch Applications
○ High-Speed Switching Applications

Unit: mm



JEDEC	―
JEITA	―
TOSHIBA	2-2T1B

Weight: 7.0 mg (typ.)

- N-ch: 1.5-V drive
  P-ch: 1.8-V drive
- N-ch, P-ch, 2-in-1
- Low ON-resistance Q1 N-ch: R_{on} = 247 mΩ (max) (@V_{GS} = 1.5 V)
  R_{on} = 190 mΩ (max) (@V_{GS} = 1.8 V)
  R_{on} = 139 mΩ (max) (@V_{GS} = 2.5 V)
  Q2 P-ch: R_{on} = 430 mΩ (max) (@V_{GS} = −1.8 V)
  R_{on} = 294 mΩ (max) (@V_{GS} = −2.5 V)

Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	20	V
Gate-source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	1.6	A
	Pulse	I_{DP}	3.2	

Q2 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	−20	V
Gate-source voltage		V_{GSS}	±8	V
Drain current	DC	I_D	−1.5	A
	Pulse	I_{DP}	−3	

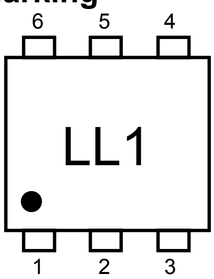
Absolute Maximum Ratings (Ta = 25 °C) (Q1, Q2 Common)

Characteristics	Symbol	Rating	Unit
Drain power dissipation	P_D(Note 1)	500	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C

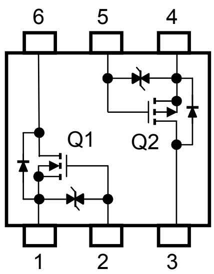
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Mounted on an FR4 board. (total dissipation) (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad : 645 mm^2)

Marking



Equivalent Circuit (top view)



Start of commercial production
2008-01

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Q1 Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 1 mA, V_{GS} = 0 V	20	—	—	V
		$V_{(BR)\ DSX}$	I_D = 1 mA, V_{GS} = -10 V	12	—	—	
Drain cutoff current		I_{DSS}	V_{DS} =20 V, V_{GS} = 0 V	—	—	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 1 mA	0.35	—	1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 1A (Note 2)	2.5	5.0	—	S
Drain-source ON-resistance		$R_{DS\ (ON)}$	I_D = 1 A, V_{GS} = 4.0 V (Note 2)	—	87	119	mΩ
			I_D = 1 A, V_{GS} = 2.5 V (Note 2)	—	105	139	
			I_D = 0.8 A, V_{GS} = 1.8 V (Note 2)	—	125	190	
			I_D = 0.3 A, V_{GS} = 1.5 V (Note 2)	—	145	247	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	260	—	pF
Output capacitance		C_{oss}		—	45	—	
Reverse transfer capacitance		C_{rss}		—	37	—	
Total Gate Charge		Q_g	V_{DS} = 10 V, I_D= 1.6 A, V_{GS} = 4 V	—	7.5	—	nC
Gate–Source Charge		Q_{gs}		—	5.6	—	
Gate–Drain Charge		Q_{gd}		—	1.9	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 0.5 A V_{GS} = 0 to 2.5 V, R_G = 4.7 Ω	—	8.3	—	ns
	Turn-off time	t_{off}		—	11.5	—	
Drain-source forward voltage		V_{DSF}	I_D = -1.6 A, V_{GS} = 0 V (Note 2)	—	-0.8	-1.2	V

Q2 Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = -1 mA, V_{GS} = 0 V	-20	—	—	V
		$V_{(BR)\ DSX}$	I_D = -1 mA, V_{GS} = +8 V	-12	—	—	
Drain cutoff current		I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	—	—	-10	μA
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = -3 V, I_D = -1 mA	-0.3	—	-1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -1 A (Note 2)	1.6	3.2	—	S
Drain-source ON-resistance		$R_{DS\ (ON)}$	I_D = -1.0 A, V_{GS} = -4 V (Note 2)	—	160	213	mΩ
			I_D = -0.8 A, V_{GS} = -2.5 V (Note 2)	—	210	294	
			I_D = -0.1 A, V_{GS} = -1.8 V (Note 2)	—	280	430	
Input capacitance		C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	—	250	—	pF
Output capacitance		C_{oss}		—	43	—	
Reverse transfer capacitance		C_{rss}		—	35	—	
Total Gate Charge		Q_g	V_{DS} = -10 V, I_D= -1.5 A, V_{GS} = -4 V	—	6.4	—	nC
Gate–Source Charge		Q_{gs}		—	4.5	—	
Gate–Drain Charge		Q_{gd}		—	1.9	—	
Switching time	Turn-on time	t_{on}	V_{DD} = -10 V, I_D = -1 A, V_{GS} = 0 to -2.5 V, R_G = 4.7 Ω	—	12	—	ns
	Turn-off time	t_{off}		—	11.2	—	
Drain-source forward voltage		V_{DSF}	I_D = 1.5 A, V_{GS} = 0 V (Note 2)	—	0.88	1.2	V

Note 2: Pulse test

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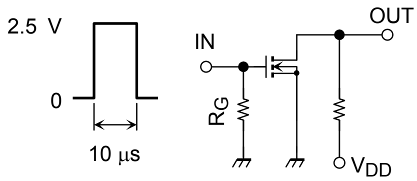
Q1 Switching Time Test Circuit

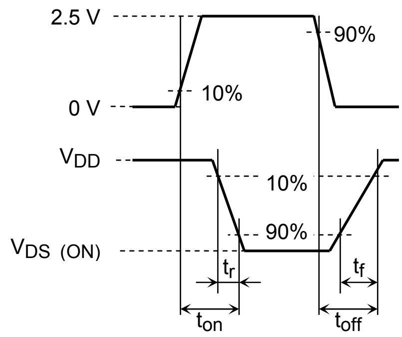
(a) Test Circuit



V_{DD} = 10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

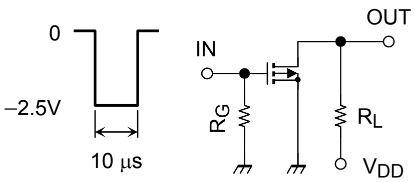
(b) V_{IN}

(c) V_{OUT}



Q2 Switching Time Test Circuit

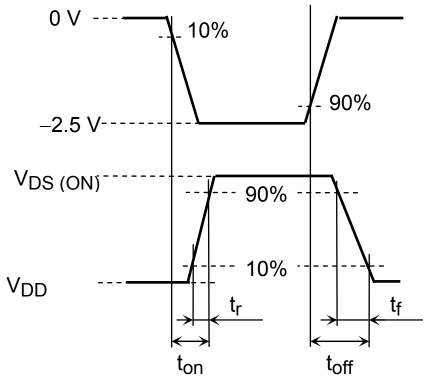
(a) Test Circuit



V_{DD} =− 10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



Q1 Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (1 mA for the Q1 of the SSM6L359TU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than $V_{th,}$ and $V_{GS(off)}$ must be lower than $V_{th.}$ This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

Q2 Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (−1 mA for the Q2 of the SSM6L39TU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than $V_{th,}$ and $V_{GS(off)}$ must be lower than $V_{th.}$ This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.
Take this into consideration when using the device.

Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

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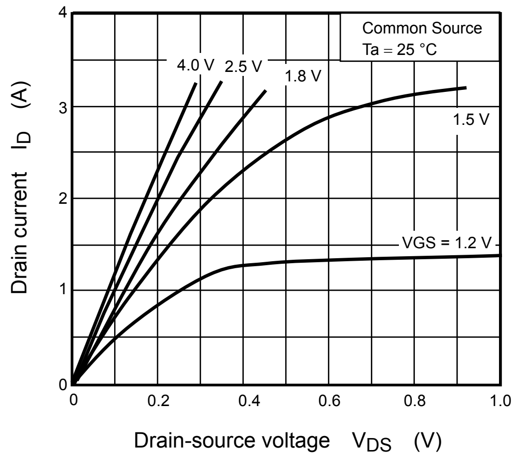
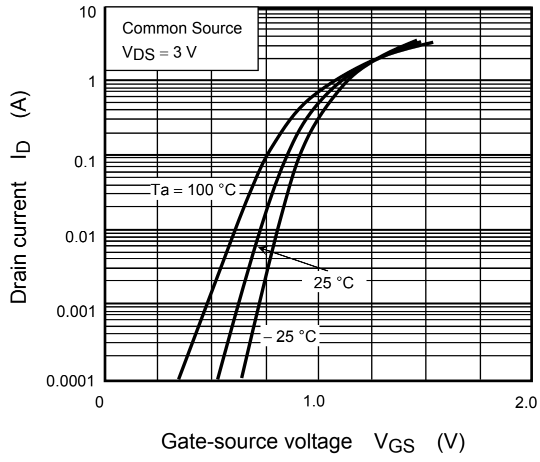
Q1 (N-ch MOSFET)

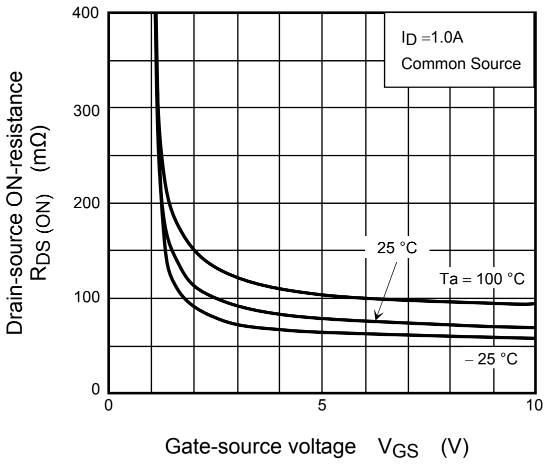
$I_D – V_{DS}$



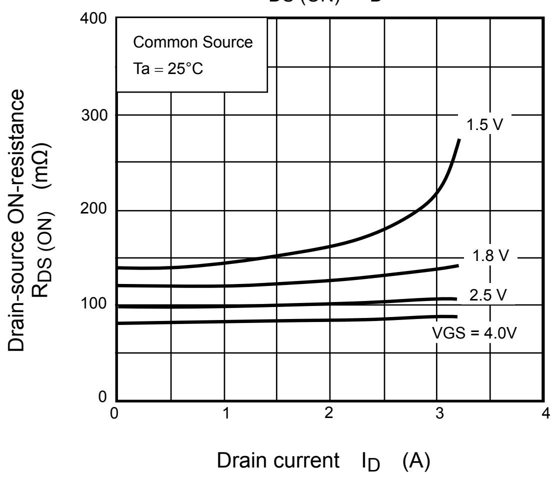
$I_D – V_{GS}$



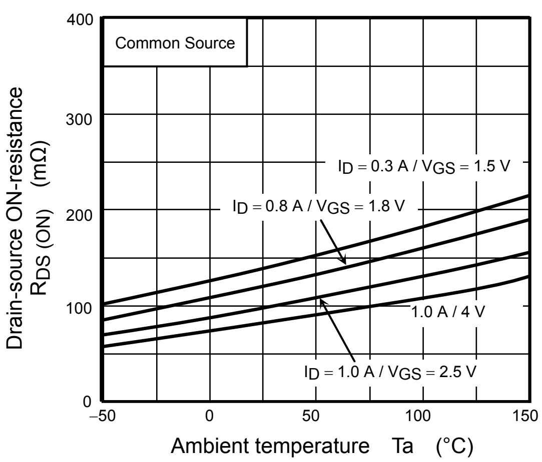
$R_{DS\,(ON)} – V_{GS}$



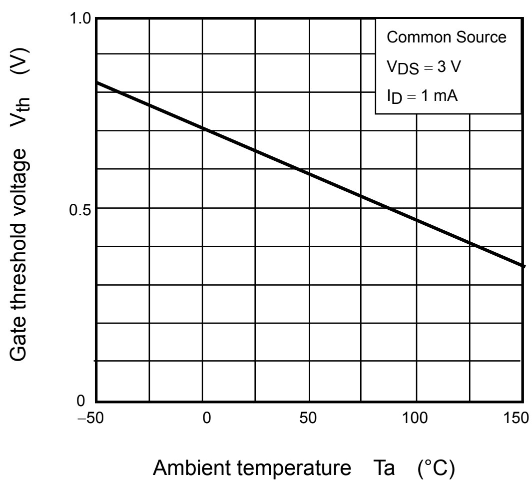
$R_{DS\,(ON)} – I_D$



$R_{DS\,(ON)} – Ta$



$V_{th} – Ta$



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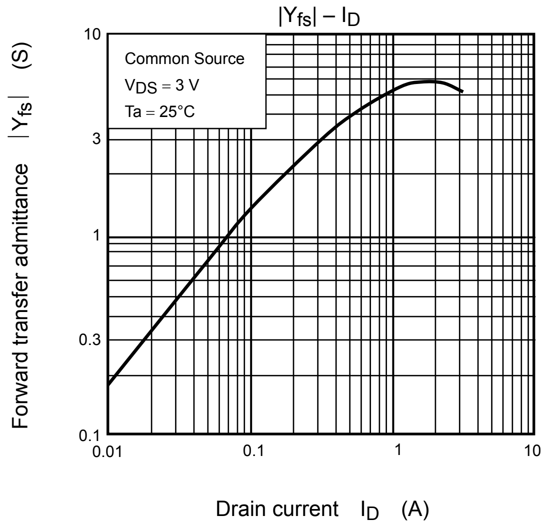
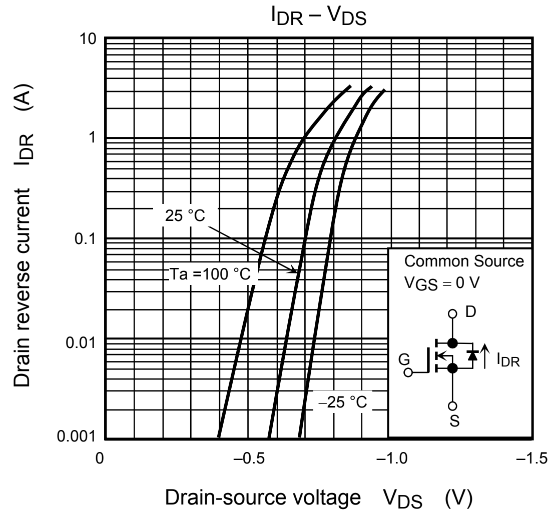
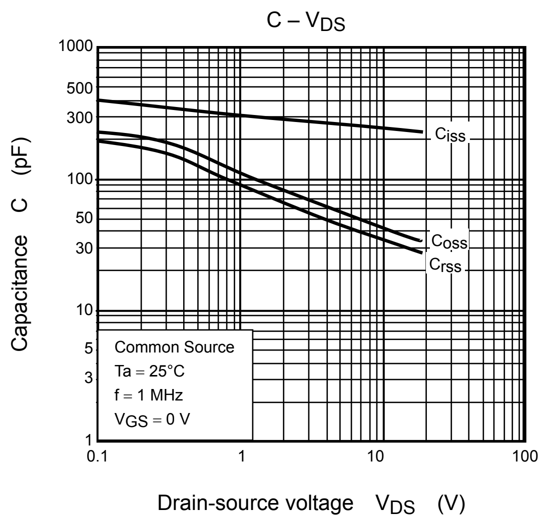
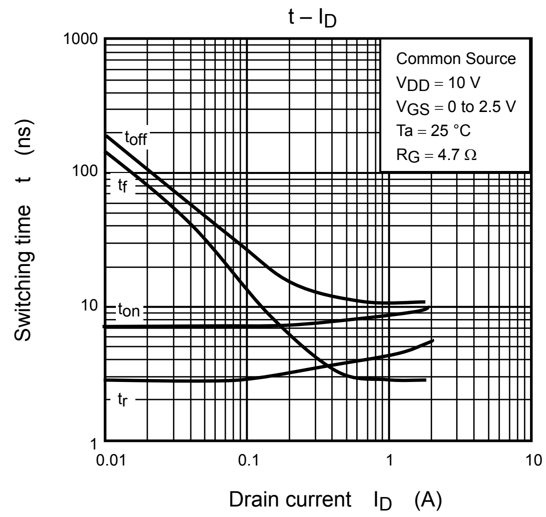
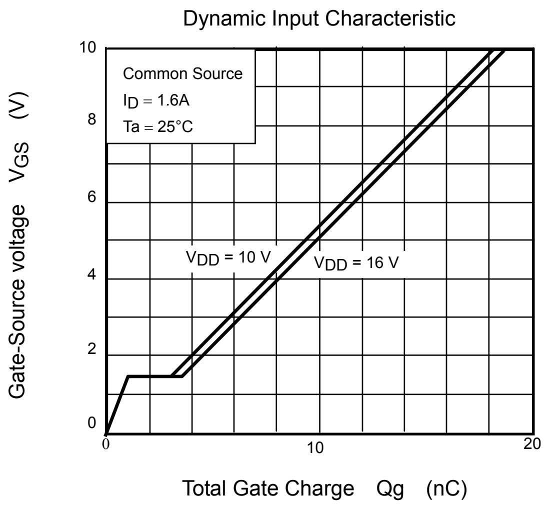
Q1 (N-ch MOSFET)











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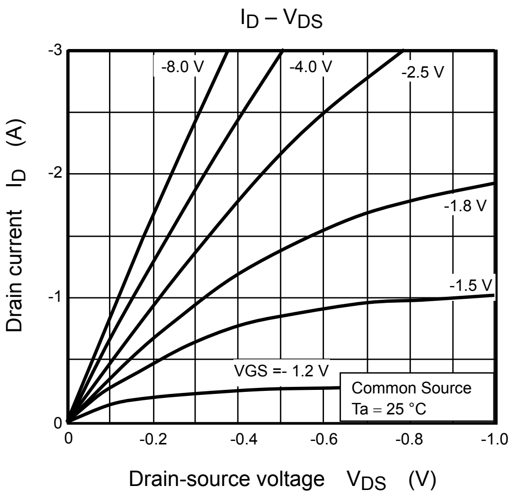
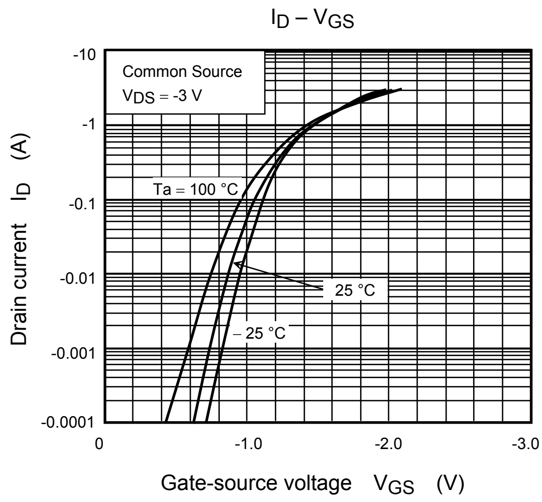
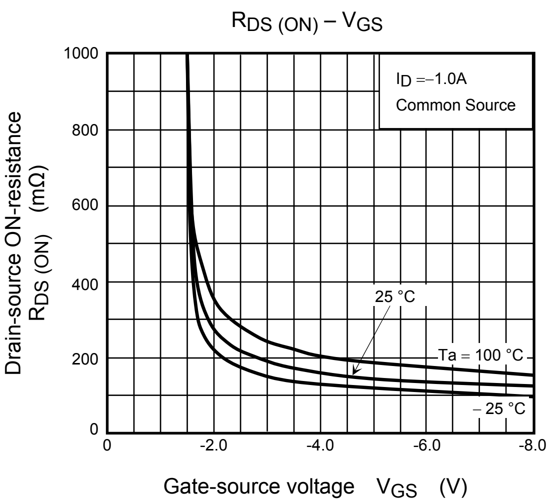
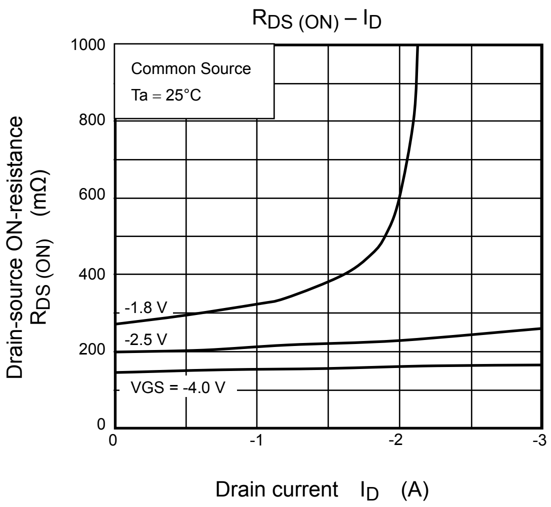
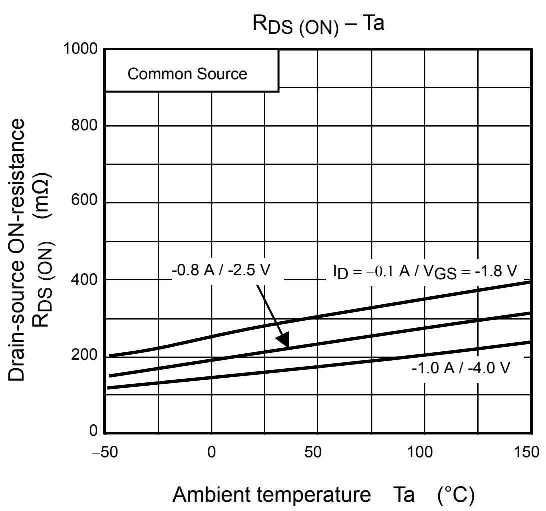
Q2 (P-ch MOSFET)

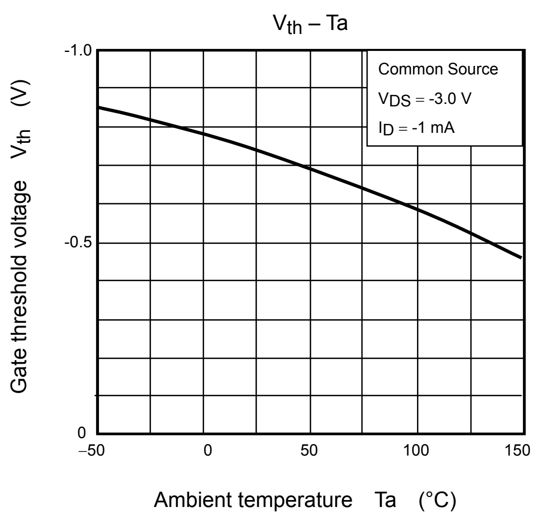












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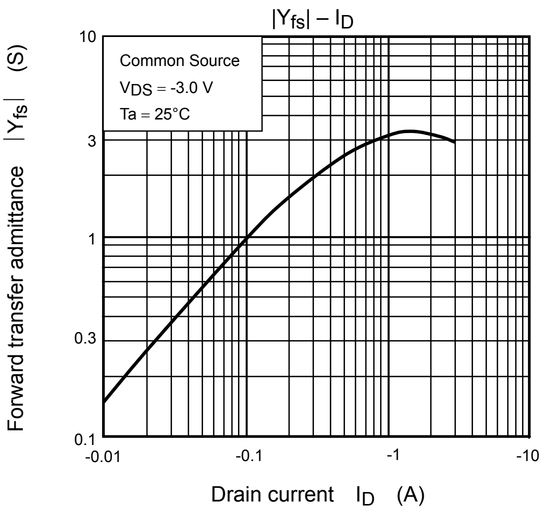
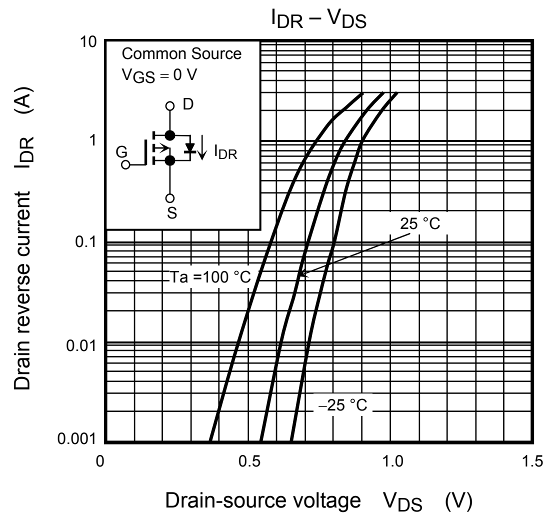
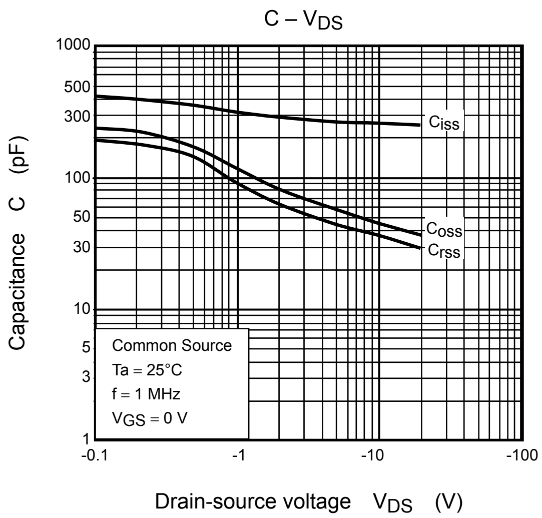
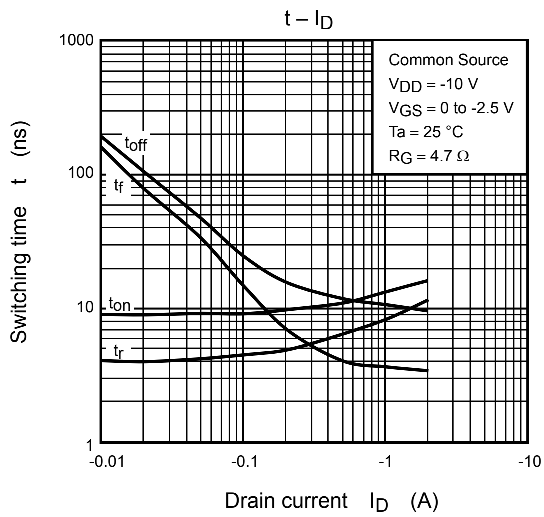
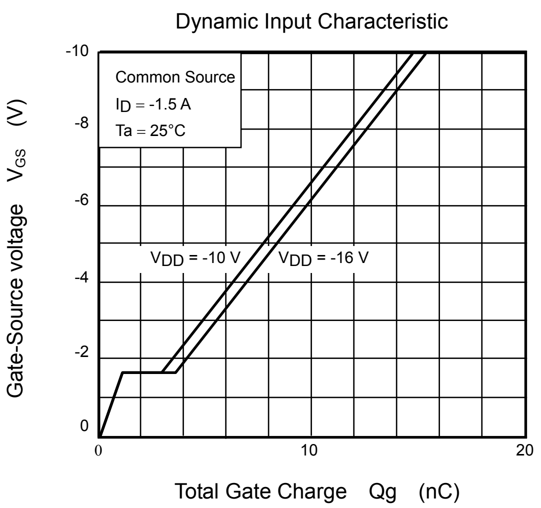
Q2 (P-ch MOSFET)











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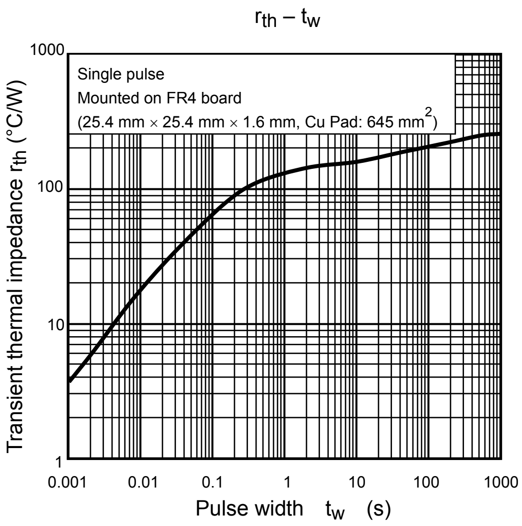
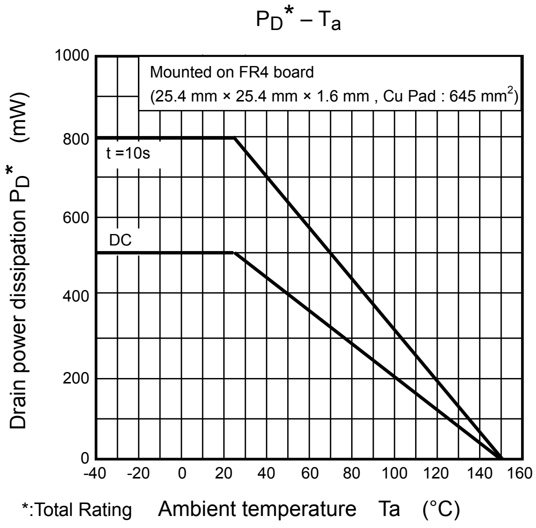
Q1,Q2 Common





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