Reset IC

PST893R/PST894R Series

Overview

This IC is a System Reset IC that detect turn-off or the power flicker in power supply of CPU or logic systems.
The IC has the delay time pin by an external capacitor and manual reset sense pin. The manual reset function can reset for system at any time.
Therefore the IC is suitable for some applications of forced reset or test function.

Features

- Low current consumption
- Manual reset function

Main specifications

- Absolute maximum rating : -0.3V ~ 6.5V
- Operating voltage : 0.7V ~ 6.0V
- Operating ambient temperature : -40℃ ~ 85℃
- Detection voltage : 0.8V ~ 5.2V (0.1V step)
- Detection voltage accuracy : ±1%
- Hysteresis voltage : Typ. VTH×0.05
- Consumption current : Typ. 0.35uA
- Output type : PST893R: CMOS
  PST894R: Open drain
- Output Logic : Active L
- Delay Resistance : Typ. 1MΩ

Packages

- SOT-25A

Application

- Reset circuits for microcomputers, CPUs and MPUs
- Reset circuits for logic circuits
- Battery voltage check circuits
- Back-up power supply switching circuits
- Level detection circuits

Model Name

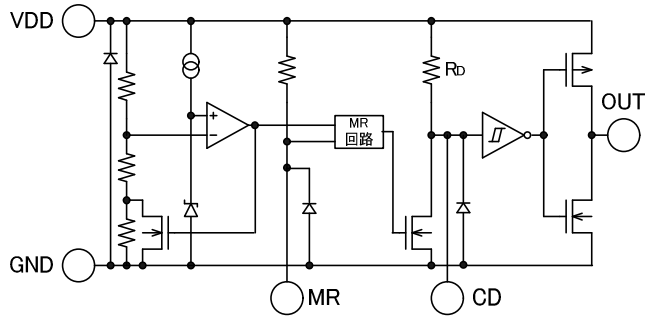
P S T 8 9 X X X X X X X

Series name (A) (B) (C) (D) (E)

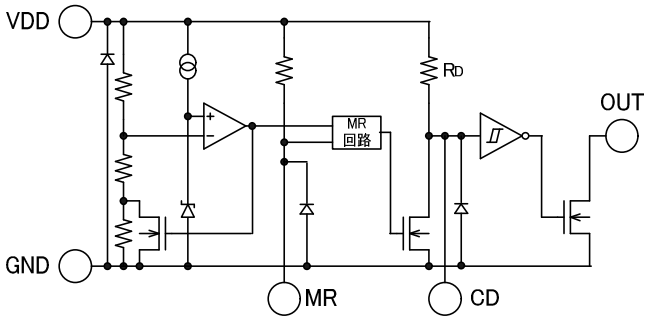
(A)	Output type	3	CMOS
		4	Open drain
(B)	Function option	R	Manual reset
(C)	Reset detection voltage	080	Specify the detection voltage with a three-digit number. Detection voltage is 0.80V to 5.20V (0.10V steps.)
		≀	
		520	
(D)	Package	N	SOT-25A
(E)	Packing specifications	R	R housing (SOT-25A)

Block Diagram

- PST853A (CMOS output)

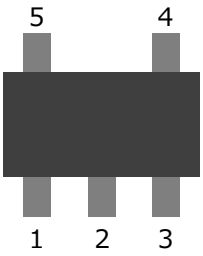


- PST854A (Open drain output)



Pin Configuration

- SOT-25A



Top view

Pin No.	Pin name	Function
1	OUT	Output pin
2	VDD	Power supply input pin
3	GND	Ground pin
4	CD	Delay pin with external capacitor
5	MR	Manual reset pin

Absolute Maximum Ratings

Item		Symbol	Min.	Max.	Unit
Supply voltage		VDD	-0.3	6.5	V
CD pin voltage		VCD	-0.3	VDD+0.3	V
MR pin voltage		VMR	-0.3	VDD+0.3	V
Output voltage	PST893R	VOUT	-0.3	VDD+0.3	V
	PST894R		-0.3	6.5	V
Output current		IOUT	0	20	mA
Storage temperature		Tstg	-55	125	℃

Recommended Operating Conditions

Item	Symbol	Min.	Max.	Unit
Operating Ambient temperature	Topr	-40	85	℃
Operating voltage	Vop	0.7	6.0	V

Electrical Characteristics

(Ta=25°C, unless otherwise specified) *Note1

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Reset voltage *Note1	VTH	VDD=H→L Upper lineTa=25℃ Lower lineTa=-40℃~85℃	0.8V	0.780 0.776	0.800 -	0.820 0.824	V	①
			0.9V	0.880 0.873	0.900 -	0.920 0.927		
			1.0V	0.980 0.970	1.000 -	1.020 1.030		
			1.1V	1.080 1.067	1.100 -	1.120 1.133		
			1.2V	1.180 1.164	1.200 -	1.220 1.236		
			1.3V	1.280 1.261	1.300 -	1.320 1.339		
			1.4V	1.380 1.358	1.400 -	1.420 1.442		
			1.5V	1.480 1.455	1.500 -	1.520 1.545		
			1.6V	1.580 1.552	1.600 -	1.620 1.648		
			1.7V	1.680 1.649	1.700 -	1.720 1.751		
			1.8V	1.780 1.746	1.800 -	1.820 1.854		
			1.9V	1.880 1.843	1.900 -	1.920 1.957		
			2.0V	1.980 1.940	2.000 -	2.020 2.060		
			2.1V	2.079 2.037	2.100 -	2.121 2.163		
			2.2V	2.178 2.134	2.200 -	2.222 2.266		
			2.3V	2.277 2.231	2.300 -	2.323 2.369		
			2.4V	2.376 2.328	2.400 -	2.424 2.472		
			2.5V	2.475 2.425	2.500 -	2.525 2.575		
			2.6V	2.574 2.522	2.600 -	2.626 2.678		
			2.7V	2.673 2.619	2.700 -	2.727 2.781		
			2.8V	2.772 2.716	2.800 -	2.828 2.884		
			2.9V	2.871 2.813	2.900 -	2.929 2.987		
			3.0V	2.970 2.910	3.000 -	3.030 3.090		

Electrical Characteristics

(Ta=25°C, unless otherwise specified) *Note1

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Reset voltage *Note1	VTH	VDD=H→L Upper line Ta=25℃ Lower line Ta=-40℃~85℃	3.1V	3.069 3.007	3.100 -	3.131 3.193	V	①
			3.2V	3.168 3.104	3.200 -	3.232 3.296		
			3.3V	3.267 3.201	3.300 -	3.333 3.399		
			3.4V	3.366 3.298	3.400 -	3.434 3.502		
			3.5V	3.465 3.395	3.500 -	3.535 3.605		
			3.6V	3.564 3.492	3.600 -	3.636 3.708		
			3.7V	3.663 3.589	3.700 -	3.737 3.811		
			3.8V	3.762 3.686	3.800 -	3.838 3.914		
			3.9V	3.861 3.783	3.900 -	3.939 4.017		
			4.0V	3.960 3.880	4.000 -	4.040 4.120		
			4.1V	4.059 3.977	4.100 -	4.141 4.223		
			4.2V	4.158 4.074	4.200 -	4.242 4.326		
			4.3V	4.257 4.171	4.300 -	4.343 4.429		
			4.4V	4.356 4.268	4.400 -	4.444 4.532		
			4.5V	4.455 4.365	4.500 -	4.545 4.635		
			4.6V	4.554 4.462	4.600 -	4.646 4.738		
			4.7V	4.653 4.559	4.700 -	4.747 4.841		
			4.8V	4.752 4.656	4.800 -	4.848 4.944		
			4.9V	4.851 4.753	4.900 -	4.949 5.047		
			5.0V	4.950 4.850	5.000 -	5.050 5.150		
			5.1V	5.049 4.947	5.100 -	5.151 5.253		
			5.2V	5.148 5.044	5.200 -	5.252 5.356		

Electrical Characteristics

(Ta=25°C, unless otherwise specified) *Note1

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Hysteresis voltage	⊿VTH	VDD=L→H	0.8V	0.024	0.040	0.064	V	①
			0.9V	0.027	0.045	0.072		
			1.0V	0.030	0.050	0.080		
			1.1V	0.033	0.055	0.088		
			1.2V	0.360	0.600	0.960		
			1.3V	0.039	0.065	0.104		
			1.4V	0.042	0.070	0.112		
			1.5V	0.045	0.075	0.120		
			1.6V	0.048	0.080	0.128		
			1.7V	0.051	0.085	0.136		
			1.8V	0.054	0.090	0.144		
			1.9V	0.057	0.095	0.152		
			2.0V	0.060	0.100	0.160		
			2.1V	0.063	0.105	0.168		
			2.2V	0.066	0.110	0.176		
			2.3V	0.069	0.115	0.184		
			2.4V	0.072	0.120	0.192		
			2.5V	0.075	0.125	0.200		
			2.6V	0.078	0.130	0.208		
			2.7V	0.081	0.135	0.216		
			2.8V	0.084	0.140	0.224		
			2.9V	0.087	0.145	0.232		
			3.0V	0.090	0.150	0.240		
			3.1V	0.093	0.155	0.248		
			3.2V	0.096	0.160	0.256		
			3.3V	0.099	0.165	0.264		
			3.4V	0.102	0.170	0.272		
			3.5V	0.105	0.175	0.280		
			3.6V	0.108	0.180	0.288		
			3.7V	0.111	0.185	0.296		
			3.8V	0.114	0.190	0.304		
			3.9V	0.117	0.195	0.312		
			4.0V	0.120	0.200	0.320		
			4.1V	0.123	0.205	0.328		
			4.2V	0.126	0.210	0.336		
			4.3V	0.129	0.215	0.344		
			4.4V	0.132	0.220	0.352		
			4.5V	0.135	0.225	0.360		
			4.6V	0.138	0.230	0.368		
			4.7V	0.141	0.235	0.376		
			4.8V	0.144	0.240	0.384		
			4.9V	0.147	0.245	0.392		
			5.0V	0.150	0.250	0.400		
			5.1V	0.153	0.255	0.408		
			5.2V	0.156	0.260	0.416		

Electrical Characteristics

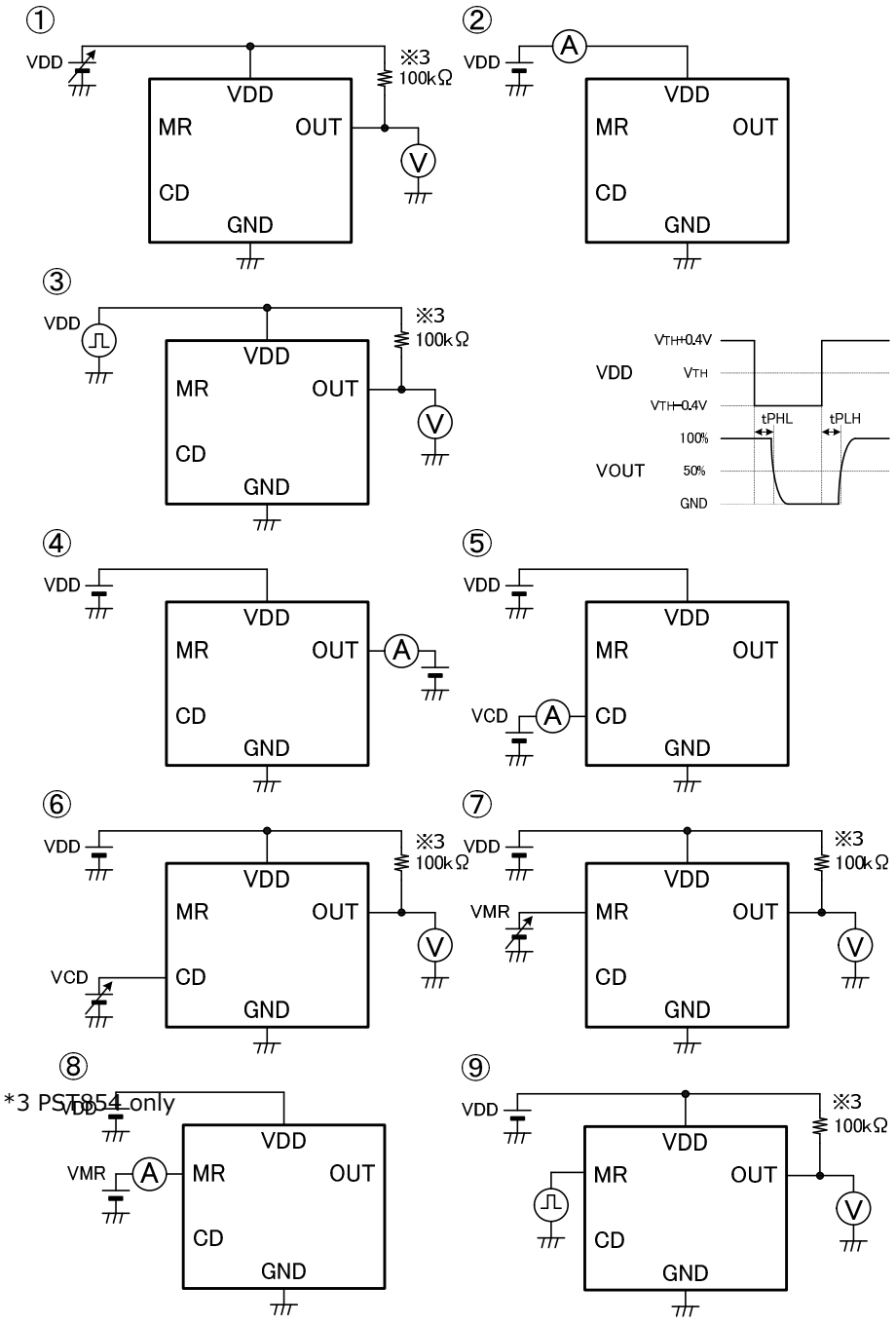
(Ta=25°C, unless otherwise specified) *Note1

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Consumption current	IDD	VDD=VTH+1V	0.8V~ 5.2V	-	0.35	1.0	uA	②
Reset threshold temperature coefficient *Note2	⊿VTH/℃	Ta=-40℃～+85℃	0.8V~ 5.2V	-	±100	-	ppm/℃	①
"L" Transfer delay time *Note2	tPHL	VDD=VTH+0.4V→VTH-0.4V	1.2V~ 5.2V	2	15	100	us	③
"H" Transfer delay time *Note2	tPLH	VDD=VTH-0.4V→VTH+0.4V	1.2V~ 5.2V	2	15	100	us	③
"L" Output current	IOL1	VDD=0.7V, VDS=0.05V	0.8V~ 5.2V	0.01	0.10	–	mA	④
	IOL2	VDD=1.2V, VDS=0.5V	1.3V~ 5.2V	0.23	2.00	–		
	IOL3	VDD=2.4V, VDS=0.5V	2.5V~ 5.2V	1.60	8.00	–		
	IOL4	VDD=3.6V, VDS=0.5V	3.7V~ 5.2V	3.20	12.0	–		
"H" Output current	IOH1	VDD=4.8V, VDS=0.5V PST893R only	0.8V~ 4.7V	0.36	0.62	-	mA	④
	IOH2	VDD=6.0V, VDS=0.5V PST893R only	0.8V~ 5.2V	0.46	0.75	-		
Output leakage current	Ileak	VDD=6V, VOUT=6V PST854R only	0.8V~ 5.2V	-	-	0.1	uA	④
Delay resistance	RCD	VDD=VTH+1V VCD=0V	0.8V~ 5.2V	0.5	1.0	2.0	MΩ	⑤
CD pin threshold voltage	VTCD	VDD=VTH×1.1 VCD=0V→VDD	0.8V~ 5.2V	VDD×0.3	VDD×0.5	VDD×0.7	V	⑥
CD pin output current 1	ICD1	VDD=0.7V VCD=0.1V	0.8V~ 5.2V	2	30	-	uA	⑤
CD pin output current 2	ICD2	VDD=0.8V VCD=0.5V	0.8V~ 1.0V	20	80	-	uA	⑤
		VDD=1.0V VCD=0.5V	1.1V~ 1.5V	50	150	-	uA	⑤
		VDD=1.5V VCD=0.5V	1.6V~ 5.2V	200	400	-	uA	⑤
MR pin input voltage H	VMR_H	VDD=VTH+1V	0.8V~ 5.2V	VDD-0.3	-	VDD×0.7	V	⑦
MR pin input voltage L	VMR_L	VDD=VTH+1V	0.8V~ 5.2V	0	-	0.3	V	⑦
MR pin input resistance	RMR	VDD=VTH+1V VMR=0V	0.8V~ 5.2V	0.5	1.0	2.0	MΩ	⑧
MR pin input pulse wide *Note2	tMR	VDD=VTH+1V	0.8V~ 5.2V	500	-	-	us	⑨

*Note1: The IC is only tested at Ta=25℃ in final test. It is guaranteed by design except Ta=25℃.

*Note2: The parameter is guaranteed by design.

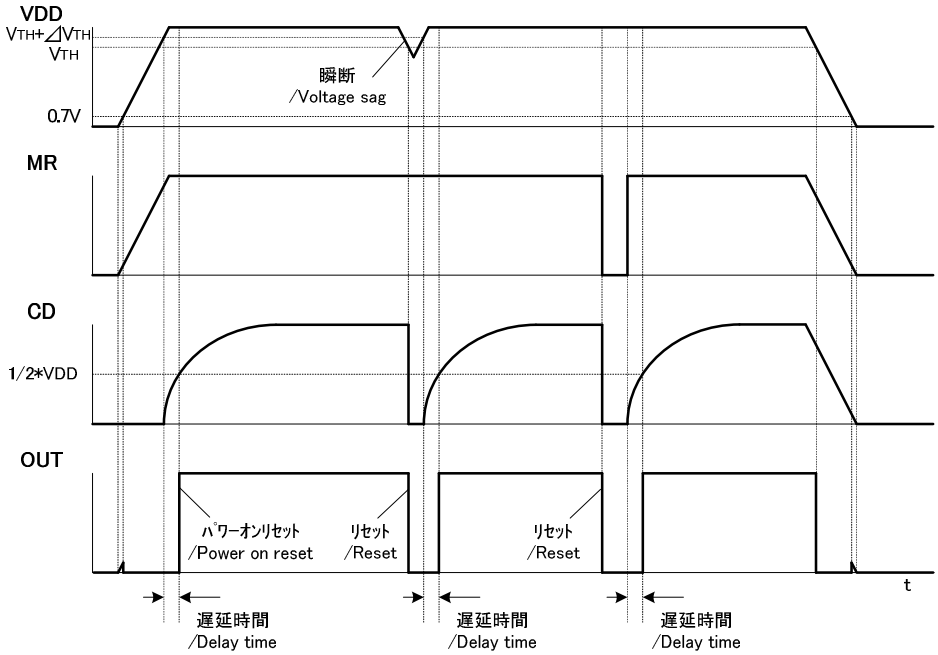
Test Circuit



*3 PST854 only

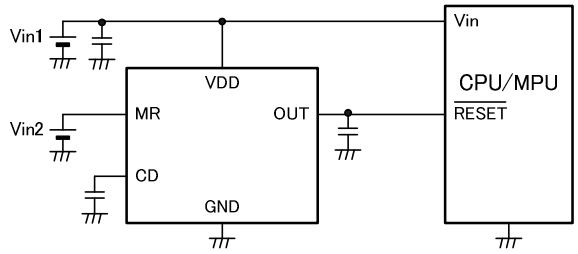
Timing Chart

- PST894R (Open drain output)

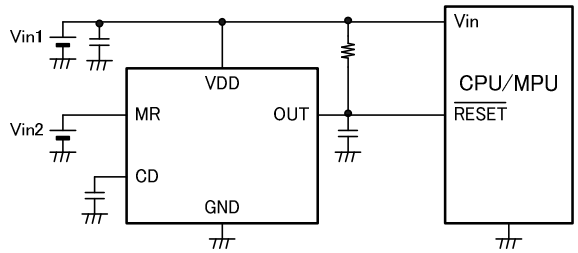


Application Circuit

▪PST893R



▪PST894R



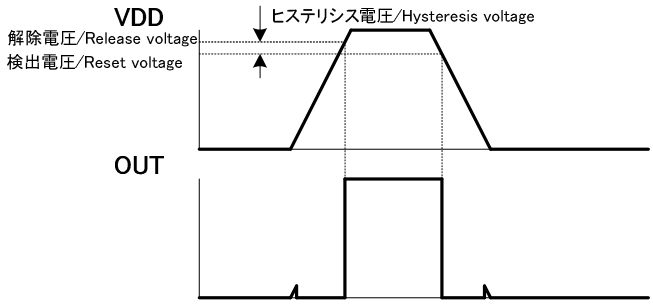
- The typical application circuit is not guaranteed for a set applications. It has to test sufficiently in a set applications.
- In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, Mitsumi shall not be liable for any such problem, nor grant a license therefore.

Application notes

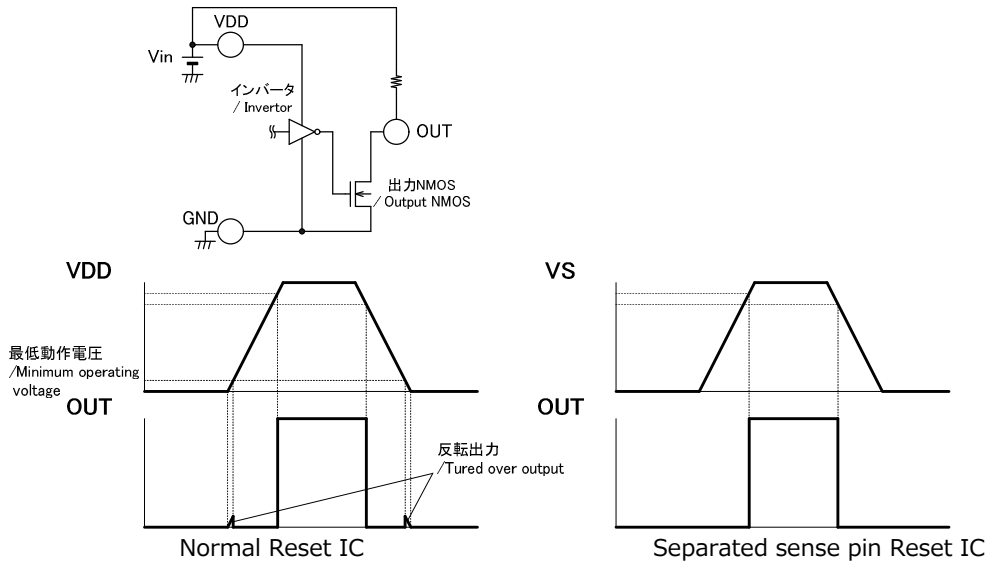
- Reset voltage
  In case of VDD=H→L, the reset voltage is the detected voltage at OUT=H→L.

- Release voltage
  In case of VDD=L→H, the release voltage is the detected voltage at OUT=L→H.
  (Release voltage = Reset voltage + Hysteresis voltage)

- Hysteresis voltage
  The hysteresis voltage prevents a malfunction from power supply noise.
  (Hysteresis voltage = Release voltage - Reset voltage)



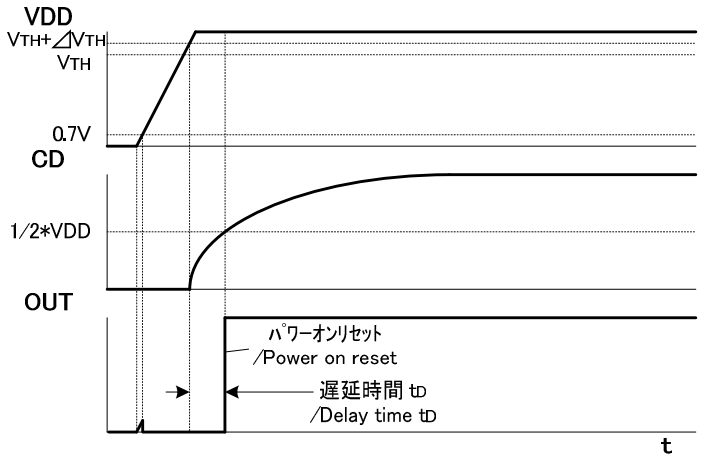
- VDD pin Minimum operating voltage
  VDD pin is a detected pin and an internal power supply circuit.
  When VDD is less than minimum operating voltage, the output NMOS is failed the bias voltage of gate.
  Therefore NMOS turn off, and OUT voltage turn over from low to high.
  If the minimum operating voltage can not be admitted, it is recommended to use a separated sense pin reset IC.



Application notes

■ Delay time

The delay circuit is connected with an external capacitor to CD pin.
The delay time is decided on time constant by an internal resistance and an external capacitor.
Power-on-reset (VS=L→H) is released, after an input voltage turned on stable voltage.



Delay Time

tD = 0.69×CD×RD [s]

C_D: External capacitor [F]
R_D: Delay resistance [Ω]

The charging time formula of the CR time constant, is a case of " VCD = 0.5 × VDD".
tD=-CD×RD×ln(1-VCD/VDD)
V_{CD}: CD threshold voltage [V]

■ CD pin

CD pin is high impedance for a delay resistance or constant current circuit.
It is necessary to take care for dew condensation or PCB or capacitor leakage.

■ Long delay time

When a high delay capacitor is used, the release delay time can be long.
But a delay time occurs in reset operation by discharge time of capacitor.
A set is recommended to design considering the delay time.

■ MR pin

MR pin can be manual reset at any timing.
When MR switches H→L, OUT switches H→L. When MR switches L→H, OUT switch H→L after delay time.
If MR pin is not used, it has to be connected with VDD pin.

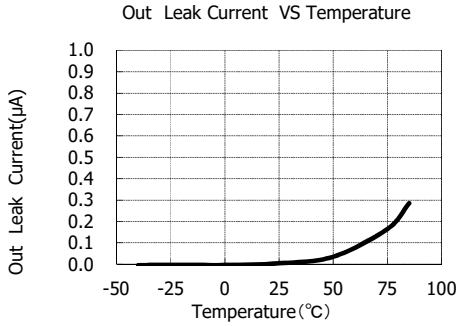
Application notes

■ CMOS output

CMOS output is inverter output between VDD and GND. It is not necessary to connect a pull-up resistance.

■ Open drain output

Open drain output is certainly connected with an external pull-up resistance.
The pull-up resistance can be supplied for any voltage and more than VDD voltage.
At high tempreture, please pays attention to the leak current for open drain NMOS,
it happens output voltage is up to leak current.

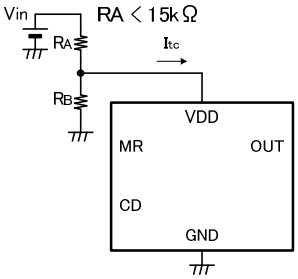


■ Oscillation

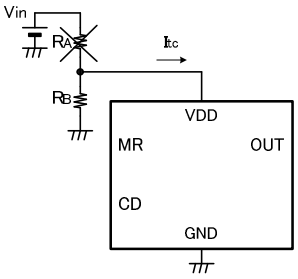
When a series resistance RA is connected with VDD, it is possible to occur an oscillation at threshold voltage.
It is occurred by voltage drops of a through current Itc at threshold and a series resistance RA.
To prevent it, RA has to be set less than 15kΩ.
In CMOS output, since it may oscillate, please do not put resistance RA.

Open drain output

・RA ＜ 15kΩ



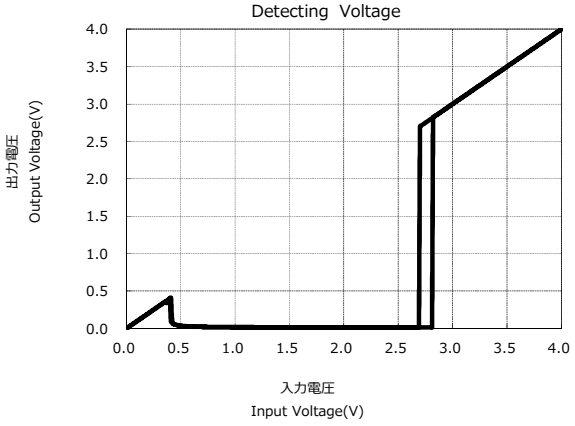
CMOS output



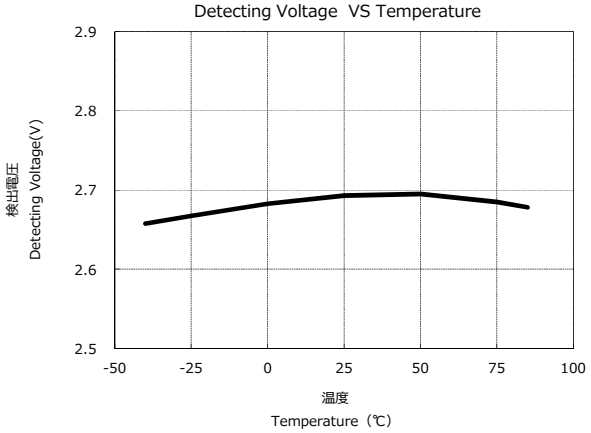
Typical Performance Characteristics (PST894R270)

(Ta=25°C, unless otherwise specified)

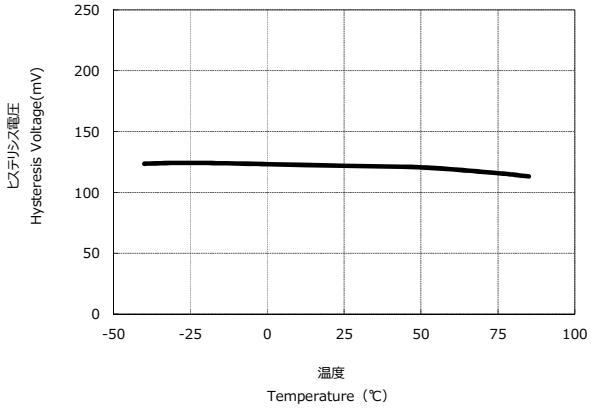
検出電圧
Detecting Voltage



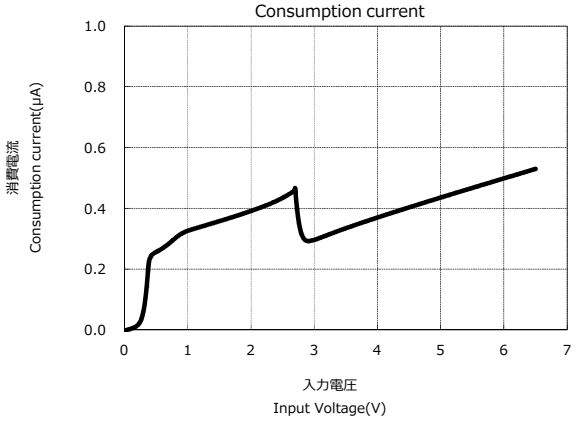
検出電圧 対 温度
Detecting Voltage VS Temperature



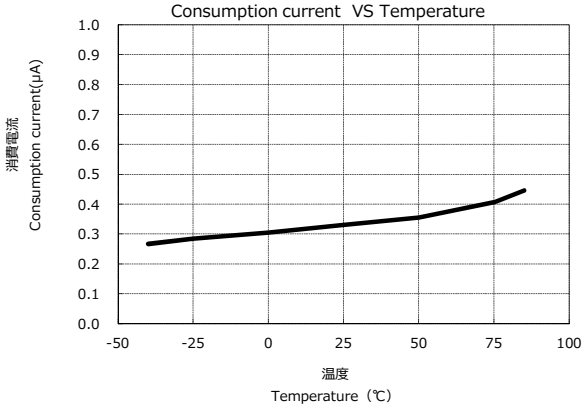
ヒステリシス電圧 対 温度
Hysteresis Voltage VS Temperature



消費電流
Consumption current



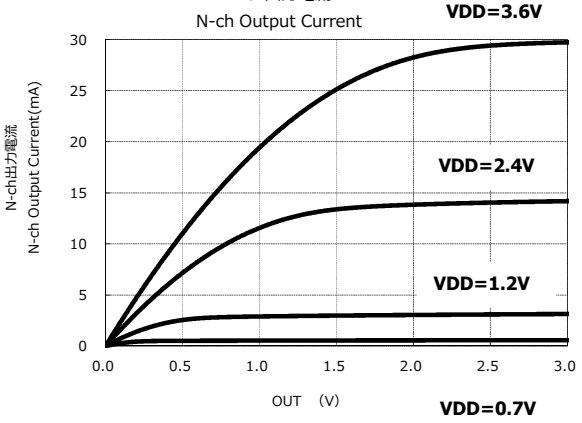
消費電流 対 温度
Consumption current VS Temperature



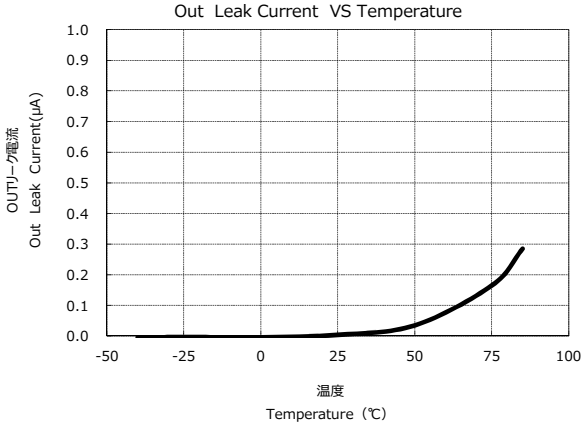
Typical Performance Characteristics (PST894R270)

(特記なき場合 Ta=25℃)

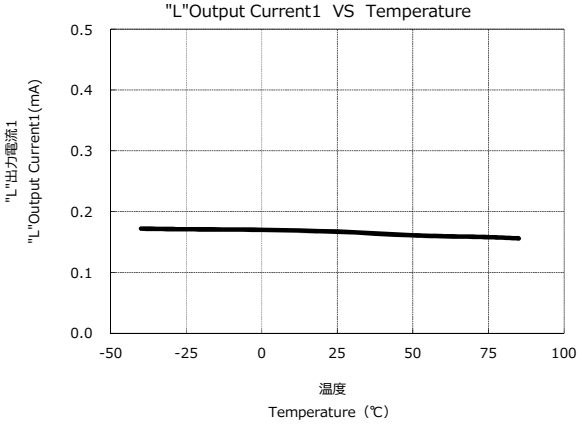
N-ch出力電流
N-ch Output Current



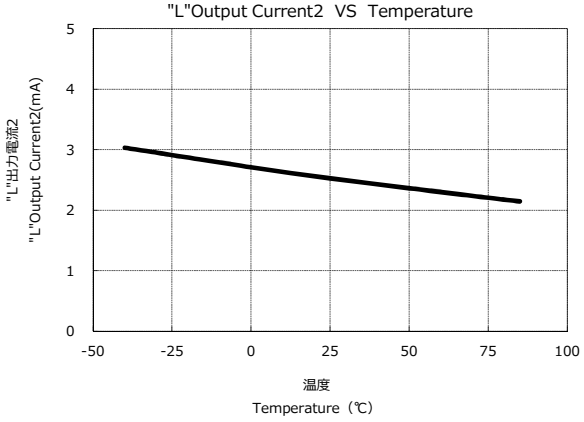
OUTリーク電流 対 温度
Out Leak Current VS Temperature



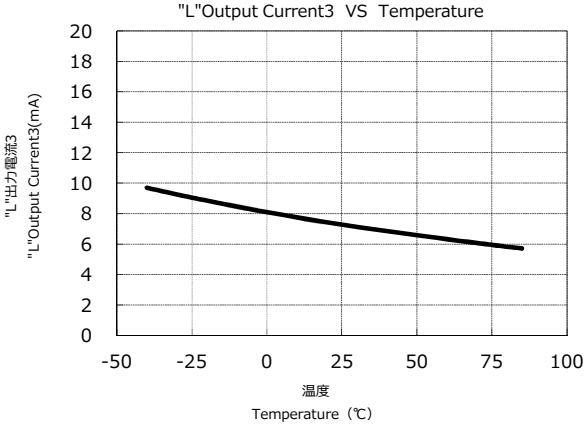
"L"出力電流1 対 温度
"L"Output Current1 VS Temperature



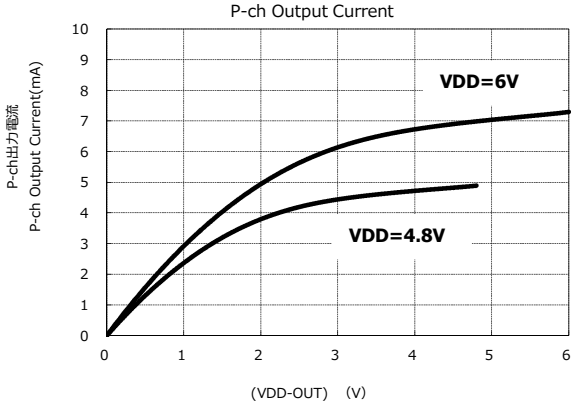
"L"出力電流2 対 温度
"L"Output Current2 VS Temperature



"L"出力電流3 対 温度
"L"Output Current3 VS Temperature



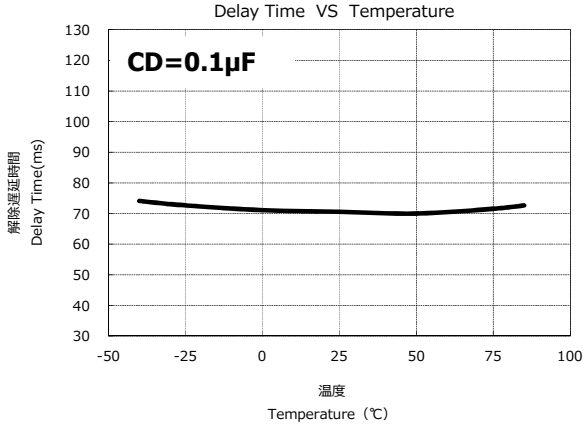
P-ch出力電流
P-ch Output Current



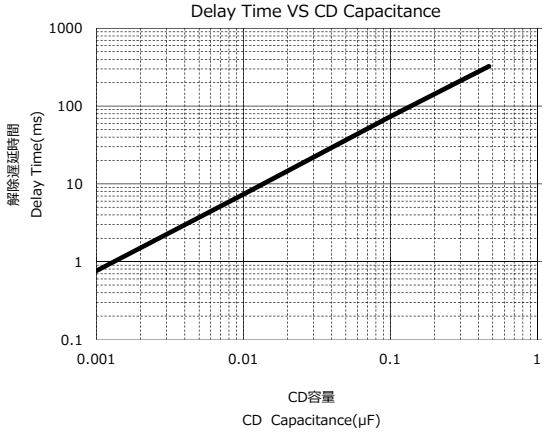
特性例 (PST894R270)

(特記なき場合 Ta=25℃)

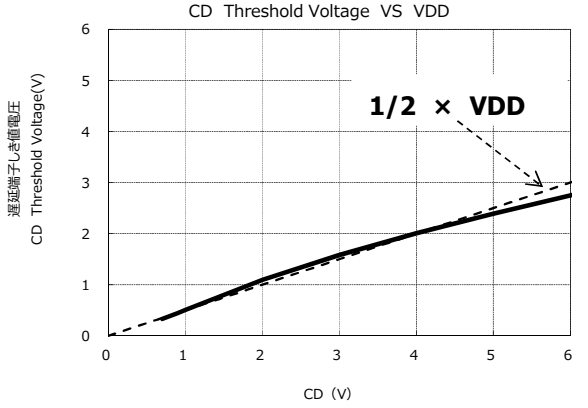
解除遅延時間 対 温度
Delay Time VS Temperature



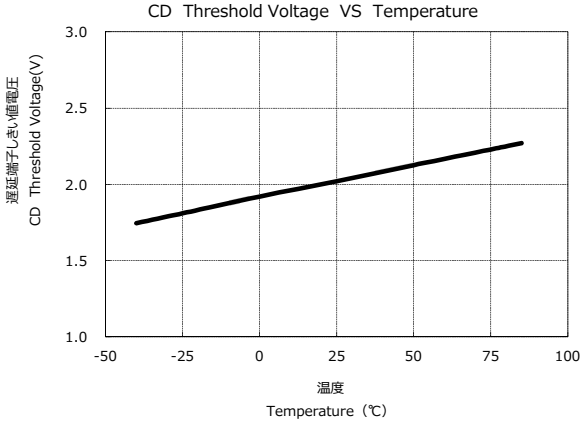
解除遅延時間 対 CD容量
Delay Time VS CD Capacitance



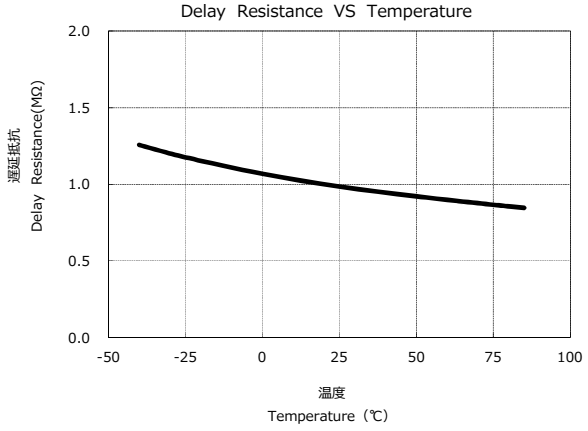
遅延端子しきい値電圧 対 VDD
CD Threshold Voltage VS VDD



遅延端子しきい値電圧 対 温度
CD Threshold Voltage VS Temperature



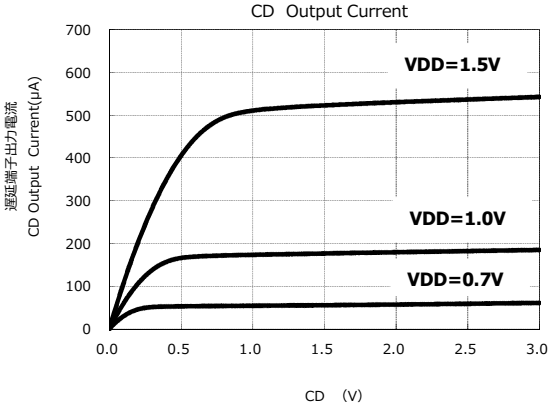
遅延抵抗 対 温度
Delay Resistance VS Temperature



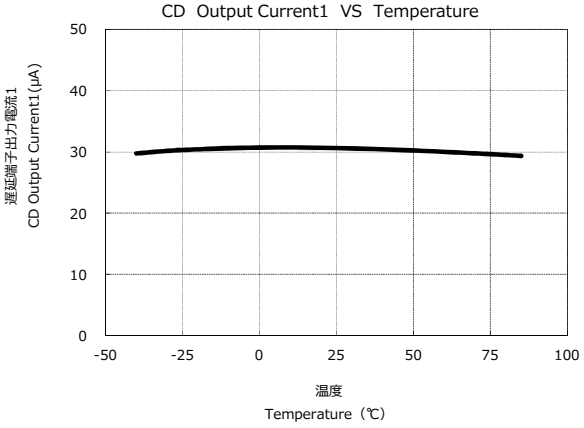
特性例 (PST894R270)

(特記なき場合 Ta=25℃)

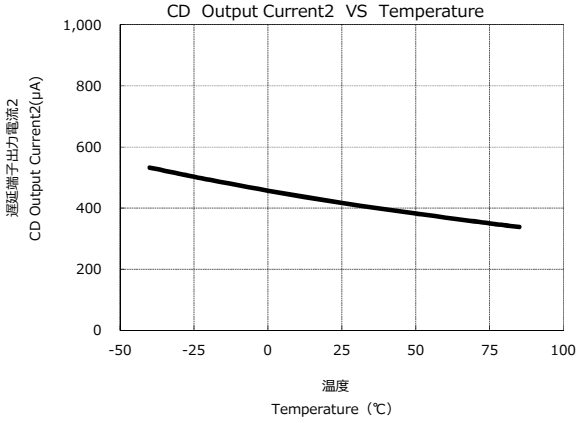
遅延端子出力電流
CD Output Current



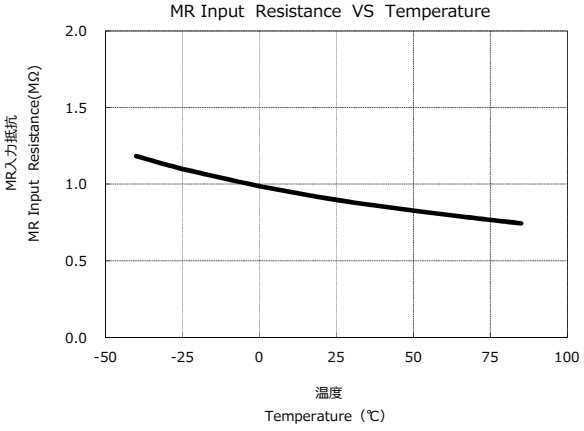
遅延端子出力電流1 対 温度
CD Output Current1 VS Temperature



遅延端子出力電流2 対 温度
CD Output Current2 VS Temperature



MR入力抵抗 対 温度
MR Input Resistance VS Temperature



MRスレッショルド電圧 対 温度
MR Threshold voltage VS Temperature