ISO7310-Q1 Robust EMC, Low Power, Single Channel Digital Isolator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM Classification Level 3A
  - Device CDM Classification Level C6
- Signaling Rate: 25 Mbps
- Integrated Noise Filter at the Input
- Default Output *High* and *Low* Options
- Low Power Consumption: Typical I_{CC}
  - 1.9 mA at 1 Mbps, 3.8 mA at 25 Mbps (5-V Supplies)
  - 1.4 mA at 1 Mbps, 2.6 mA at 25 Mbps (3.3-V Supplies)
- Low Propagation Delay: 32 ns Typical (5-V Supplies)
- 65-kV/μs Transient Immunity, Typical (5-V Supplies)
- Robust Electromagnetic Compatibility (EMC)
  - System-level ESD, EFT, and Surge Immunity
  - Low Emissions
- Isolation Barrier Life: > 25 Years
- Operates from 3.3-V and 5-V Supplies
- 3.3-V and 5-V Level Translation
- Narrow Body SOIC-8 Package
- Safety and Regulatory Approvals:
  - 4242-V_{PK} Isolation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - 3000-V_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards
  - Planned CQC Certification per GB4943.1-2011

2 Applications

- Opto-Coupler Replacement in:
  - Industrial FieldBus
    - ProfiBus
    - ModBus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

3 Description

The ISO7310-Q1 device provides galvanic isolation up to 3000 V_{RMS} for 1 minute per UL 1577 and 4242 V_{PK} per VDE V 0884-10. These devices have one isolated channel comprised of a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, the ISO7310-Q1 device prevents noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. The device has integrated noise filters for harsh industrial environment where short noise pulses may be present at the device input pins.

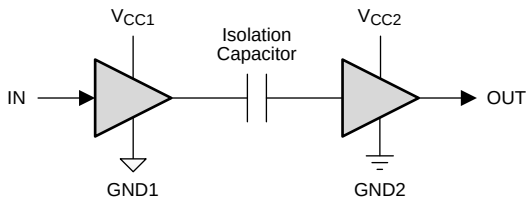
The ISO7310-Q1 device has TTL input thresholds and operate from 3-V to 5.5-V supply levels. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO7310-Q1 device has been significantly enhanced to enable system-level ESD, EFT, Surge and Emissions compliance.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7310-Q1	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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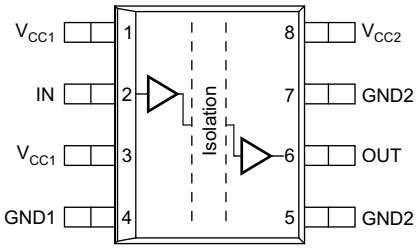
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2015	*	Initial release.

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	—	Ground connection for V_{CC1}
GND2	5	—	Ground connection for V_{CC2}
	7		
IN	2	I	Input
OUT	6	O	Output
V_{CC1}	1	—	Power supply, V_{CC1}
	3		
V_{CC2}	8	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Supply voltage(2)	V_{CC1} , V_{CC2}	–0.5	6	V
	Voltage (2)	IN, OUT	–0.5	V_{CC}+0.5(3)	V
I_O	Output current			±15	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3		5.5	V
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration	40			ns
1 / t_{ui}	Signaling rate	0		25	Mbps
T_J	Junction temperature(1)			136	°C
T_A	Ambient temperature	–40	25	125	°C

(1) To maintain the recommended operating conditions for T_J, see the *Thermal Information* table.

6.4 Thermal Information

THERMAL METRIC(1)		ISO7310-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	65.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.7	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics—5-V Supply

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 9	V_{CC2} – 0.5	4.7		V
		I_{OH} = –20 µA; see Figure 9	V_{CC2} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 9		0.2	0.4	V
		I_{OL} = 20 µA; see Figure 9		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			480		mV
I_{IH}	High-level input current	IN = V_{CC}			10	µA
I_{IL}	Low-level input current	IN = 0 V	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 11.	25	65		kV/µs

6.6 Supply Current Characteristics—5-V Supply

All inputs switching with square wave clock signal for dynamic I_{CC} measurement. V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15 pF	I_{CC1}		0.3	0.6	mA
			I_{CC2}		1.6	2.4	
	10 Mbps	C_L = 15 pF	I_{CC1}		0.5	1	
			I_{CC2}		2.2	3.2	
	25 Mbps	C_L = 15 pF	I_{CC1}		0.8	1.3	
			I_{CC2}		3	4.2	

6.7 Electrical Characteristics—3.3-V Supply

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 9	V_{CC2} – 0.5	3		V
		I_{OH} = –20 µA; see Figure 9	V_{CC2} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 9		0.2	0.4	V
		I_{OL} = 20 µA; see Figure 9		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			450		mV
I_{IH}	High-level input current	IN = V_{CC}			10	µA
I_{IL}	Low-level input curre	IN = 0 V	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 11	25	50		kV/µs

6.8 Supply Current Characteristics—3.3-V Supply

All inputs switching with square wave clock signal for dynamic I_{CC} measurement. V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: V_I = V_{CC} or 0 V, AC Input: C_L = 15 pF	I_{CC1}		0.2	0.4	mA
			I_{CC2}		1.2	1.8	
	10 Mbps	C_L = 15 pF	I_{CC1}		0.3	0.5	
			I_{CC2}		1.6	2.2	
	25 Mbps	C_L = 15 pF	I_{CC1}		0.5	0.8	
			I_{CC2}		2.1	3	

6.9 Power Dissipation Characteristics

V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 12.5 MHz 50% duty-cycle square wave (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation				34	mW
P_{D1}	Power dissipation by Side-1				7.9	mW
P_{D2}	Power dissipation by Side-2				26.1	mW

6.10 Switching Characteristics—5-V Supply

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	20	32	58	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$	See Figure 9			4	ns
$t_{sk(pp)}$ (2)	Part-to-part skew time				24	ns
t_r	Output signal rise time	See Figure 9		2.5		ns
t_f	Output signal fall time	See Figure 9		2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 10		7.5		µs

(1) Also known as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.11 Switching Characteristics

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	22	36	67	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$	See Figure 9			3.5	ns
$t_{sk(pp)}$ (2)	Part-to-part skew time				28	ns
t_r	Output signal rise time	See Figure 9		3.2		ns
t_f	Output signal fall time	See Figure 9		2.7		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 10		7.4		µs

(1) Also known as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.12 Typical Characteristics

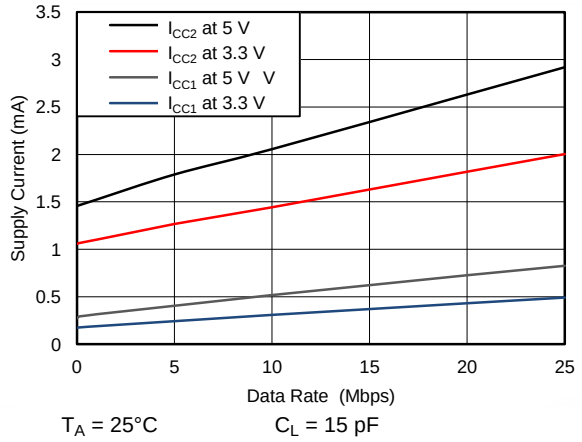


Figure 1. Supply Current vs Data Rate (With 15-pF Load)

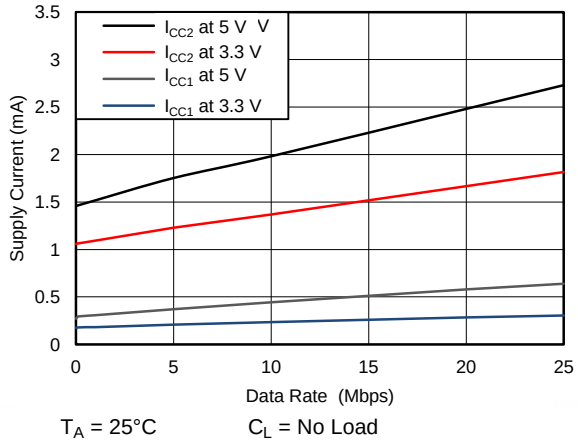


Figure 2. Supply Current vs Data Rate (With No Load)

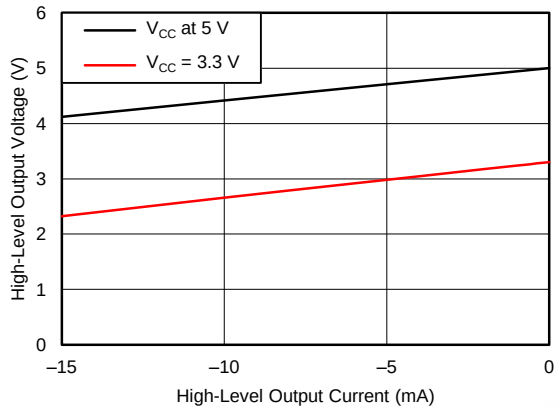


Figure 3. High-Level Output Voltage vs High-level Output Current

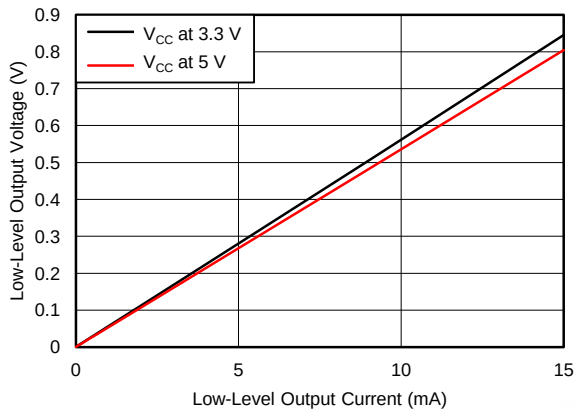


Figure 4. Low-Level Output Voltage vs Low-Level Output Current

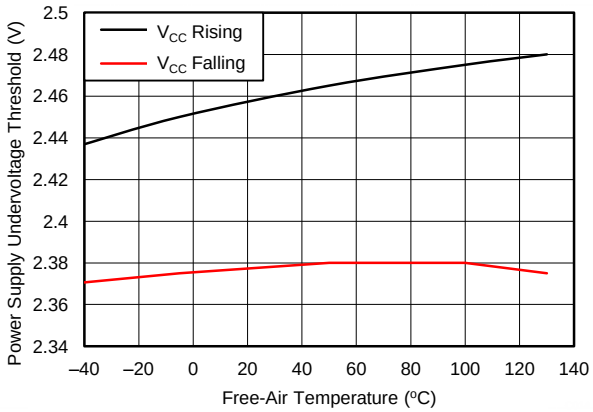


Figure 5. Power Supply Undervoltage Threshold vs Free-Air Temperature

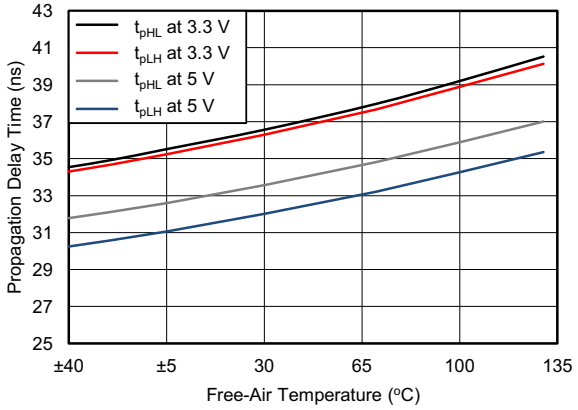


Figure 6. Propagation Delay Time vs Free-Air Temperature

Typical Characteristics (continued)

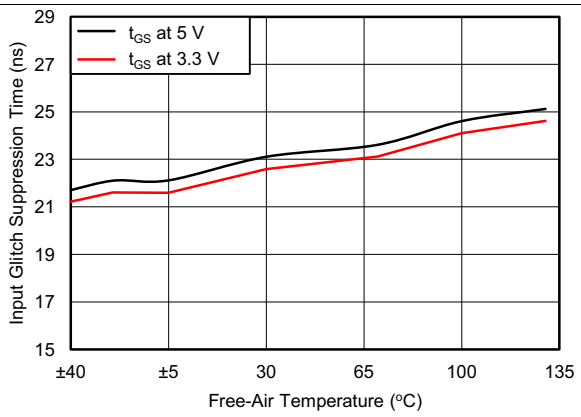


Figure 7. Input Glitch Suppression Time vs Free-Air Temperature

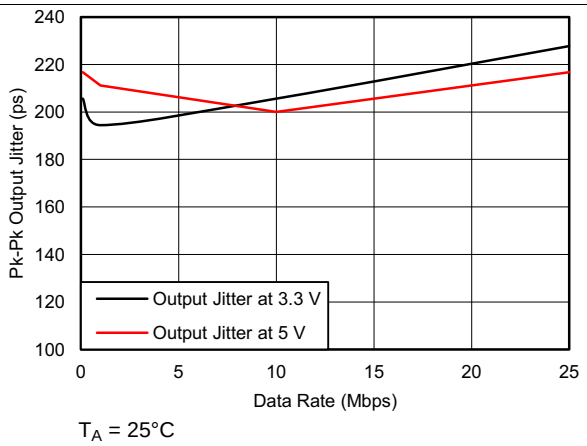
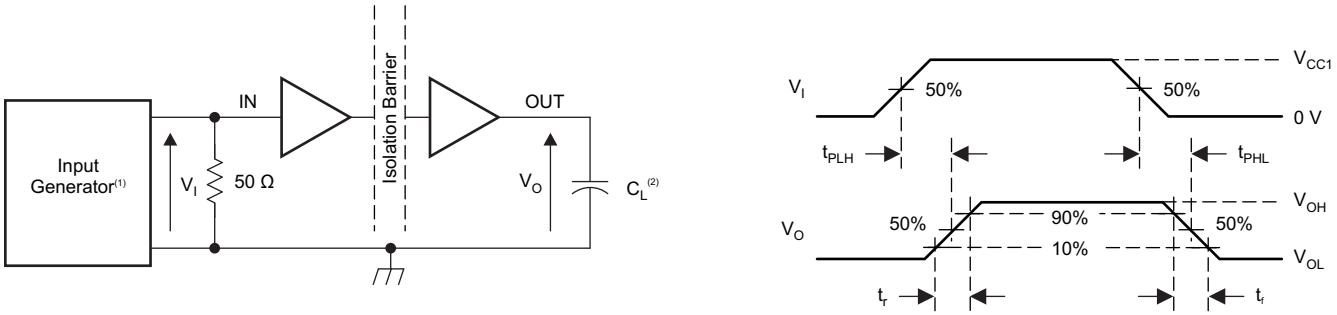


Figure 8. Output Jitter vs Data Rate

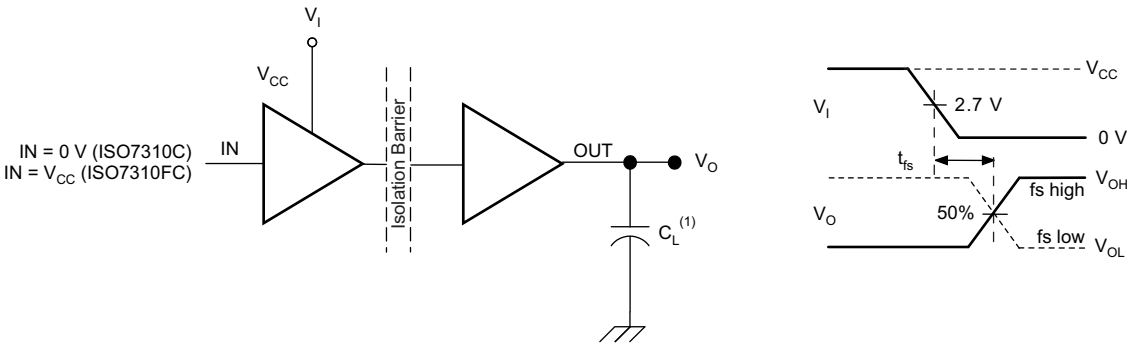
7 Parameter Measurement Information



(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.

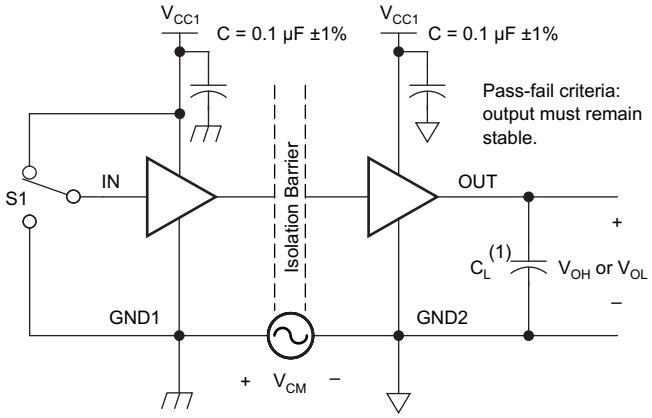
(2) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 9. Switching Characteristic Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 10. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 11. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The isolator in Figure 12 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency (HF) channel with a bandwidth from 100 kbps up to 25 Mbps, and a low-frequency (LF) channel covering the range from 100 kbps down to DC.

In principle, a single-ended input signal entering the HF channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transient pulses, which then are converted into CMOS levels by a comparator. The transient pulses at the input of the comparator can be either above or below the common mode voltage VREF depending on whether the input bit transitions from 0 to 1 or 1 to 0. The comparator threshold is adjusted based on the expected bit transition. A decision logic (DCL) at the output of the HF channel comparator measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

8.2 Functional Block Diagram

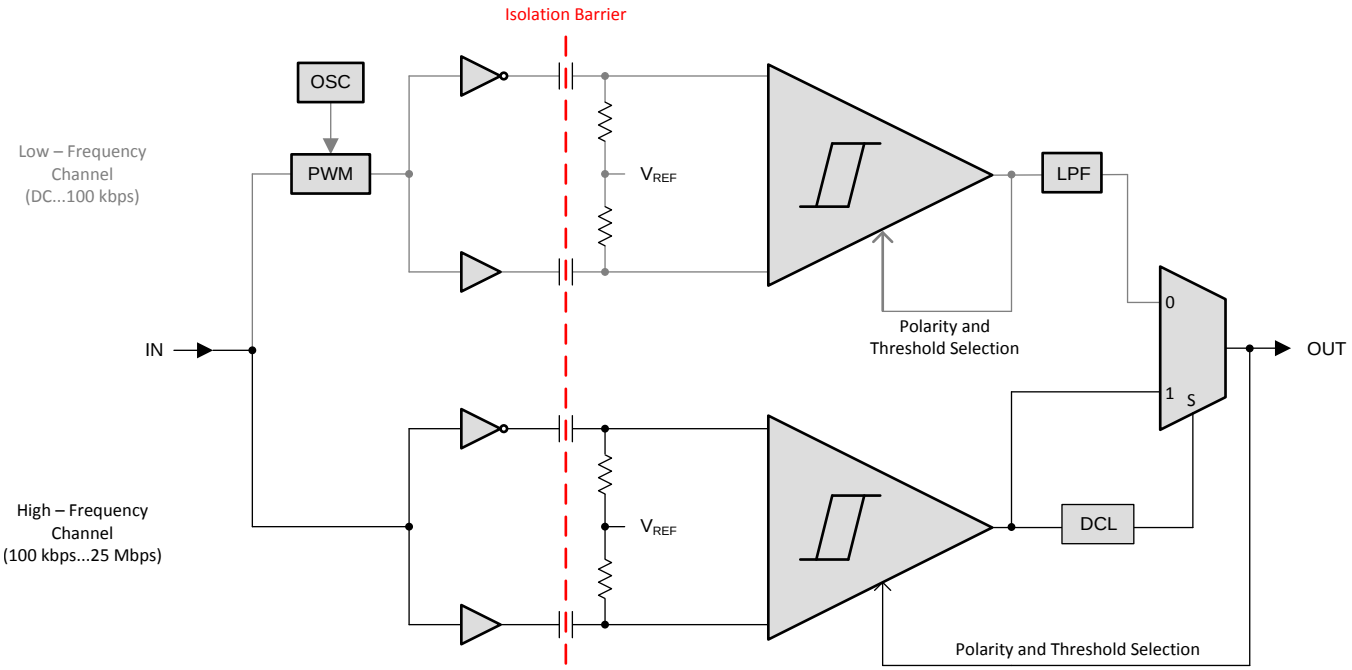


Figure 12. Conceptual Block Diagram of a Digital Capacitive Isolator

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.3 Feature Description

ORDERABLE DEVICE	RATED ISOLATION	MAX DATA RATE	DEFAULT OUTPUT
ISO7310CQDQ1 and ISO7310CQDRQ1	3000 V_{RMS} / 4242 V_{PK} (1)	25 Mbps	High
ISO7310FCQDQ1 and ISO7310FCQDRQ1			Low

(1) See the *Regulatory Information* section for detailed Isolation Ratings

8.3.1 High Voltage Feature Description

8.3.1.1 Insulation and Safety-Related Specifications for D-8 Package

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	400			V
DTI	Minimum internal gap (internal clearance)	Distance through the insulation	13			µm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C		$>10^{11}$		Ω
C_{IO}	Isolation capacitance, input to output(1)	V_{IO} = 0.4 sin (2πft), f = 1 MHz		0.5		pF
C_I	Input capacitance(2)	V_I = V_{CC}/2 + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		1.6		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.1.2 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IOWM}	Maximum isolation working voltage		400	V_{RMS}
V_{IORM}	Maximum repetitive peak voltage per DIN V VDE V 0884-10		566	V_{PK}
V_{PR}	Input-to-output test voltage per DIN V VDE V 0884-10	After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	680	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, Partial Discharge < 5 pC	906	
		Method b1, $V_{PR} = V_{IORM} \times 1.875$, t = 1 s (100% Production test) Partial discharge < 5 pC	1062	
V_{IOTM}	Maximum transient overvoltage per DIN V VDE V 0884-10	$V_{TEST} = V_{IOTM}$ t = 60 sec (qualification) t= 1 sec (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage per DIN V VDE V 0884-10	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 7800\ V_{PK}$ (qualification)	6000	V_{PK}
V_{ISO}	Withstand isolation voltage per UL 1577	$V_{TEST} = V_{ISO} = 3000\ V_{RMS}$, t = 60 sec (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 3600\ V_{RMS}$, t = 1 sec (100% production)	3000	V_{RMS}
R_S	Insulation resistance	V_{IO} = 500 V at T_S = 150°C	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–III

8.3.1.3 Regulatory Information

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK}; Maximum Surge Isolation Voltage, 6000 V_{PK}; Maximum Repetitive Peak Voltage, 566 V_{PK}	400 V_{RMS} Basic Insulation and 200 V_{RMS} Reinforced Insulation working voltage per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2; 300 V_{RMS} Basic Insulation working voltage per CSA 61010-1-12 and IEC 61010-1 3rd Ed.	Single protection, 3000 V_{RMS} (1)	Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Master contract number: 220991	File number: E181974	Certification planned

(1) Production tested ≥ 3600 V_{RMS} for 1 second in accordance with UL 1577.

8.3.1.4 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 119.9 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			190	mA
		$R_{\theta JA}$ = 119.9 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			290	
T_S	Maximum safety temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

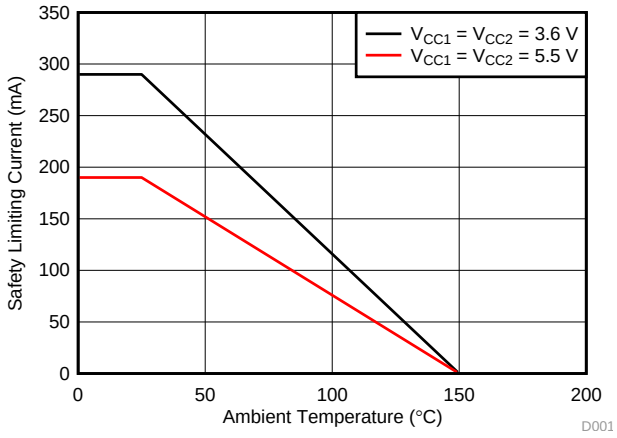


Figure 13. Thermal Derating Curve per VDE

8.4 Device Functional Modes

Table 2 lists the functional modes for the ISO7310-Q1 device.

Table 2. Function Table(1)

V_{CC1}	V_{CC2}	IN	OUT	
			ISO7310CQDQ1 AND ISO7310CQDRQ1	ISO7310FCQDQ1 AND ISO7310FCQDRQ1
PU	PU	H	H	H
		L	L	L
		Open	H(2)	L(3)
PD	PU	X	H(2)	L(3)
X	PD	X	Undetermined	Undetermined

(1) PU = Powered up (V_{CC} ≥ 3 V); PD = Powered down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level
(2) In fail-safe condition, output defaults to high level
(3) In fail-safe condition, output defaults to low level

8.4.1 Device I/O Schematics

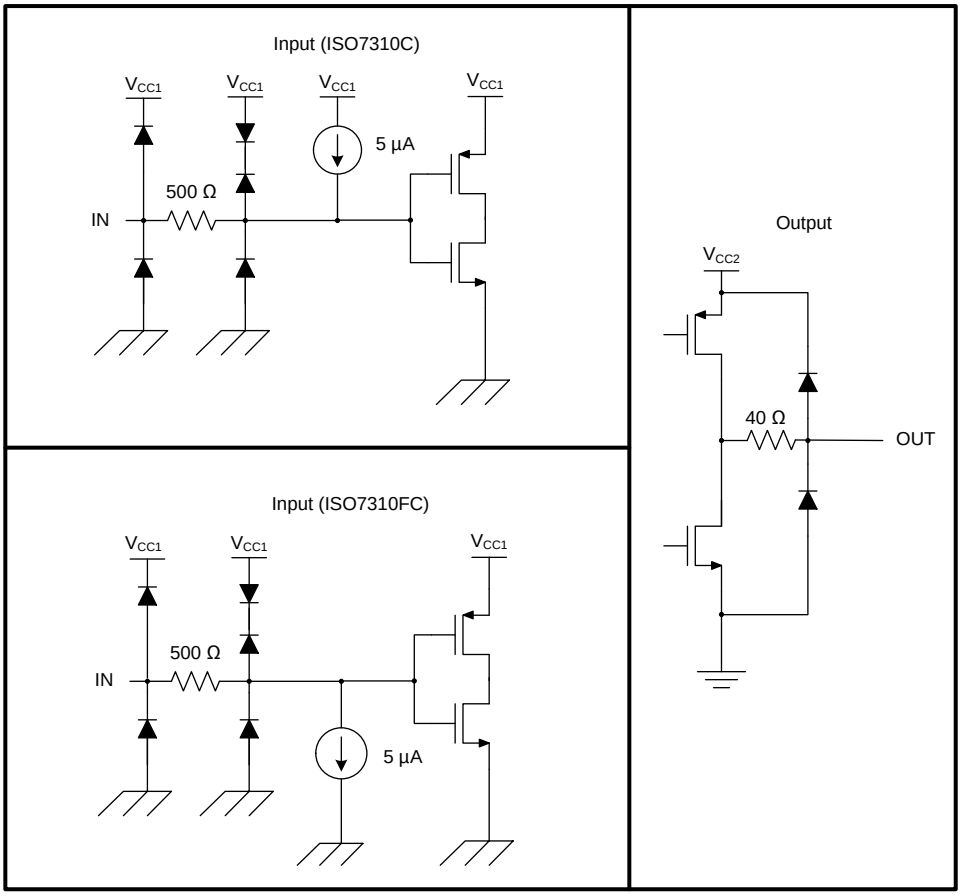


Figure 14. Device I/O Schematics

9 Applications and Implementation

NOTE

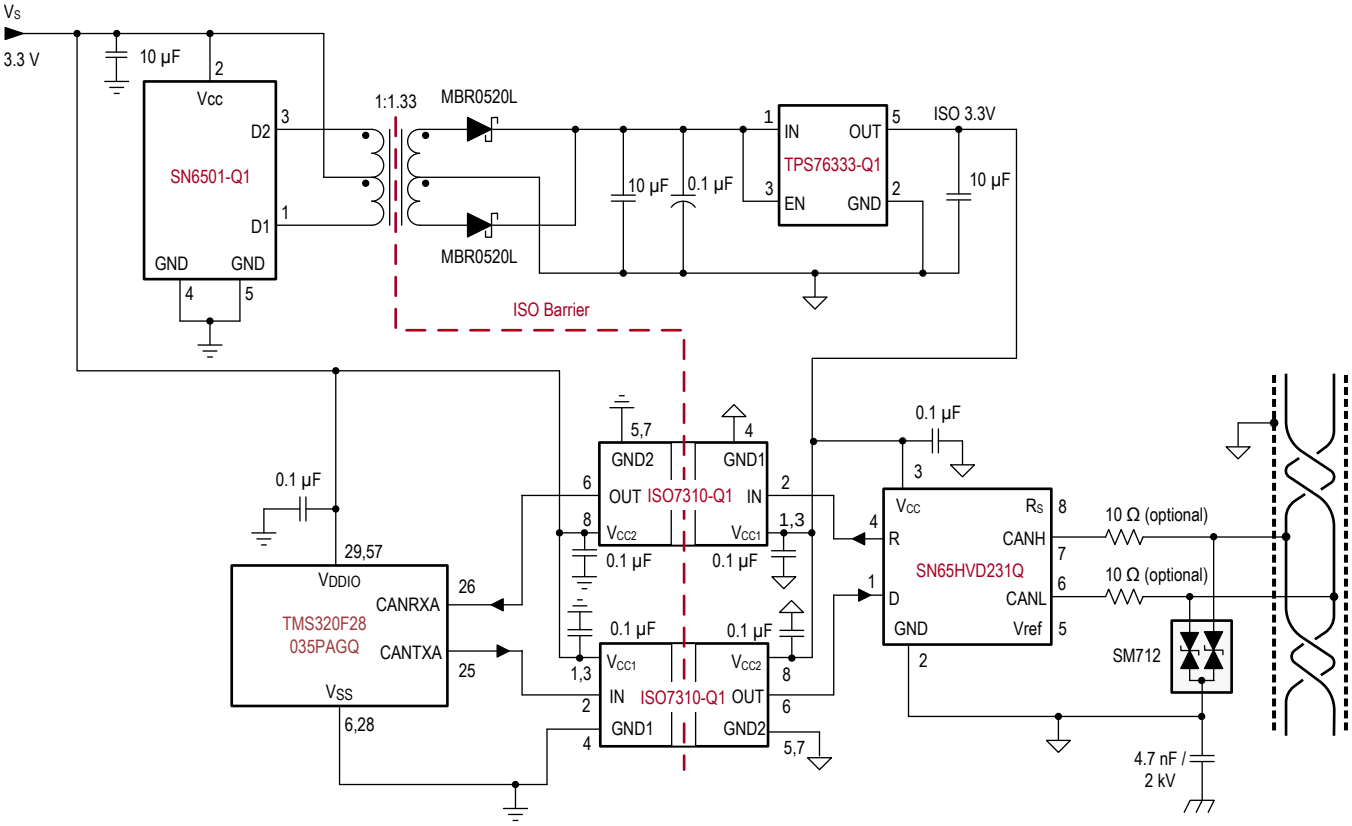
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7310-Q1 device uses single-ended TTL-logic switching technology. The supply voltage range is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (essentially µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7310-Q1 device can be used with a Texas Instruments' microcontroller, CAN transceiver, transformer driver, and low-dropout voltage regulator to create an Isolated CAN Interface as shown in Figure 15.



(1) Multiple pins and capacitors omitted for clarity purpose.

Figure 15. Isolated CAN Interface

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Typical Supply Current Equations

For the equations in this section, the following is true:

- I_{CC1} and I_{CC2} are typical supply currents measured in mA
- f is the data rate measured in Mbps
- C_L is the capacitive load measured in pF

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 0.30517 + (0.01983 \times f) \quad (1)$$

$$I_{CC2} = 1.40021 + (0.02879 \times f) + (0.0021 \times f \times C_L) \quad (2)$$

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 0.18133 + (0.01166 \times f) \quad (3)$$

$$I_{CC2} = 1.053 + (0.01607 \times f) + (0.001488 \times f \times C_L) \quad (4)$$

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7310-Q1 device only requires two external bypass capacitors to operate.

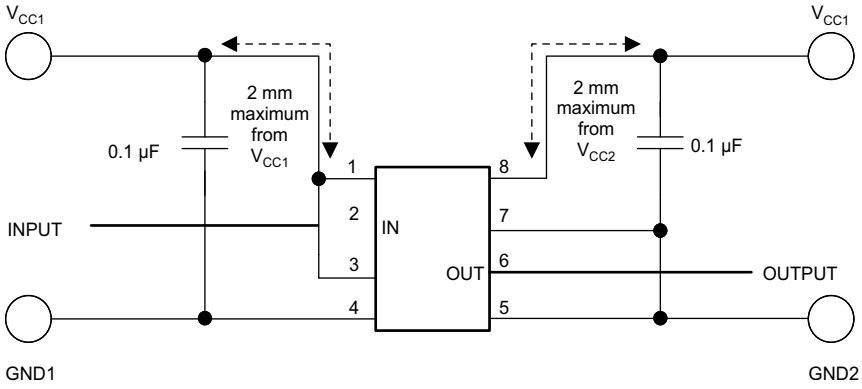


Figure 16. Typical ISO7310-Q1 Circuit Hook-up

9.2.2.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7310-Q1 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

Typical Application (continued)

9.2.3 Application Curves

The following typical eye diagrams of the ISO7310-Q1 device indicate low jitter and wide open eye at the maximum data rate of 25 Mbps.

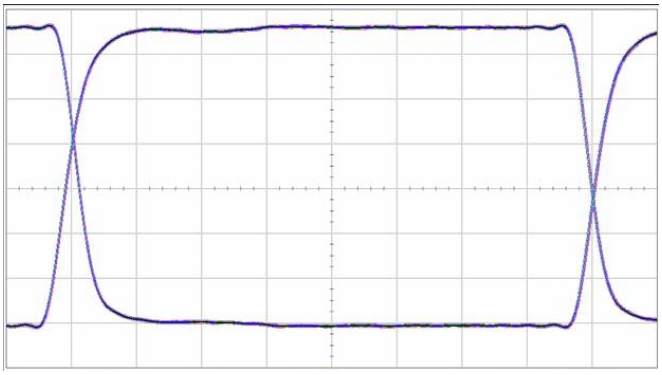


Figure 17. Eye Diagram at 25 Mbps, 5 V and 25°C

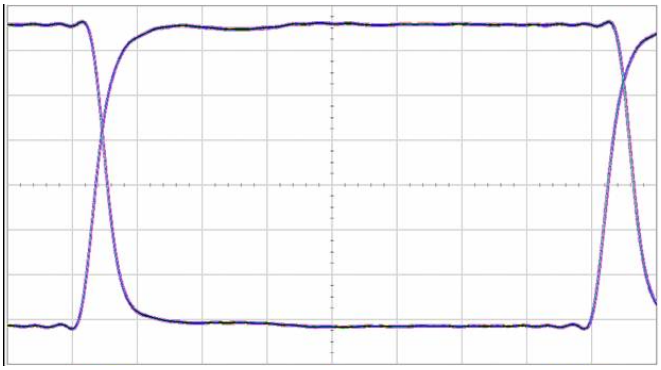


Figure 18. Eye Diagram at 25 Mbps, 3.3 V and 25°C

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501-Q1 device. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501-Q1 datasheet (SLLSEF3).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 19). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the application note SLLA284, *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

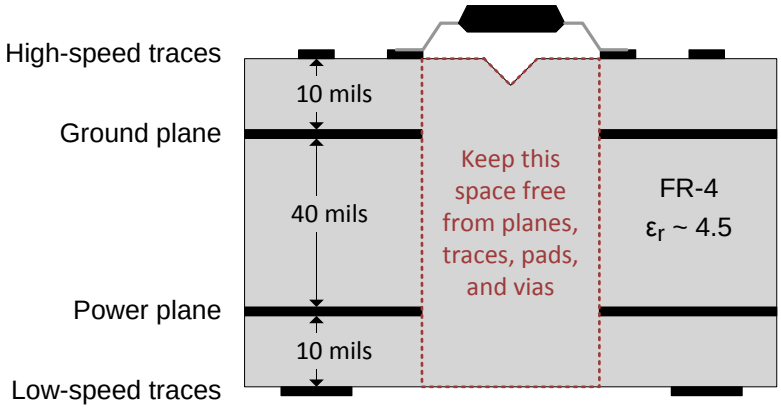


Figure 19. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Digital Isolator Design Guide*, SLLA284
- *ISO7310 Evaluation Module User's Guide*, SLLU206
- *Isolation Glossary*, SLLA353
- *SN6501-Q1 Transformer Driver for Isolated Power Supplies*, SLLSEF3
- *SN65HVD231Q 3.3-V CAN Transceivers*, SGLS398
- *TMS320F28035 Piccolo™ Microcontrollers*, SPRS584
- TPS76333-Q1 *Low-Power 150-mA Low-Dropout Linear Regulators*, SGLS247

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

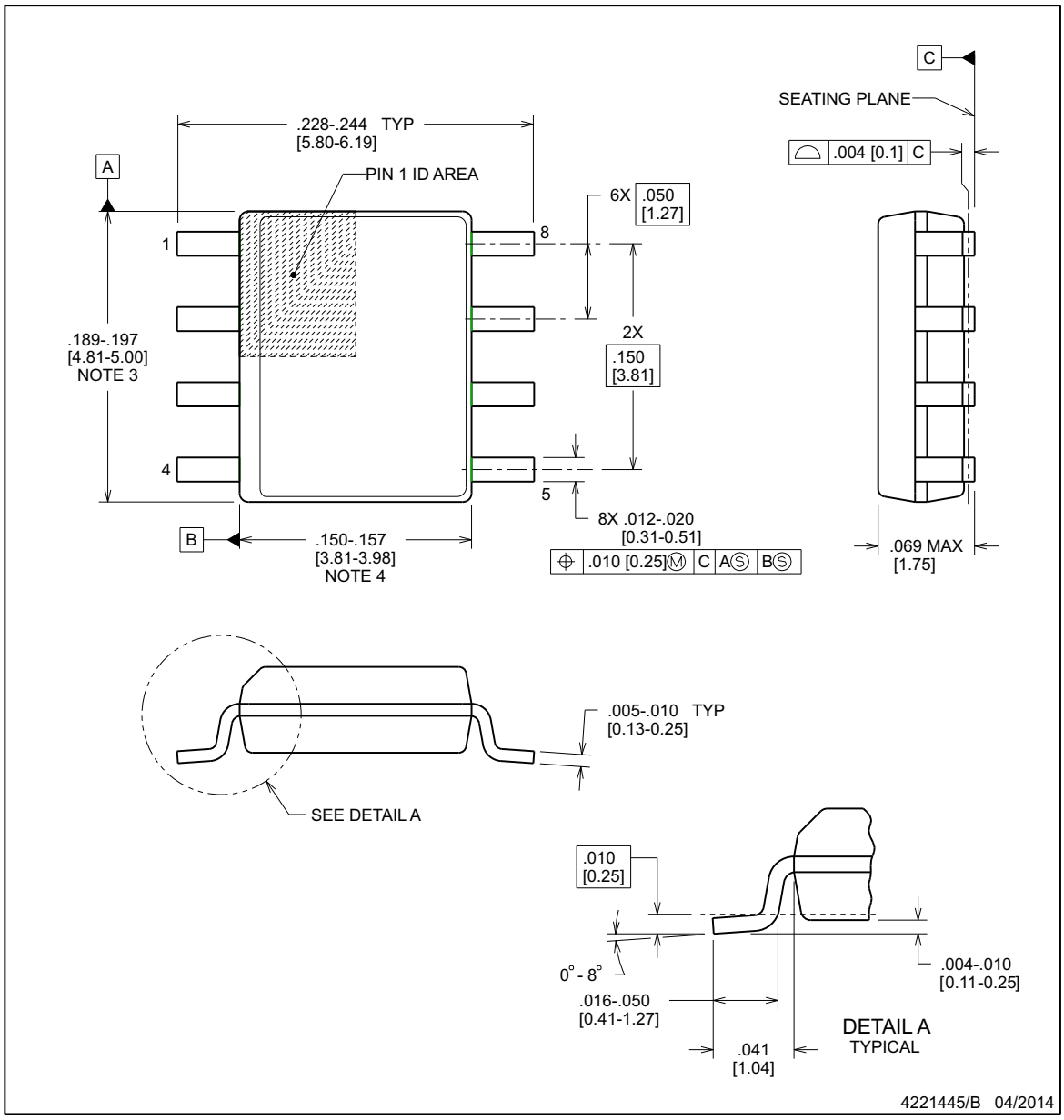
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SOIC



NOTES:

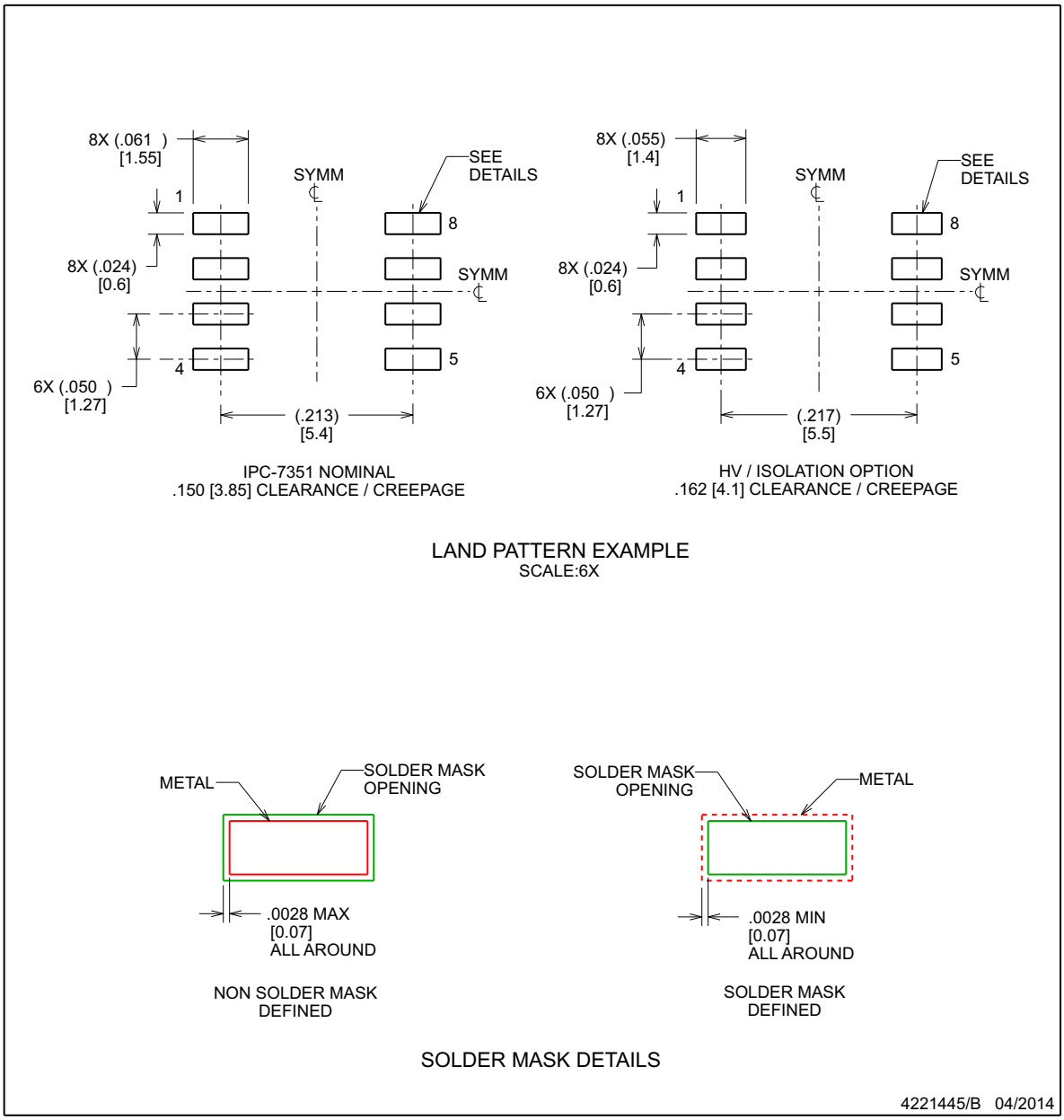
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

SOIC



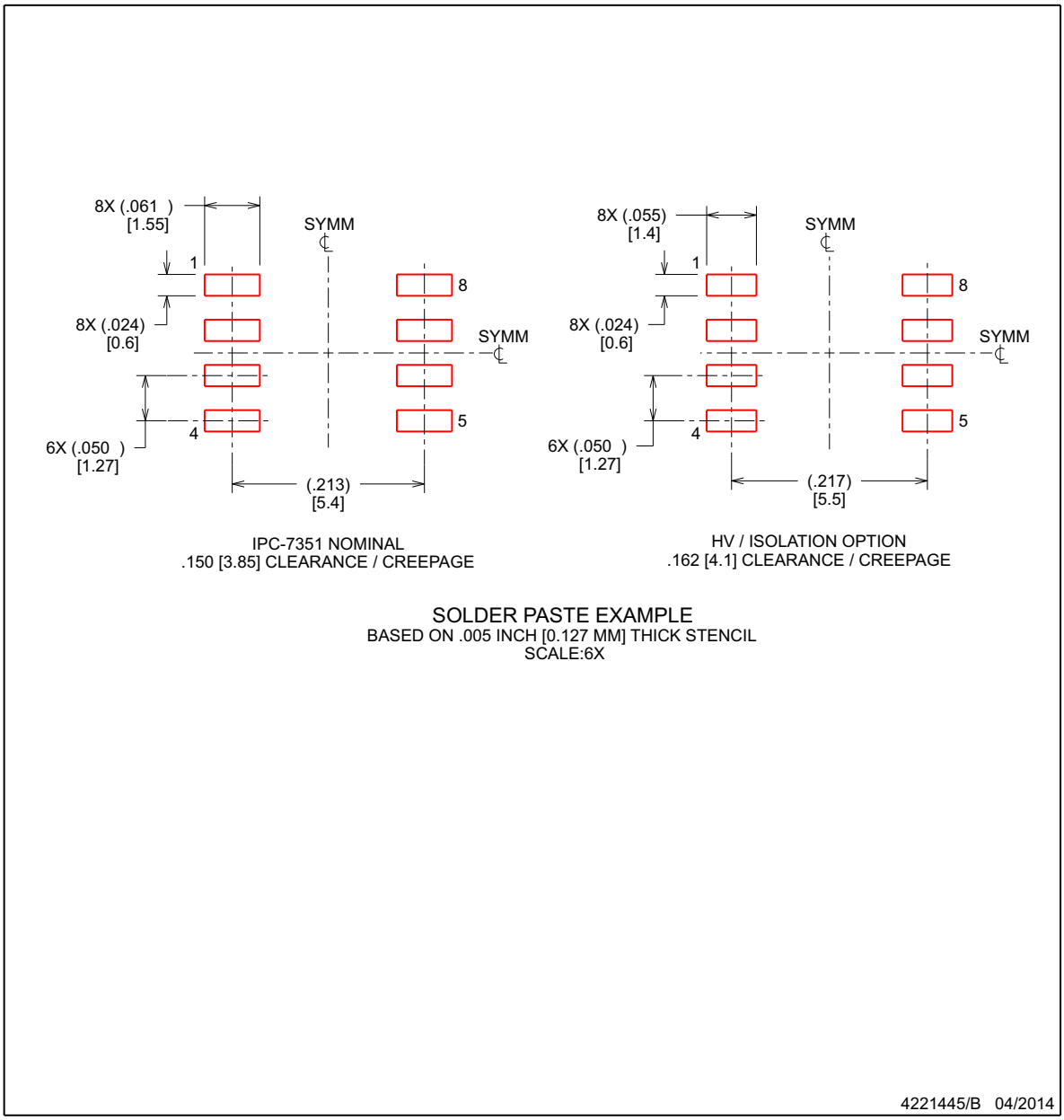
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B — **SOIC - 1.75 mm max height**

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7310CQDQ1	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7310Q
ISO7310CQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7310Q
ISO7310FCQDQ1	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7310FQ
ISO7310FCQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7310FQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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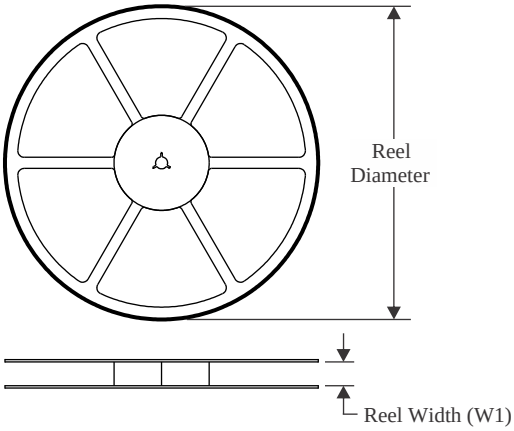
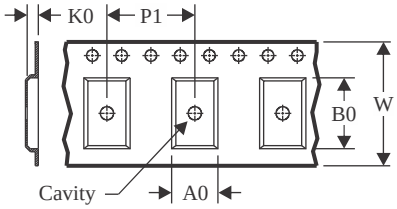
TAPE AND REEL INFORMATION

REEL DIMENSIONS

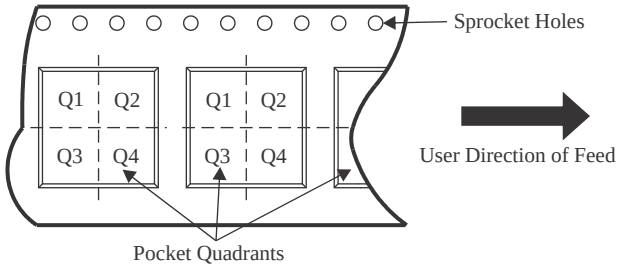


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

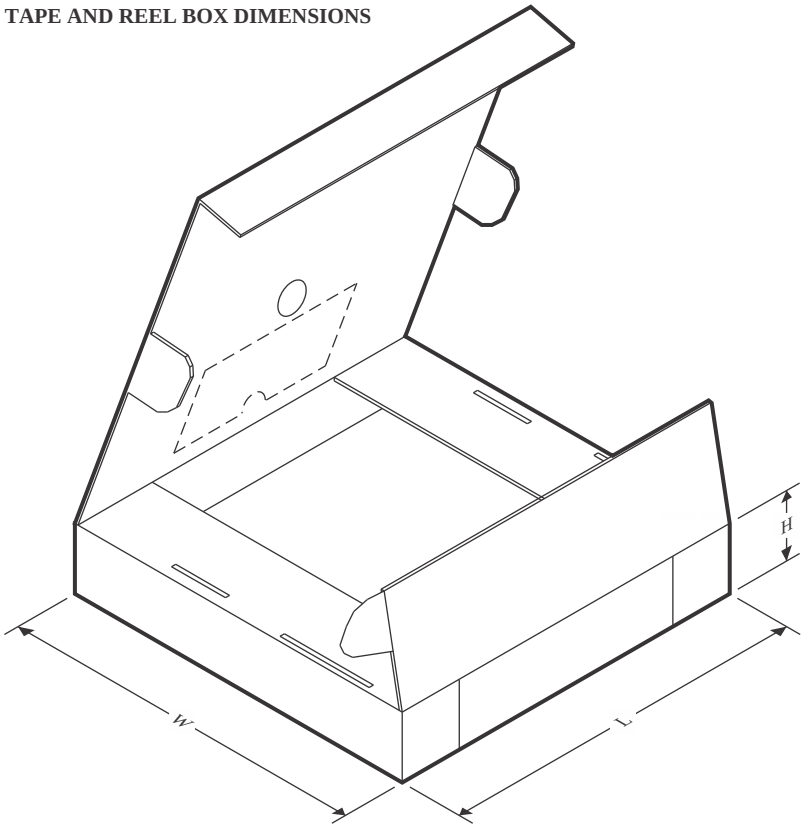
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7310CQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7310FCQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

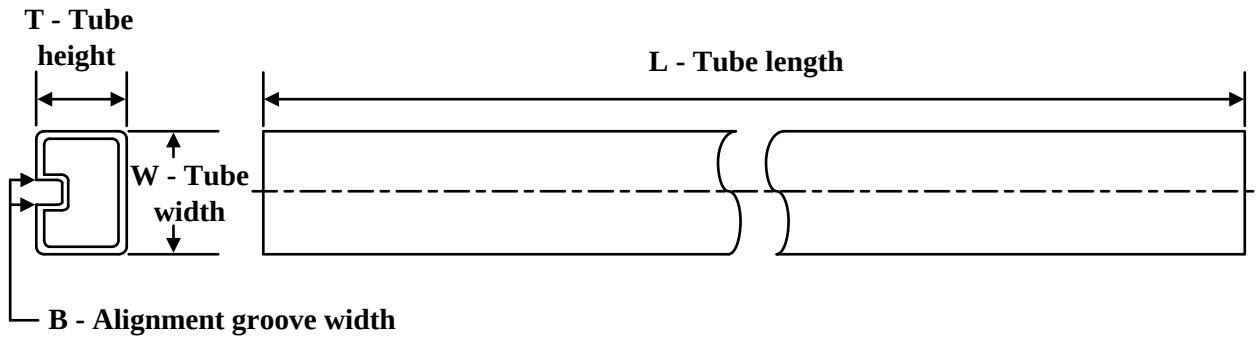
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7310CQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7310FCQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7310CQDQ1	D	SOIC	8	75	505.46	6.76	3810	4
ISO7310FCQDQ1	D	SOIC	8	75	505.46	6.76	3810	4

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