

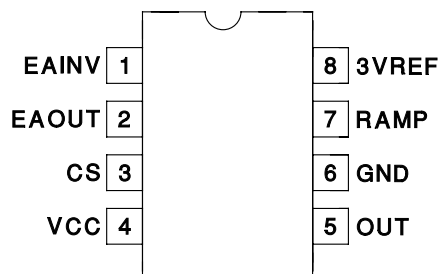
ABSOLUTE MAXIMUM RATINGS

VCC	35V
EAINV	-0.6V to VCC
IEAOUT	25mA
RAMP	-0.3V to 4V
CS	-0.3V to VCC
Iout	-0.7A to 0.7A
I3VREF	15mA
Storage Temperature	-65°C to +150°C
Junction Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (TOP VIEW)
D, N or J Packages



ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1572	-55°C to +125°C	J
UC2572	-40°C to +85°C	D, N or J
UC3572	0°C to +70°C	D or N

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 5V, CT = 680pF, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
3VREF		2.94	3	3.06	V
Line Regulation	VCC = 4.75 to 30V		1	10	mV
Load Regulation	I3VREF = 0V to -5mA		1	10	mV
Oscillator Section					
Frequency	VCC = 5V to 30V	85	100	115	kHz
Error Amp Section					
EAINV	EAOUT = 2V	-10	0	10	mV
	IEANV = -1mA		-0.2	-0.9	V
IEAINV	EAOUT = 2V		-0.2	-1.0	μA
AVOL	EAOUT = 0.5V to 3V	65	90		dB
EAOUT High	EAINV = -100mV	3.6	4	4.4	V
EAOUT Low	EAINV = 100mV		0.1	0.2	V
IEAOUT	EAINV = -100mV, EAOUT = 2V	-350	-500		μA
	EAINV = 100mV, EAOUT = 2V	7	20		mA
Unity Gain Bandwidth	TJ = 25°C, F = 10kHz	0.6	1		MHz
Current Sense Comparator Section					
Threshold		0.185	0.205	0.225	V
Input Bias Current	CS = 0		-0.4	-1	μA
CS Propagation Delay			300		nS

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 5V, CT = 680pF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Drive Output Section					
OUT High Saturation	I _{OUT} = 0		0	0.3	V
	I _{OUT} = -10mA		0.7	1.5	V
	I _{OUT} = -100mA		1.5	2.5	V
OUT Low Saturation	I _{OUT} = 10mA		0.1	0.4	V
	I _{OUT} = 100mA		1.5	2.2	V
Rise Time	T _J = 25°C, C _{LOAD} = 1nF + 3.3 Ohms		30	80	nS
Fall Time	T _J = 25°C, C _{LOAD} = 1nF + 3.3 Ohms		30	80	nS
Pulse Width Modulator Section					
Maximum Duty Cycle	EAINV = +100mV, VCC = 5V to 30V		92	96	%
Minimum Duty Cycle	EAINV = -100mV, VCC = 5V to 30V			0	%
Modulator Gain	EAOUT = 1.5V to 2.5V	45	55	65	%/V
Undervoltage Lockout Section					
Start Threshold		3.5	4.2	4.5	V
Hysteresis		100	200	300	mV
Sleep Mode Section					
Threshold		1.8	2.2	2.6	V
Supply Current Section					
IVCC	VCC = 5V, 30V		9	15	mA
	VCC = 30, CS = 3V		50	150	μA

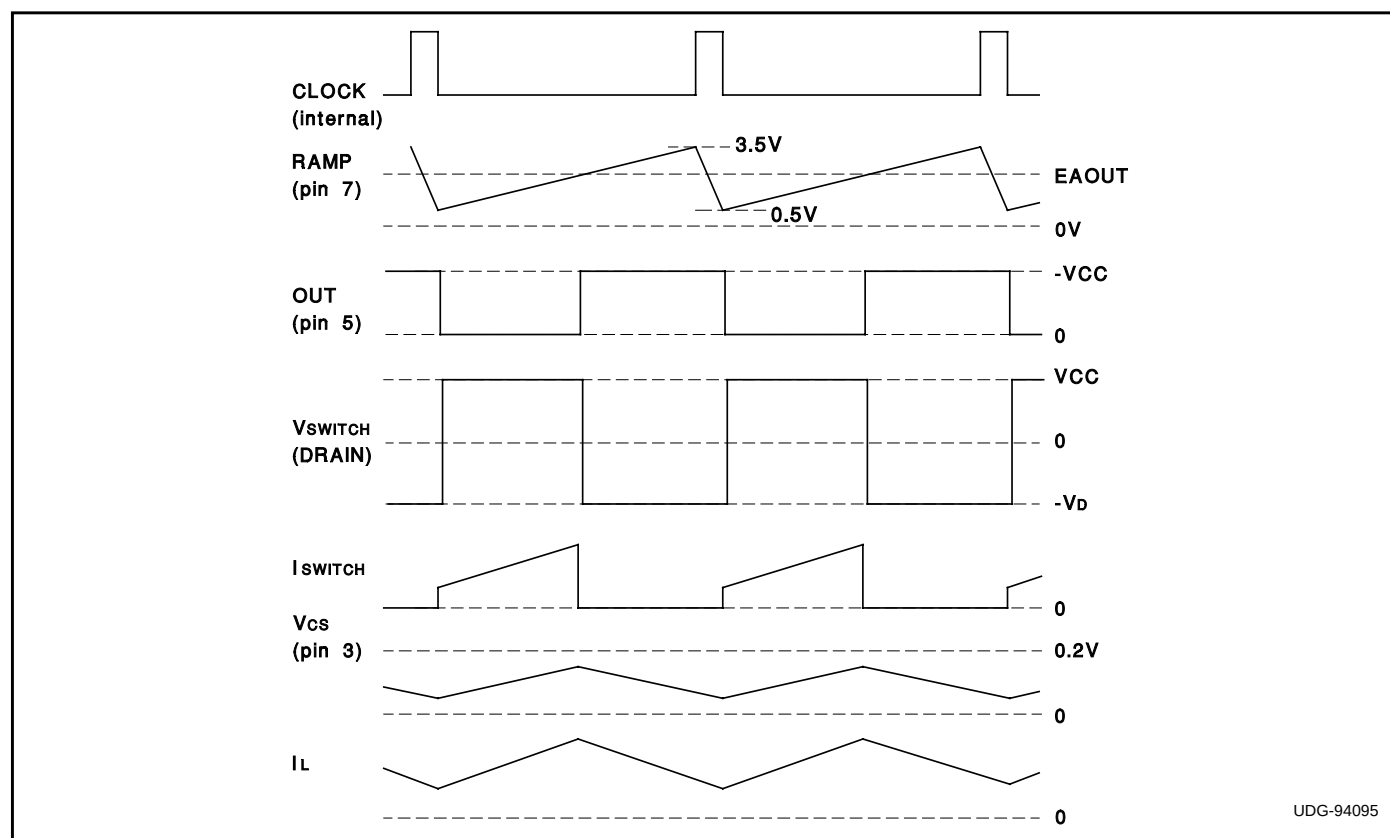


Figure 1. Typical waveforms.

PIN DESCRIPTIONS

3VREF: Precision 3V reference. Bypass with 100nF capacitor to GND.

CS: Current limit sense pin. Connect to a ground referenced current sense resistor in series with the flyback inductor. OUT will be held high (PMOS switch off) if CS exceeds 0.2V.

EAINV: Inverting input to error amplifier. Summing junction for 3VREF and VOUT sense. The non-inverting input of the error amplifier is internally connected to GND. This pin will source a maximum of 1mA.

EAOUT: Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

GND: Circuit Ground.

OUT: Gate drive for external PMOS switch connected between Vcc and the flyback inductor. OUT drives the gate of the PMOS switch between Vcc and GND.

RAMP: Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k \cdot C_{RAMP}}$$

Recommended operating frequency range is 10kHz to 200kHz.

VCC: Input voltage supply to chip. Range is 4.75 to 30V. Bypass with a 1μF capacitor.

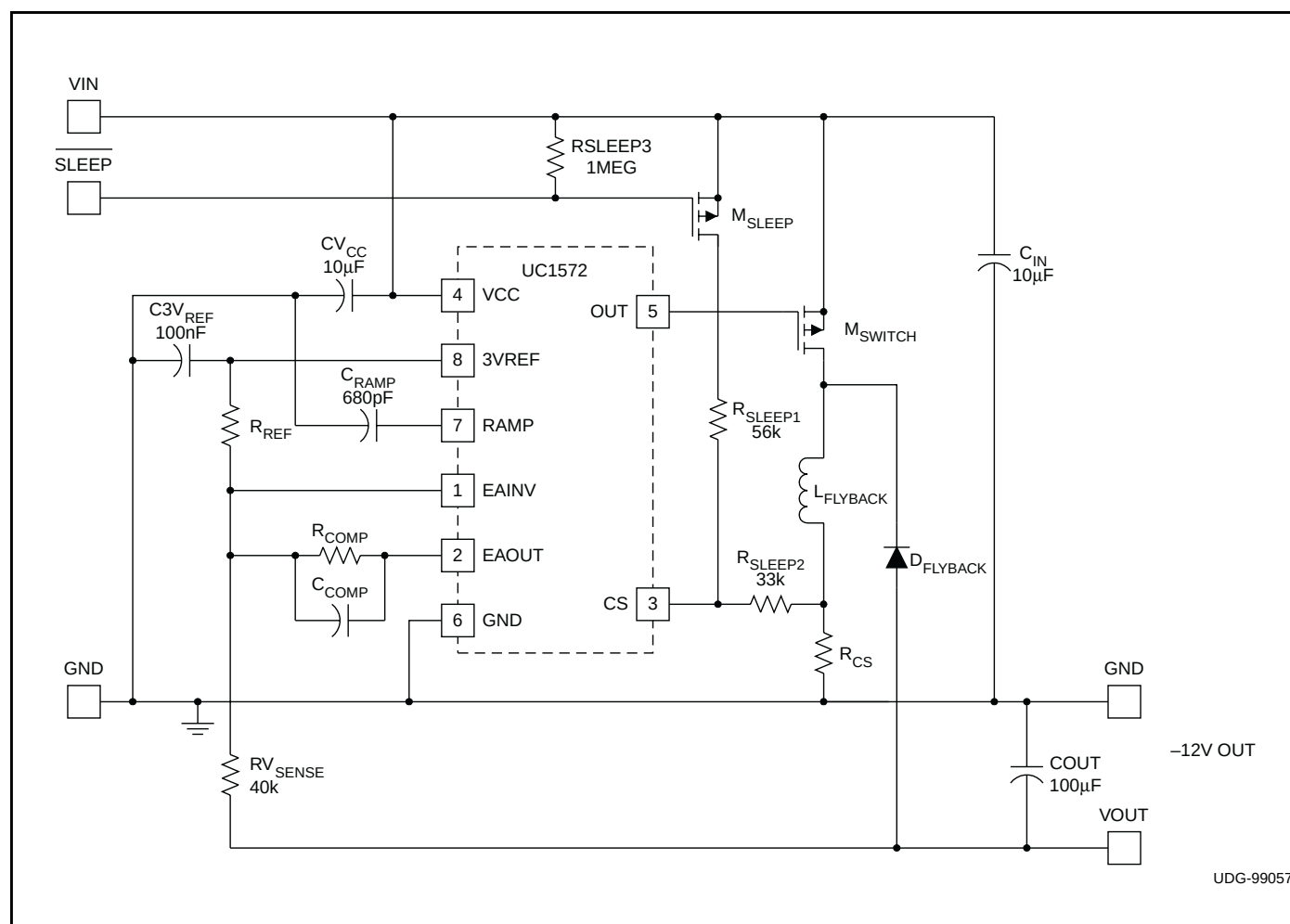


Figure 2. Typical application: +5V to -12V flyback converter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2572D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2572D	Samples
UC2572DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2572D	Samples
UC2572DTR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2572D	Samples
UC3572D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3572D	Samples
UC3572DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3572D	Samples
UC3572DTR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3572D	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

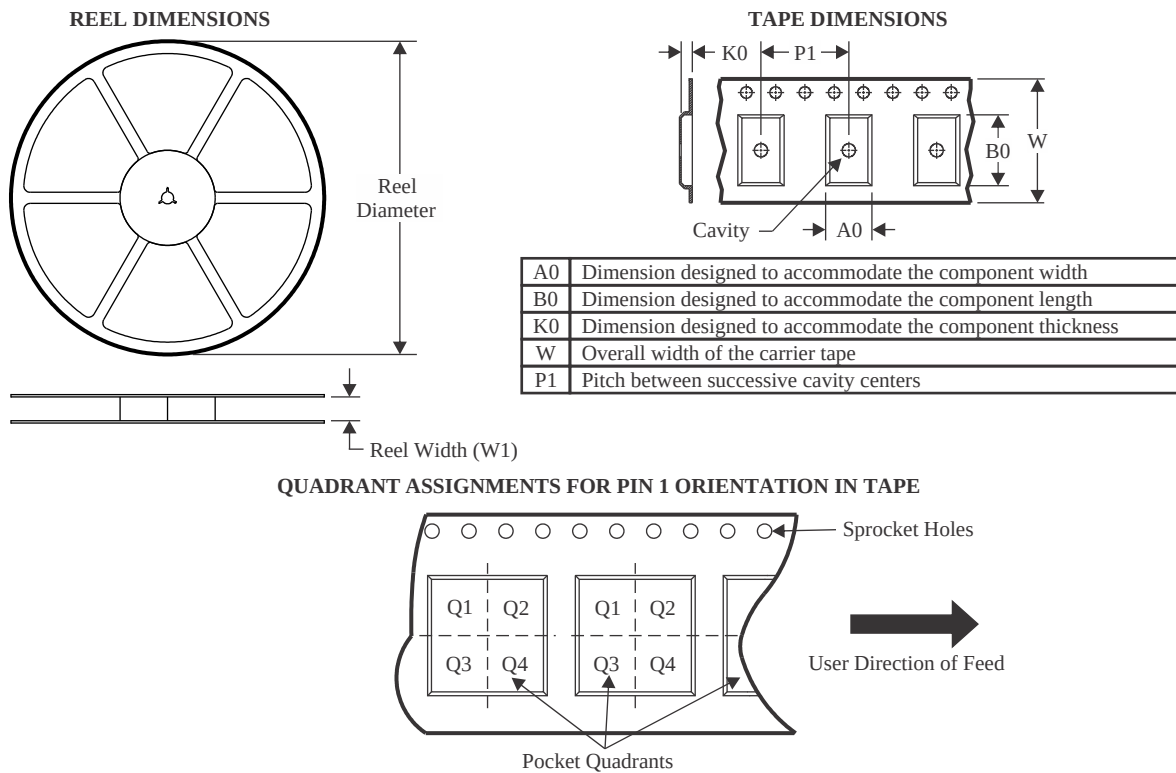
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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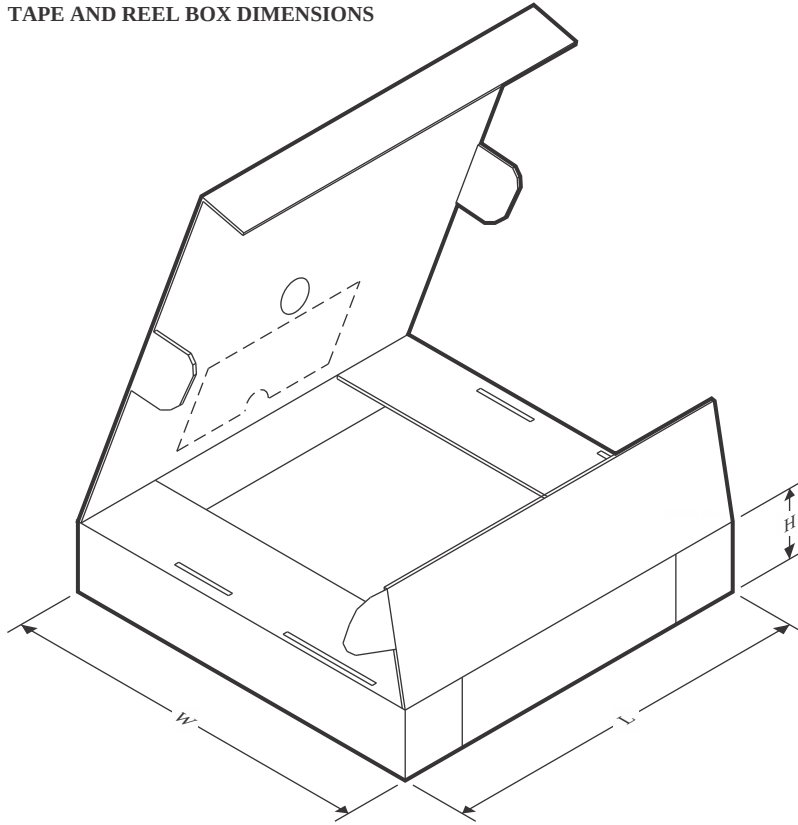
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2572DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3572DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

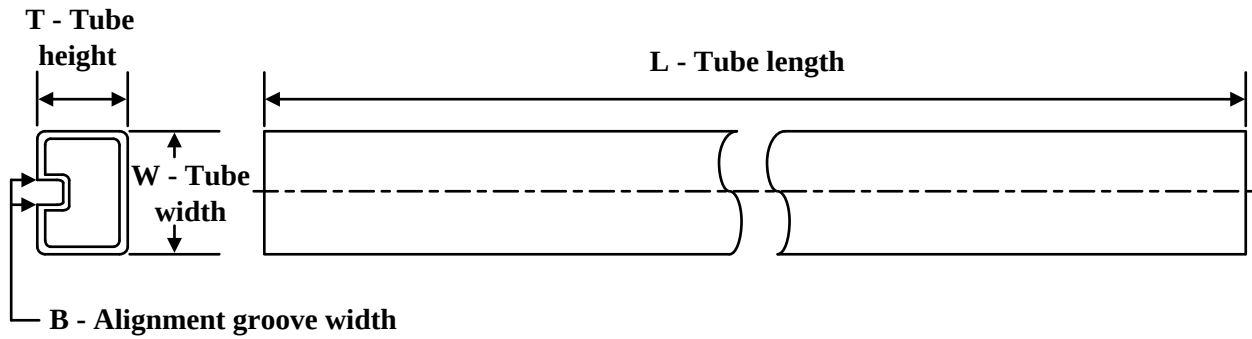
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2572DTR	SOIC	D	8	2500	340.5	338.1	20.6
UC3572DTR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UC2572D	D	SOIC	8	75	507	8	3940	4.32
UC2572DG4	D	SOIC	8	75	507	8	3940	4.32
UC3572D	D	SOIC	8	75	507	8	3940	4.32
UC3572DG4	D	SOIC	8	75	507	8	3940	4.32

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