R9A02G015

ASSP (USB Power Delivery Controller)

R19DS0101EJ0100
Rev.1.00
Mar 29, 2019

1. OUTLINE

1.1 Features

Ultra-low power consumption technology
- V_{DD} = single power supply voltage of 2.7 to 5.5 V
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core
- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: 0.04167 µs: @ 24 MHz operation with high-speed on-chip oscillator
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 7 KB

Code flash memory
- Code flash memory: 128 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory
- Data flash memory: 2 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 2.7 to 5.5 V

High-speed on-chip oscillator
- Select from 48 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: ±1.0% (V_{DD} = 2.7 to 5.5 V, T_A = -20 to +85°C)

Operating ambient temperature
- T_A = -40 to +85°C (A: Consumer applications)

Power management and reset function
- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select reset from 6 levels)

USB
- Complying with USB Specification Revision 2.0, incorporating host/function controller
- Corresponding to full-speed transfer (12 Mbps) and low-speed (1.5 Mbps)
- Complying with Battery Charging Specification Revision 1.2
- Compliant with the 2.1 A/1.0 A charging mode.

Serial interfaces
- CSI: 2 channels
- UART: 1 channel
- Simplified I^2C: 2 channels
- I^2C: 2 or 3 channels

Timers
- 16-bit timer: 8 channels
- 12-bit interval timer: 1 channel
- Watchdog timer: 1 channel

A/D converter
- 8/10-bit resolution A/D converter (V_{DD} = 2.7 to 5.5 V)
- Analog input: 8 channels
- Internal reference voltage (1.45 V) and temperature sensor

I/O ports
- I/O port: 23 or 28 (N-ch open drain I/O [withstand voltage of 6 V]: 5, N-ch open drain I/O [V_{DD} withstand voltage]: 8 or 13)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- On-chip clock output/buzzer output controller

Others
- On-chip BCD (binary-coded decimal) correction circuit

Remark
The functions mounted depend on the product.
See **1.6 Outline of Functions**.

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ROM, RAM capacities

Flash ROM	Data flash	RAM	R9A02G015	
			32 pins (with USB)	32 pins (without USB)
128 KB	2 KB	7 KB Note	R9A02G0150	R9A02G0151

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.

R9A02G0150/R9A02G0151: Start address FE300H

1.2 Ordering Information

Figure 1 - 1 Part Number and Package of R9A02G015

Pin count	Package	Ordering Part Number	Remarks
32 pins	32-pin QFN (4 × 4 mm, 0.4 mm pitch)	R9A02G015020GNP#AC0	Product with USB (R9A02G0150)
		R9A02G015120GNP#AC0	Product without USB (R9A02G0151)

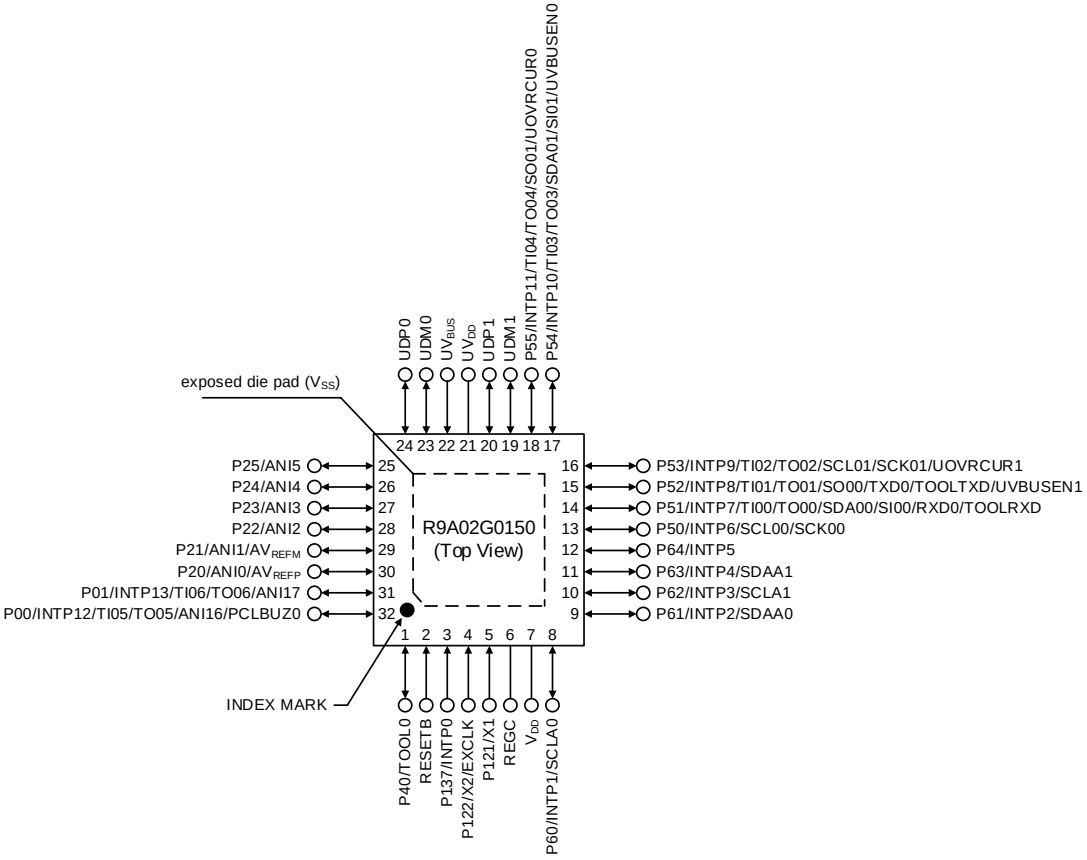
Caution **The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

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1.3 Pin Configuration (Top View)

1.3.1 32-pin product (with USB)

• 32-pin QFN (4 × 4 mm, 0.4 mm pitch)



Caution 1. Connect the exposed die pad (V_{SS}) to ground.

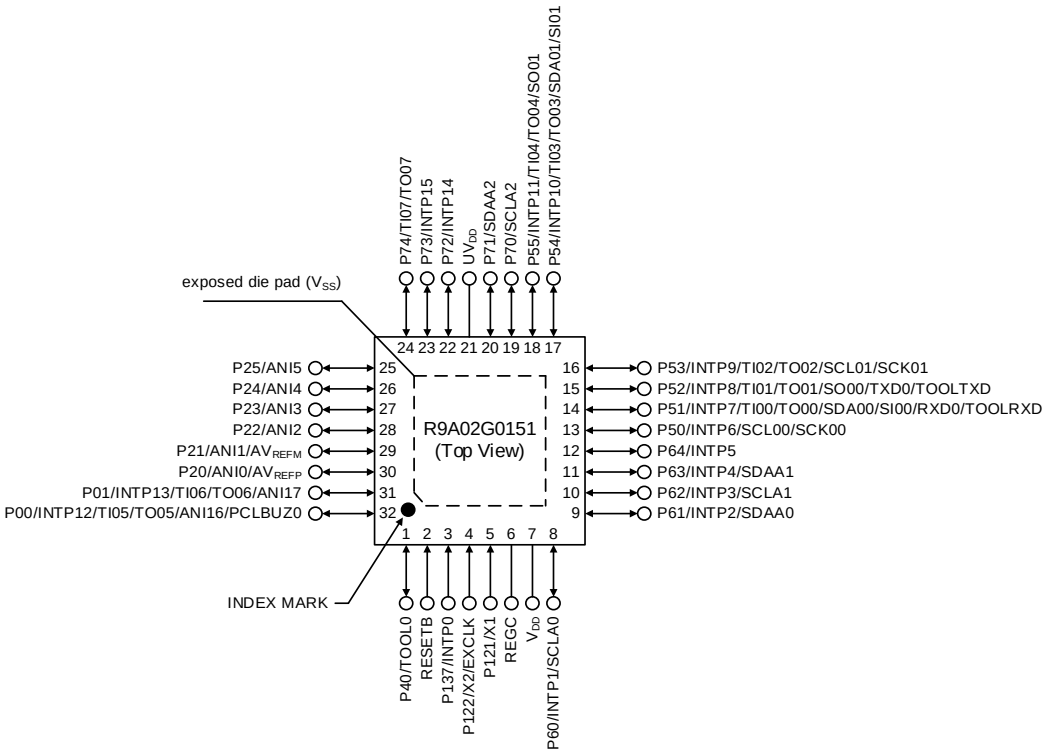
Caution 2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 µF).

Remark For pin identification, see **1.4 Pin Identification**.

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1.3.2 32-pin product (without USB)

• 32-pin QFN (4 × 4 mm, 0.4 mm pitch)



Caution 1. Connect the exposed die pad (V_{SS}) to ground.

Caution 2. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 µF).

Remark For pin identification, see **1.4 Pin Identification**.

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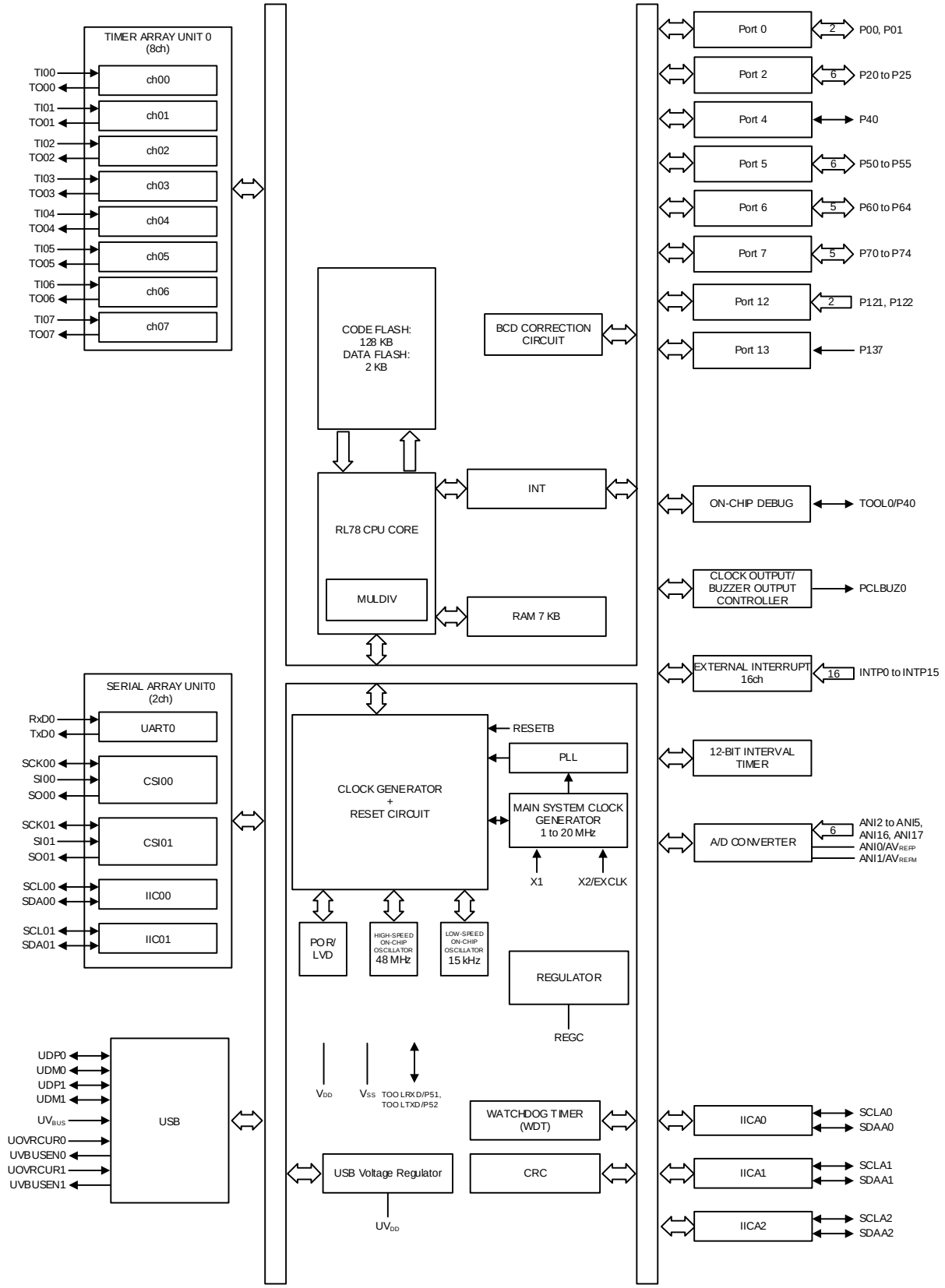
1.4 Pin Identification

ANI0 to ANI5, ANI16, ANI17:	Analog input
AV_{REFM}:	A/D converter reference potential (- side) input
AV_{REFP}:	A/D converter reference potential (+ side) input
EXCLK:	External clock input (main system clock)
INTP0 to INTP15:	External interrupt input
P00, P01:	Port 0
P20 to P25:	Port 2
P40:	Port 4
P50 to P55:	Port 5
P60 to P64:	Port 6
P70 to P74:	Port 7
P121, P122:	Port 12
P137:	Port 13
PCLBUZ0:	Programmable clock output/buzzer output
REGC:	Regulator capacitance
RESETB:	Reset
RxD0:	Receive data
SCK00, SCK01:	Serial clock input/output
SCLA0 to SCLA2, SCL00, SCL01:	Serial clock input/output
SDAA0 to SDAA2, SDA00, SDA01:	Serial data input/output
SI00, SI01:	Serial data input
SO00, SO01:	Serial data output
TI00 to TI07:	Timer input
TO00 to TO07:	Timer output
TOOL0:	Data input/output for tool
TOOLRXD, TOOLTXD:	Data input/output for external device
TxD0:	Transmit data
UDM0, UDM1, UDP0, UDP1:	USB Input/Output
UOVRCUR0, UOVRCUR1:	USB Input
UVBUSEN0, UVBUSEN1:	USB Output
UV_{DD}:	USB Power Supply/USB Regulator Capacitance
UV_{BUS}:	USB Input/USB Power Supply (USB Optional BC)
V_{DD}:	Power supply
V_{SS}:	Ground
X1, X2:	Crystal oscillator (main system clock)

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1.5 Block Diagram

1.5.1 32-pin products



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1.6 Outline of Functions

(1/2)

Item		32-pin (with USB)	32-pin (without USB)
		R9A02G0150	R9A02G0151
Code flash memory (KB)		128 KB	
Data flash memory (KB)		2 KB	
RAM		7KB Note 1	
Address space		1 MB	
Main system clock	High-speed system clock (f_{MX})	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V)	
	High-speed on-chip oscillator clock (f_{IH}) Max: 24 MHz	HS (High-speed main) mode: 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V)	
	PLL clock	6, 12, 24 MHz Note 2: V_{DD} = 2.7 to 5.5 V	
Subsystem clock	Low-speed on-chip oscillator clock(f_{IL})	15 kHz (TYP.): V_{DD} = 2.7 to 5.5 V	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f_{HOCO} = 48MHz/f_{IH} = 24 MHz operation)	
		0.04167 μs (PLL clock: f_{PLL} = 48 MHz/f_{IH} = 24 MHz Note 2 operation)	
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	23	28
	CMOS I/O	15	20
	CMOS input	3	
	N-ch open-drain I/O (6 V tolerance)	5	
Timer	16-bit timer	8 channels	
	Watchdog timer	1 channel	
	12-bit interval timer	1 channel	
	Timer output	7	8
Clock output/buzzer output		1	
		2.93 kHz, 5.86 kHz, 11.7 kHz, 1.5 MHz, 3 MHz, 6 MHz (Main system clock: f_{MAIN} = 24 MHz operation)	
10-bit resolution A/D converter		8 channels	
Serial interface		CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels	
	I^2C bus	2 channels	3 channels

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(2/2)

Item		32-pin (with USB)	32-pin (without USB)
		R9A02G0150	R9A02G0151
USB	Host controller	2 channels	—
	Function controller	1channel	—
Vectored interrupt sources	Internal	22	21
	External	14	16
Reset		• Reset by RESETB pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note 3 • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset: 1.51 ± 0.04 V (T_A = -40 to +85°C) • Power-down-reset: 1.50 ± 0.04 V (T_A = -40 to +85°C)	
Voltage detector	Power on	2.81 V to 4.06 V (6 stages)	
	Power down	2.75 V to 3.98 V (6 stages)	
On-chip debug function		Provided (Enable to tracing)	
Power supply voltage		V_{DD} = 2.7 to 5.5 V	
Operating ambient temperature		T_A = -40 to +85°C	

Note 1. The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.

R9A02G0150/R9A02G0151: Start address FE300H

Note 2. In the PLL clock 48 MHz operation, the system clock is 2/4/8 dividing ratio.

Note 3. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

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2. ELECTRICAL SPECIFICATIONS

The target products A: Consumer applications; T_A = -40 to +85°C
R9A02G0150, R9A02G0151

Cautions 1. The R9A02G015 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2 Functions other than port pins in the R9A02G015 User's Manual.

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2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
UV_{DD} pin input voltage	V_{IUVDD}	UV_{DD}	−0.3 to V_{DD} +0.3	V
Input voltage	V_{I1}	P00, P01, P20 to P25, P40, P50 to P55, P70 to P74, P121, P122, P137, RESETB	−0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60 to P64 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	UDP0, UDM0, UDP1, UDM1	−0.3 to +6.5	V
	V_{I4}	UV_{BUS}	−0.3 to +6.5	V
Output voltage	V_{O1}	P00, P01, P20 to P25, P40, P50 to P55, P70 to P74	−0.3 to V_{DD} +0.3 Note 2	V
	V_{O2}	UDP0, UDM0, UDP1, UDM1	−0.3 to +6.5	V
Analog input voltage	V_{AI1}	ANI16, ANI17	−0.3 to V_{DD} +0.3 and −0.3 to AV_{REF} (+) +0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI5	−0.3 to V_{DD} +0.3 and −0.3 to AV_{REF} (+) +0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. AV_{REF} (+) : The + side reference voltage of the A/D converter. This can be selected from AV_{REFP}, the internal reference voltage (1.45 V), and V_{DD}.

3. V_{SS} : Reference voltage

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Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00, P01, P40, P50 to P55, P70-P74	−40	mA
		Total of all pins −170 mA	P00, P01, P40	−70	mA
			P50 to P55, P70 to P74	−100	mA
	I_{OH2}	Per pin	P20 to P25	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00, P01, P40, P50 to P55, P60 to P64, P70 to P74	40	mA
		Total of all pins 170 mA	P00, P01, P40	70	mA
			P50 to P55, P60 to P64, P70 to P74	100	mA
	I_{OL2}	Per pin	P20 to P25	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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2.2 Oscillator Characteristics

2.2.1 X1 oscillator characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{HOCO}		1		48	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85 °C	–1.0		+1.0	%
		–40 to –20 °C	–1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

2.2.3 PLL oscillator characteristics

(T_A = –40 to +85°C, 2.7V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
PLL input frequency Note	f_{PLLIN}	High-speed system clock	6.00		16.00	MHz
PLL output frequency Note	f_{PLL}			48.00		MHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

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2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00, P01, P40, P50 to P55, P70 to P74	Normal input buffer	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00, P01, P50 to P55, P70 to P74	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 2.7 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
	V_{IH3}	P20 to P25		0.7V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P64		0.7V_{DD}		6.0	V
	V_{IH5}	P121, P122, P137, RESETB		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00, P01, P40, P50 to P55, P70 to P74	Normal input buffer	0		0.2V_{DD}	V
	V_{IL2}	P00, P01, P50 to P55, P70 to P74	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 2.7 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P25		0		0.3V_{DD}	V
	V_{IL4}	P60 to P64		0		0.3V_{DD}	V
	V_{IL5}	P121, P122, P137, RESETB		0		0.2V_{DD}	V

Caution The maximum value of V_{IH} of pins P00, P01, P50-P55, and P70-P74 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00, P01. P40, P50 to P55, P70 to P74	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –1.5 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P25	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P00, P01, P40, P50 to P55, P70 to P74	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
	V_{OL2}	P20 to P25	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P64	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.4	V

Caution P00, P01, P50-P55, and P70-P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00, P01, P20 to P25, P40, P50 to P55, P60 to P64, P70 to P74, P137, RESETB	V_I = V_{DD}				1	μA
	I_{LIH2}	P121, P122	V_I = V_{DD}	In input port or external clock input			1	μA
Input leakage current, low	I_{LIL1}	P00, P01, P20 to P25, P40, P50 to P55, P60 to P64, P70 to P74, P137, RESETB	V_I = V_{SS}				–1	μA
	I_{LIL2}	P121, P122	V_I = V_{SS}	In input port or external clock input			–1	μA
On-chip pll-up resistance	R_U	P00, P01, P40, P50 to P55, P70 to P74	V_I = V_{SS}, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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2.3.2 Supply current characteristics

(T_A = 25 °C, V_{DD} = 3.3 V , V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (High-speed main) mode	f_{HOCO} = 48 MHz f_{IH} = 24 MHz Note 2		2.8		mA
				f_{HOCO} = 24 MHz f_{IH} = 24 MHz Note 2		2.6		mA
	I_{DD2} Note 3	HALT mode	HS (High-speed main) mode	f_{HOCO} = 48 MHz f_{IH} = 24 MHz Note 4		0.92		mA
				f_{HOCO} = 24 MHz f_{IH} = 24 MHz Note 4		0.72		mA
	I_{DD3} Note 5	STOP mode				0.26		μA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, or V_{SS}. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed system clock is stopped.

3. During HALT instruction execution by flash memory.

4. When high-speed system clock and Low-speed on-chip oscillator clock are stopped.

5. Not including the current flowing into the 12-bit interval timer and watchdog timer.

Remarks 1. f_{HOCO}: High-speed on-chip oscillator clock frequency (Max. 48 MHz)

2. f_{IH}: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2, 4, or 8 (Max. 24 MHz)

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(T_A = 25 °C, V_{DD} = UV_{DD} = 3.3 V , V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB operating current Note 1	I_{USBF} Note 2	During USB communication operation under the following settings and conditions: • The function controller is set to operate in full-speed mode • The internal power supply for the USB is stopped. • f_{HOCO} = 48MHz, f_{IH} = 24MHz		1.8		mA
	I_{SUSP} Note 3	During suspended state under the following settings and conditions: • The function controller is set to full-speed mode (the UDP0 pin is pulled up). • The internal power supply for the USB is stopped. • The system is set to STOP mode (When the high-speed on-chip oscillator and high-speed system clock are stopped. When the watchdog timer is stopped.).		180		μA

Notes 1. Current flowing into V_{DD} and UV_{DD}.

2. Current consumed only by the USB module.

3. Includes the current supplied from the pull-up resistor of the UDP0 pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.

Remarks 1. f_{HOCO}: High-speed on-chip oscillator clock frequency (Max. 48 MHz)

2. f_{IH}: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2, 4, or 8 (Max. 24 MHz)

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2.4 AC Characteristics

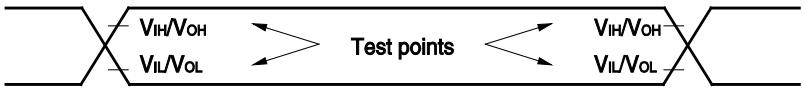
2.4.1 Basic operation

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

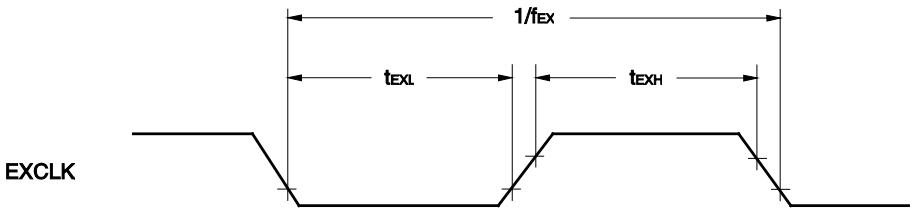
Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (High-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
		In the self programming mode	HS (High-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP15	2.7 V ≤ V_{DD} ≤ 5.5 V		1			μs
RESETB low-level width	t_{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

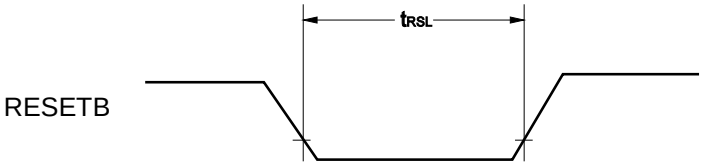
AC Timing Test Points



External System Clock Timing



RESETB Input Timing



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2.5 Peripheral Functions Characteristics

2.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

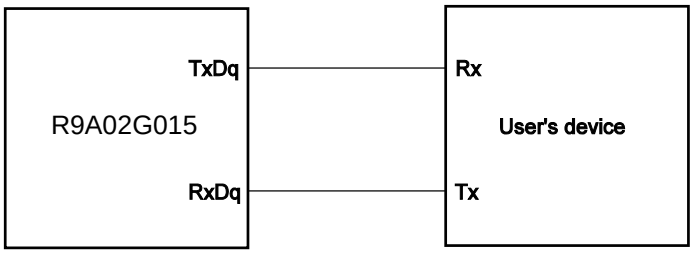
(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note			4.0	Mbps

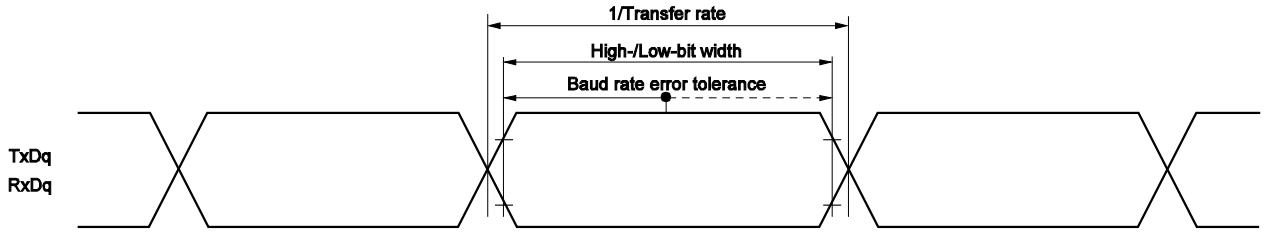
Note The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0), g: PIM and POM number (g = 5)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

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(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	83.3			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 7$			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 10$			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		23			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		33			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 5.5 V		10			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 20 pF Note 4				10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 5)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

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(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	167			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 – 12			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 – 18			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		44			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			19			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4				25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM numbers (g = 5)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

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(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	16 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 – 7			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 – 8			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK}+20			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK}+31			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK}+44	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

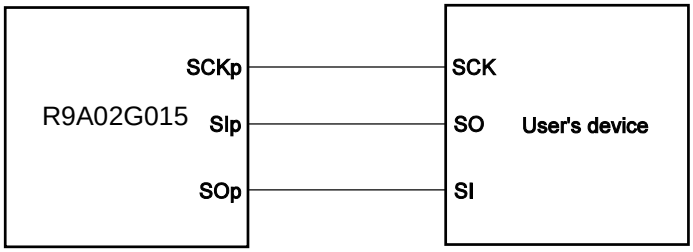
Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01), m: Unit number (m = 0),
n: Channel number (n = 0, 1), g: PIM number (g = 0, 5, 7)

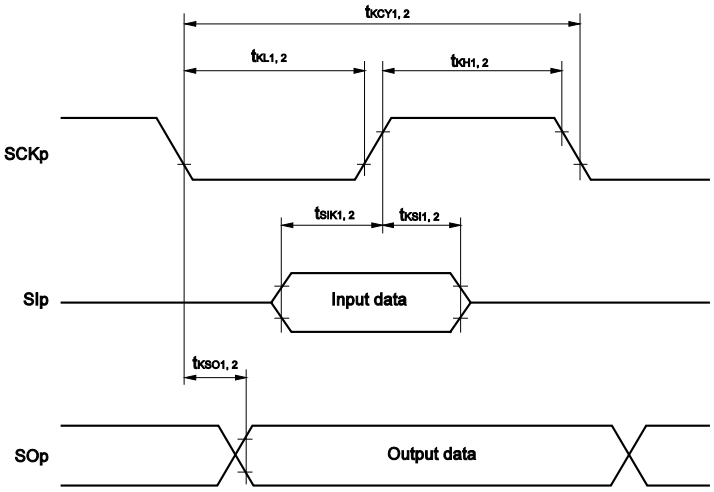
2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

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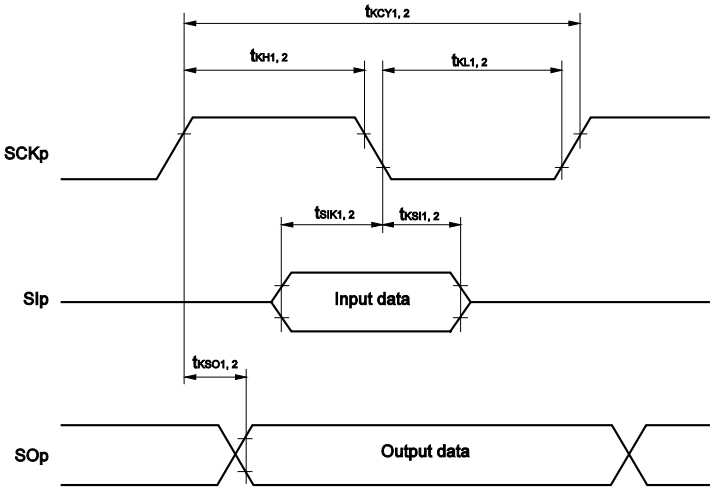
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01)

2. m: Unit number, n: Channel number (mn = 00, 01)

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(5) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1	kHz
		2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 85 Note 2		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 145 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	ns
		2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	ns

Notes 1. The value must also be equal to or less than $f_{MCK}/4$.

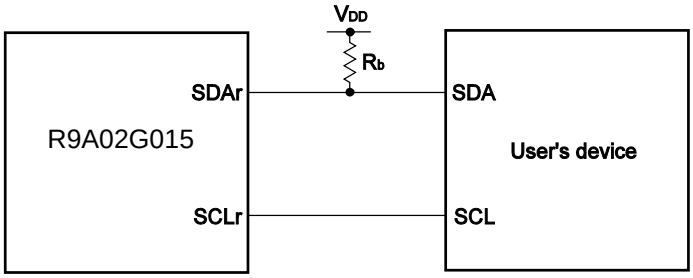
2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

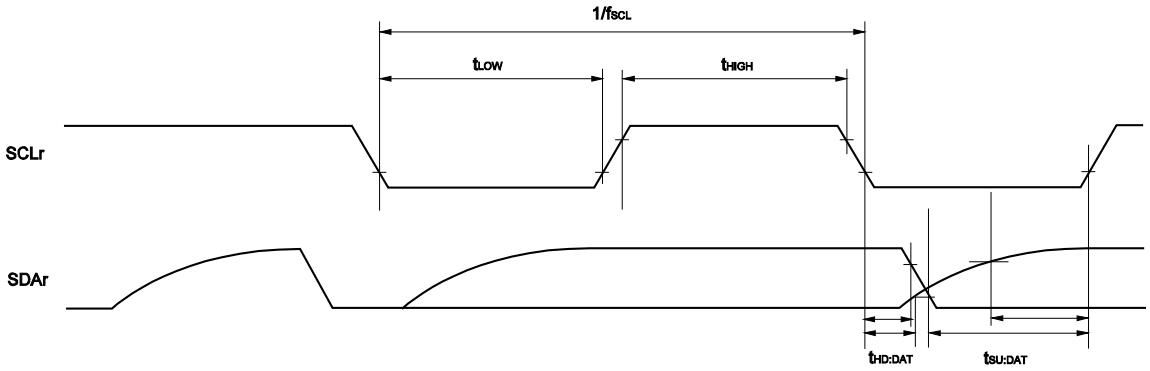
(**Caution** and **Remarks** are listed on the next page.)

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Simplified I²C mode mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remarks 1. R_b[Ω]:Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 01), g: PIM number (g = 5), h: POM number (h = 5)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01)

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(6) Communication at different potential (2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V				$f_{MCK}/6$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 2			4.0	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V				$f_{MCK}/6$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 2			4.0	Mbps

Notes 1. Use it with $V_{DD} \geq V_b$.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0), g: PIM and POM number (g = 5)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00)

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(6) Communication at different potential (2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		transmission	4.0 V ≤ V_{DD} ≤ 5.5 V,				**Note 1**	bps
			2.7 V ≤ V_b ≤ 4.0 V	Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V			2.8 Note 2	Mbps
			2.7 V ≤ V_{DD} < 4.0 V				**Note 3**	bps
			2.3 V ≤ V_b ≤ 2.7 V	Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V			1.2 Note 4	Mbps

Notes 1. The smaller maximum transfer rate derived by using fMCK/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ VDD ≤ 5.5 V and 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-Cb \times Rb \times \ln(1 - \frac{2.2}{Vb})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-Cb \times Rb \times \ln(1 - \frac{2.2}{Vb})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using fMCK/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ VDD < 4.0 V and 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-Cb \times Rb \times \ln(1 - \frac{2.0}{Vb})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-Cb \times Rb \times \ln(1 - \frac{2.0}{Vb})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

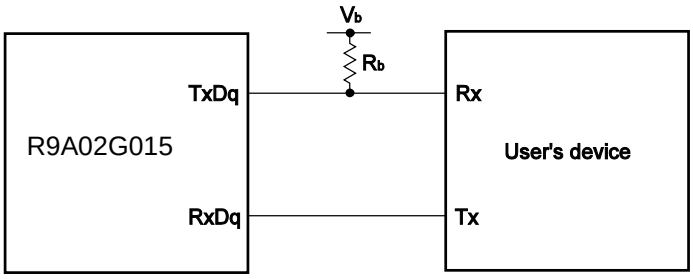
* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

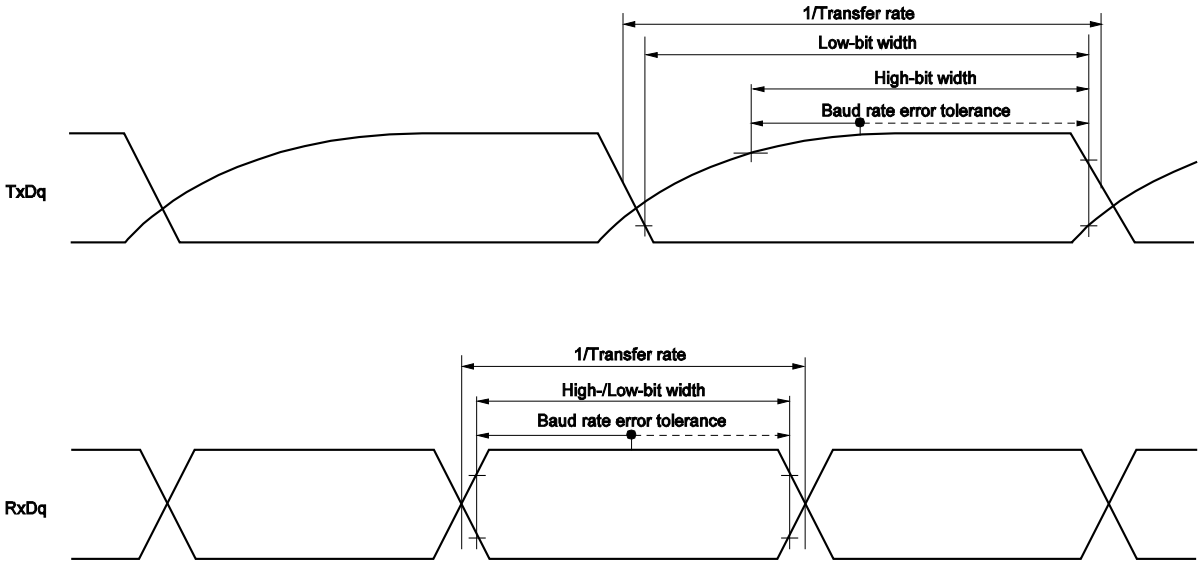
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Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

2. q: UART number (q = 0), g: PIM and POM number (g = 5)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

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(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200			ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300			ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 50			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 120			ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 7			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 10			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		58			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121			ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10			ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ				60	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ				130	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		23			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		33			ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10			ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ				10	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ				10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(**Caution** and **Remark** are listed on the next page.)

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Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM number (g = 5)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00)

4. This value is valid only when CSI00's peripheral I/O redirect function is not used.

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(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)
(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300			ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500			ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 75			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 170			ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 12			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 18			ns

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. Use it with $V_{DD} \geq V_b$.

(**Remarks** are listed two pages after the next page.)

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(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177			ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19			ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			195	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44			ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19			ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			25	ns

(**Notes**, **Cautions** and **Remarks** are listed on the next page.)

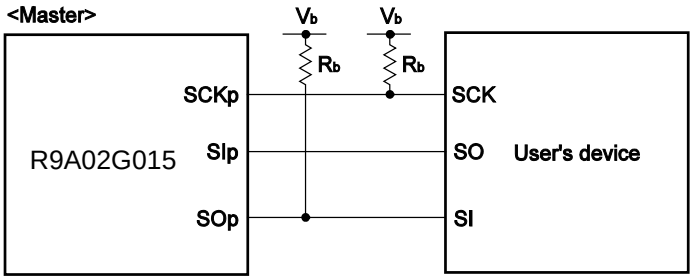
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Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



Remarks 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

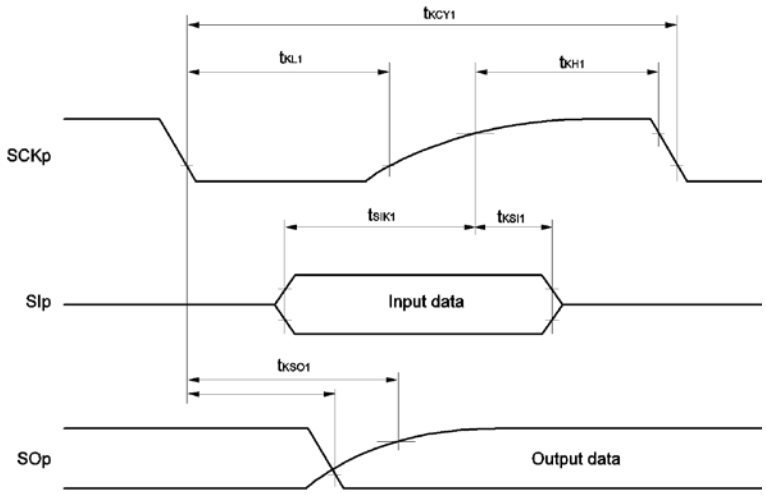
2. p: CSI number (p = 00), m: Unit number, n: Channel number (mn = 00), g: PIM and POM number (g = 5)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

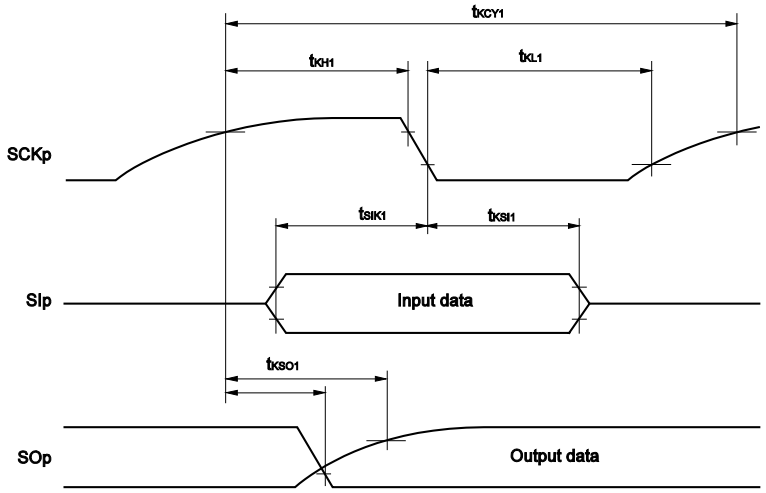
4. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

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CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00), m: Unit number, n: Channel number (mn = 00), g: PIM and POM number (g =5)

2. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

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(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 – 12			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 18			ns
SIp setup time (to SCKp↑) Note 2	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 20			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20			ns
SIp hold time (from SCKp↑) Note 3	t_{KSI2}			1/f_{MCK} + 31			ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ				2/f_{MCK} + 214	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

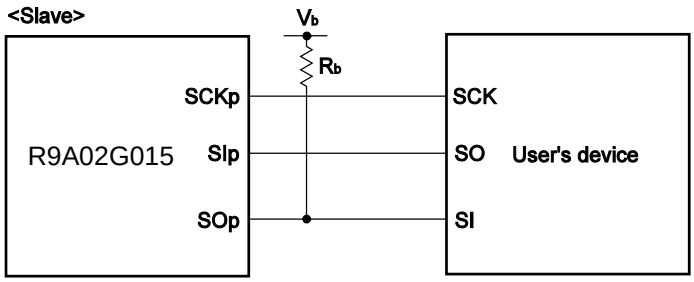
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(**Caution** and **Remarks** are listed on the next page.)

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Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



Remarks 1. R_b[Ω]:Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

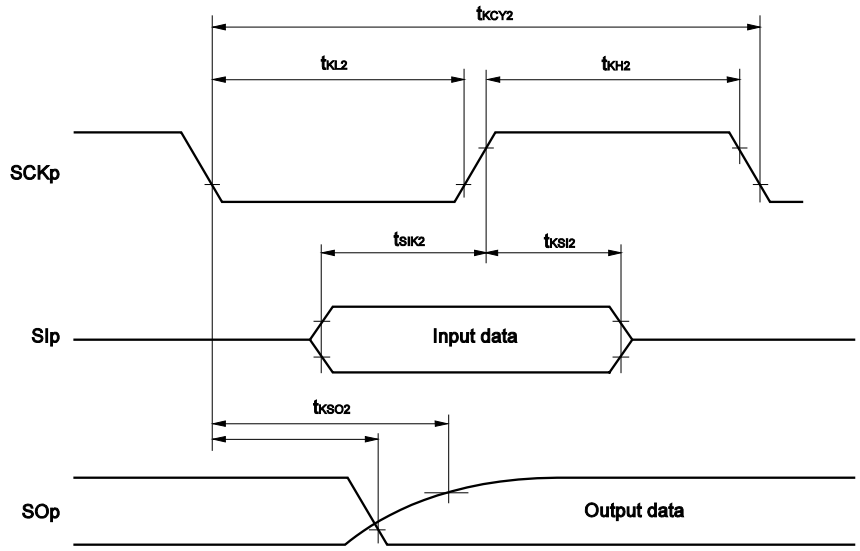
2. p: CSI number (p = 00), m: Unit number, n: Channel number (mn = 00), g: PIM and POM number (g = 5)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

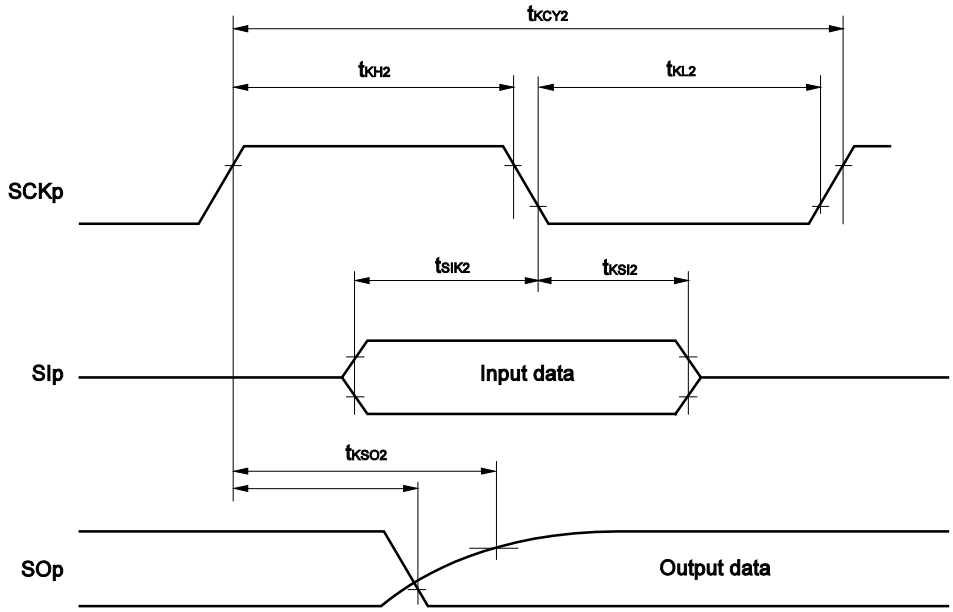
4. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

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CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00), m: Unit number, n: Channel number (mn = 00),
g: PIM and POM number (g = 5)

2. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

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(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (1/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1	kHz
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		400 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1150		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		ns
Hold time when SCLr = “H”	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	245		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	675		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

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(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (2/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 Note 2		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 Note 2		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	$1/f_{MCK}$ + 190 Note 2		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 190 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

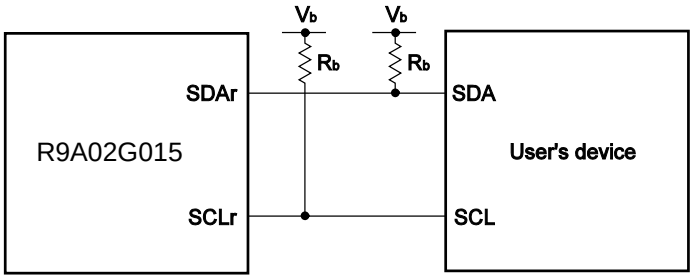
2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

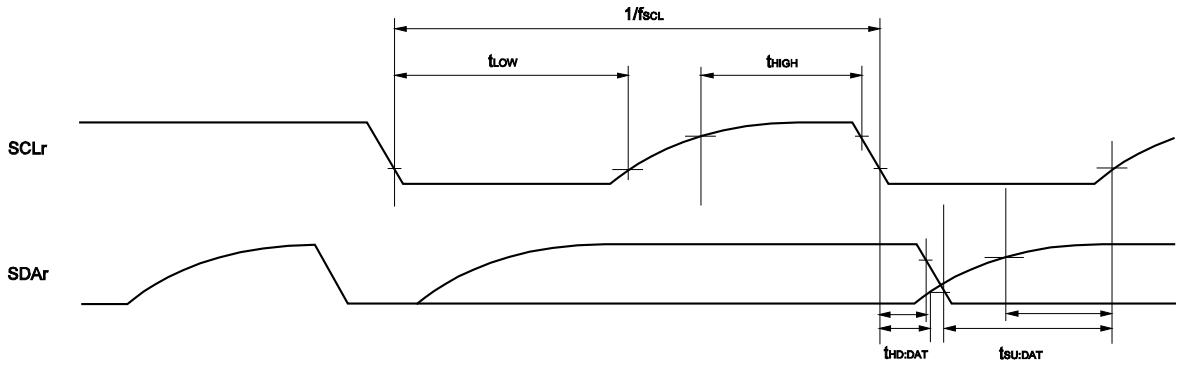
(**Remarks** are listed on the next page.)

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Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00), g: PIM, POM number (g = 5)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00)

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2.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	100	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		250		μs
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	3.45	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I^2C fast mode

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

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(3) I^2C fast mode plus

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	1000	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		μs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		50		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.45	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		μs

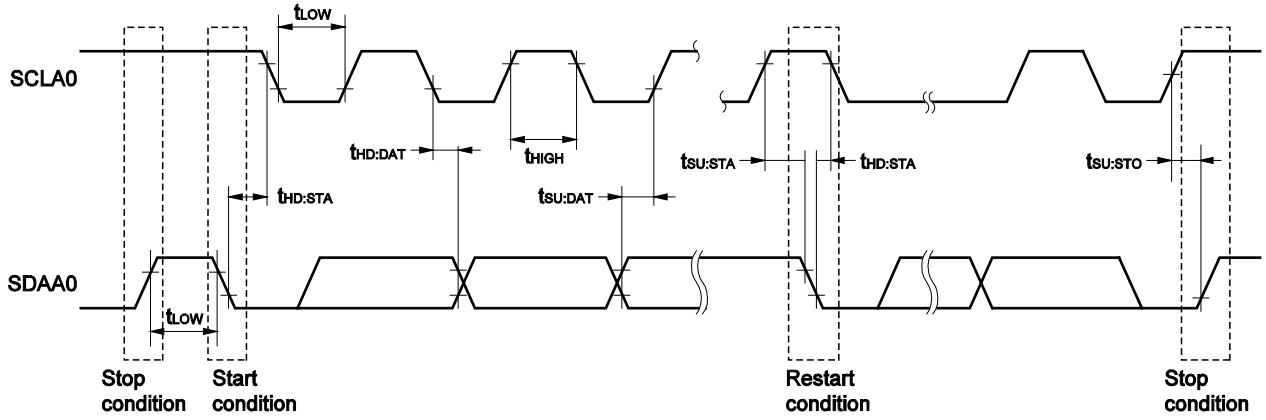
Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



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2.5.3 USB

(1) Electrical specifications

(T_A = –40 to +85°C, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UV_{DD}	UV_{DD} input voltage characteristic	UV_{DD}	V_{DD} = 3.0 to 5.5 V, PXXCON = 1, VDDUSEB = 0 (UV_{DD} ≤ V_{DD})	3.0	3.3	3.6	V
	UV_{DD} output voltage characteristic	UV_{DD}	V_{DD} = 4.0 to 5.5 V, PXXCON = VDDUSEB = 1	3.0	3.3	3.6	V
UV_{BUS}	UV_{BUS} input voltage characteristic	UV_{BUS}	Function	4.35 (4.02[Note])	5.00	5.5	V
			Host	4.75	5.00	5.5	V

Note Value of instantaneous voltage

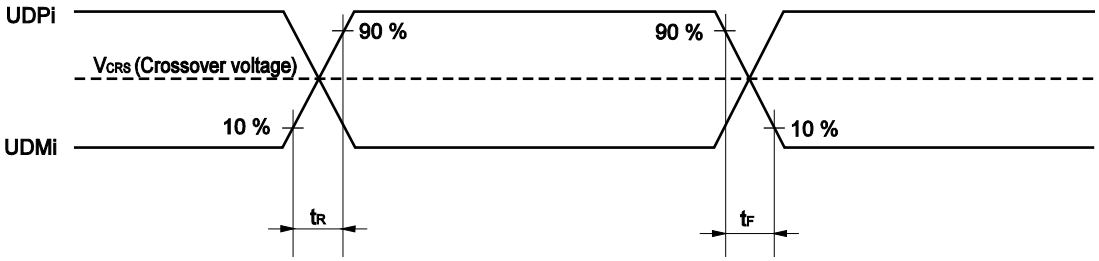
(T_A = –40 to +85°C, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi/UDMi pins input characteristic	Input voltage		V_{IH}		2.0			V
			V_{IL}				0.8	V
	Difference input sensitivity		V_{DI}	| UDP voltage – UDM voltage |	0.2			V
	Difference common mode range		V_{CM}		0.8		2.5	V
UDPi/UDMi pins output characteristic (FS driver)	Output voltage		V_{OH}	I_{OH} = –200 μA	2.8		3.6	V
			V_{OL}	I_{OL} = 2.4 mA	0		0.3	V
	Transi-tion time	Rising	t_{FR}	Rising: From 10% to 90 % of amplitude, Falling: From 90% to 10 % of amplitude, CL = 50 pF	4		20	ns
		Falling	t_{FF}		4		20	ns
	Matching (TFR/TFF)		T_{FRFM}		90		111.1	%
	Crossover voltage		V_{FCRS}		1.3		2.0	V
	Output Impedance		Z_{DRV}	UV_{DD} voltage = 3.3 V, Pin voltage = 1.65 V	28		44	Ω
UDPi/UDMi pins pull-up, pull-down	Pull-down resistor		R_{PD}		14.25		24.80	kΩ
	Pull-up resistor (i = 0 only)	Idle	R_{PUI}		0.9		1.575	kΩ
		Recep-tion	R_{PUA}		1.425		3.09	kΩ
UV_{BUS}	UV_{BUS} pull-down resistor		R_{VBUS}	UV_{BUS} voltage = 5.5 V		1000		kΩ
	UV_{BUS} input voltage		V_{IH}		3.20			V
			V_{IL}				0.8	V

Remark i = 0, 1

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Timing of UDPi and UDMi



(2) BC standard

(T_A = –40 to +85°C, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB standard BC1.2	UDPi sink current	I_{DP_SINK}		25		175	μA
	UDMi sink current	I_{DM_SINK}		25		175	μA
	Dedicated charging port resistor	R_{DCP_DAT}	0 V < UDP/UDM voltage < 1.0 V			200	Ω
	Data detection voltage	V_{DAT_REF}		0.25		0.4	V
	UDPi source voltage	V_{DP_SRC}	Output current 250 μA	0.5		0.7	V
	UDMi source voltage	V_{DM_SRC}	Output current 250 μA	0.5		0.7	V

Remark i = 0, 1

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(3) BC option standard (Host)

(T_A = –40 to +85°C, 4.75 V ≤ UV_{BUS} ≤ 5.5 V, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi output voltage (UV_{BUS} divider ratio) • VDOUEi = 1	VDSELi [3:0]	1000	V_{P20}		38	40	42	% UV_{BUS}
		1001	V_{P27}		51.6	53.6	55.6	% UV_{BUS}
		1010	V_{P20}		38	40	42	% UV_{BUS}
		1100	V_{P33}		60	66	72	% UV_{BUS}
UDMi output voltage (UV_{BUS} divider ratio) • VDOUEi = 1	VDSELi [3:0]	1000	V_{M20}		38	40	42	% UV_{BUS}
		1001	V_{M20}		38	40	42	% UV_{BUS}
		1010	V_{M27}		51.6	53.6	55.6	% UV_{BUS}
		1100	V_{M33}		60	66	72	% UV_{BUS}
UDPi comparing voltage **Note 1** (UV_{BUS} divider ratio) • VDOUEi = 1 • CUSDETEi = 1	VDSELi [3:0]	1000	V_{HDETP_UP0}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETP_DWN0}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
		1001	V_{HDETP_UP1}	The rise of pin voltage detection voltage	60.5			% UV_{BUS}
			V_{HDETP_DWN1}	The fall of pin voltage detection voltage			45.0	% UV_{BUS}
		1010	V_{HDETP_UP2}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETP_DWN2}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
UDMi comparing voltage **Note 1** (UV_{BUS} divider ratio) • VDOUEi = 1 • CUSDETEi = 1	VDSELi [3:0]	1000	V_{HDETM_UP0}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETM_DWN0}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
		1001	V_{HDETM_UP1}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETM_DWN1}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
		1010	V_{HDETM_UP2}	The rise of pin voltage detection voltage	60.5			% UV_{BUS}
			V_{HDETM_DWN2}	The fall of pin voltage detection voltage			45.0	% UV_{BUS}
UDPi pull-up detection **Note 2** Connect detection with the full speed function (pull-up resistor)		1000 1001 1010	R_{HDET_PULL}	In full-speed mode, the power supply voltage range of pull-up resistors connected to the USB function module is between 3.0 V and 3.6 V.			1.575	kΩ
UDMi pull-up detection **Note 2** Connect detection with the low-speed (pull-up resistor)		1000 1001 1010	R_{HDET_PULL}	In low-speed mode, the power supply voltage range of pull-up resistors connected to the USB function module is between 3.0 V and 3.6 V.			1.575	kΩ
UDMi sink current detection **Note 2** Connect detection with the BC1.2 portable device (sink resistor)		1000 1001 1010	I_{HDET_SINK}		25			μA

Notes 1. If the voltage output from UDPi or UDMi exceeds the range of the MAX and MIN values prescribed in this specification, DPCUSDETi (bit 8) and DMCUSDETi (bit 9) of the USBBCOPTi register are set to 1.

2. If the pull-up resistance or sink current prescribed in this specification is applied to UDPi or UDMi, DPCUSDETi (bit 8) and DMCUSDETi (bit 9) of the USBBCOPTi register are set to 1.

Remark i = 0, 1

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(4) BC option standard (Function)

(T_A = –40 to +85°C, 4.35 V ≤ UV_{BUS} ≤ 5.5 V, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi/UDMi input reference voltage (UV_{BUS} divider ratio) • VDOUEi = 0	VDSELi [3:0]	0000	V_{DDET0}		27	32	37	% UV_{BUS}
		0001	V_{DDET1}		29	34	39	% UV_{BUS}
		0010	V_{DDET2}		32	37	42	% UV_{BUS}
		0011	V_{DDET3}		35	40	45	% UV_{BUS}
		0100	V_{DDET4}		38	43	48	% UV_{BUS}
		0101	V_{DDET5}		41	46	51	% UV_{BUS}
		0110	V_{DDET6}		44	49	54	% UV_{BUS}
		0111	V_{DDET7}		47	52	57	% UV_{BUS}
		1000	V_{DDET8}		51	56	61	% UV_{BUS}
		1001	V_{DDET9}		55	60	65	% UV_{BUS}
		1010	V_{DDET10}		59	64	69	% UV_{BUS}
		1011	V_{DDET11}		63	68	73	% UV_{BUS}
		1100	V_{DDET12}		67	72	77	% UV_{BUS}
		1101	V_{DDET13}		71	76	81	% UV_{BUS}
		1110	V_{DDET14}		75	80	85	% UV_{BUS}
		1111	V_{DDET15}		79	84	89	% UV_{BUS}

Remark i = 0, 1

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2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (–) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (–) = AV_{REFM}
ANI0 to ANI5	Refer to **2.6.1 (1)**.	Refer to **2.6.1 (3)**.	Refer to **2.6.1 (4)**.
ANI16, ANI17	Refer to **2.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **2.6.1 (1)**.		–

(1) When $AV_{REF(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI2 to ANI5, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +85°C, 2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Note 2]	2.7 V ≤ V_{DD} ≤ 5.5 V		1.2	±3.5	LSB
Analog input voltage	V_{AIN}	ANI2 to ANI7		0		AV_{REFP}	V
		Internal reference voltage (2.7 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} [Note 3]			V
		Temperature sensor output voltage (2.7 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} [Note 3]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. When AV_{REFP} < V_{DD}, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

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(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI16, ANI17

(T_A = –40 to +85°C, 2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} Note 2	2.7 V ≤ V_{DD} ≤ 5.5 V		1.2	±5.0	LSB
Analog input voltage	V_{AIN}	ANI16, ANI17		0		AV_{REFP} and V_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. When AV_{REFP} < V_{DD}, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

(3) Reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), Reference voltage (–) = V_{SS} (ADREFM = 0), target ANI pin : ANI0 to ANI5, ANI16, ANI17, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error Note 1	AINL	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI5, ANI16, ANI17		0		V_{DD}	V
		Internal reference voltage (2.7 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} Note 2			V
		Temperature sensor output voltage (2.7 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} Note 2			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

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(4) When Reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), Reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0 to ANI5, ANI16, ANI17

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR} Note 1, Reference voltage (–) = AV_{REFM} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		8			Bit
Analog input voltage	V_{AIN}		0		V_{BGR} Note 1	V

Notes 1. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

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2.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

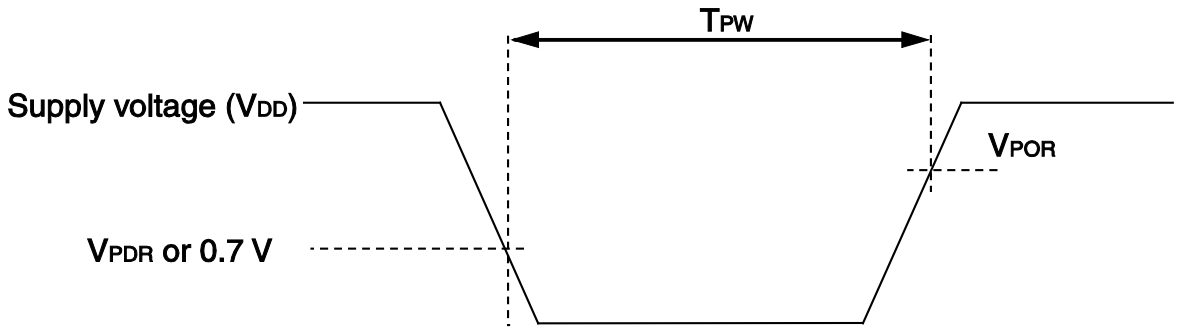
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

2.6.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock (f_{MAIN}) is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



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2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +85°C, $V_{PDR} \le V_{DD} \le 5.5$ V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time		t_{LD}				300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +85°C, $V_{PDR} \le V_{DD} \le 5.5$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDC0}	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage			2.40	2.45	2.50	V
	V_{LVDC1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
				Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage			2.70	2.75	2.81	V
	V_{LVDD1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDD3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	4.06	V

2.6.5 Power supply voltage rising slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

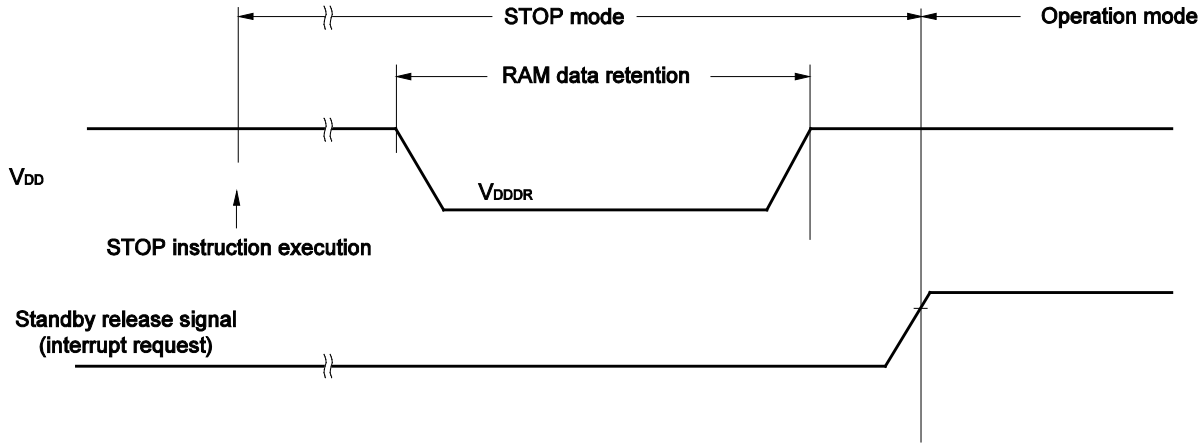
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2.7 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46[Note]		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	2.7 V ≤ V_{DD} ≤ 5.5 V	1		24	MHz
Number of code flash rewrites	C_{erwr}	Retaining years: 20 years T_A = +85°C	1,000			Times
Number of data flash rewrites **Notes 1, 2, 3**		Retaining years: 1 year T_A = +25°C		1,000,000		
		Retaining years: 5 years T_A = +85°C	100,000			
		Retaining years: 20 years T_A = +85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library.

3. These specifications show the characteristics of the flash memory and the results obtained from Renesas Electronics reliability testing.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

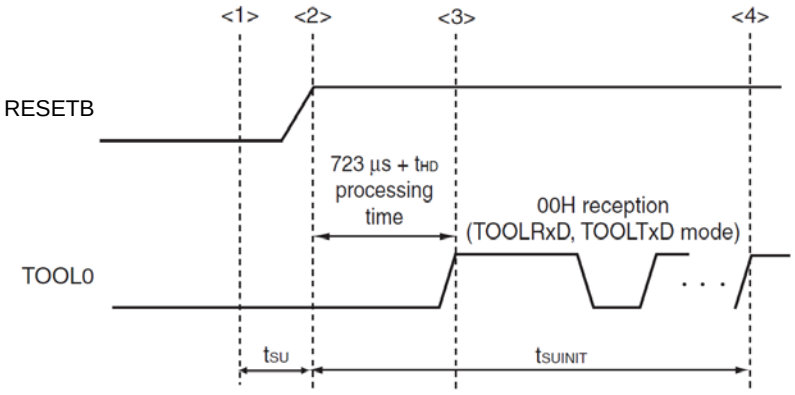
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

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2.10 Timing Specs for Switching Flash Memory Programming Modes

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends

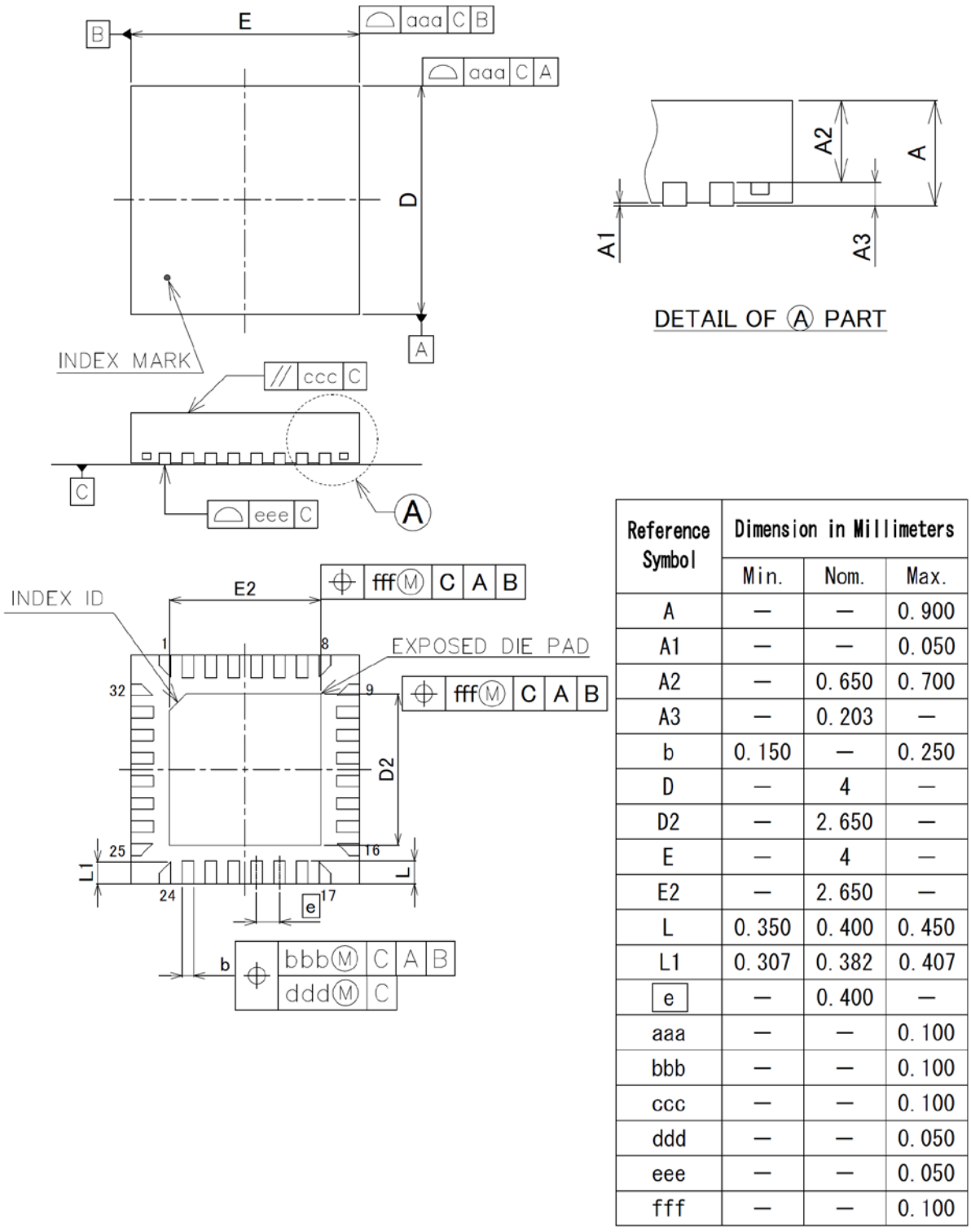
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (excluding the processing time of the firmware to control the flash memory)

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3. PACKAGE DRAWINGS

32-pin QFN (4 x 4 mm)

JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-HVQFN32-4×4-0.40	PVQN0032LD-A	0.04



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.900
A1	—	—	0.050
A2	—	0.650	0.700
A3	—	0.203	—
b	0.150	—	0.250
D	—	4	—
D2	—	2.650	—
E	—	4	—
E2	—	2.650	—
L	0.350	0.400	0.450
L1	0.307	0.382	0.407
e	—	0.400	—
aaa	—	—	0.100
bbb	—	—	0.100
ccc	—	—	0.100
ddd	—	—	0.050
eee	—	—	0.050
fff	—	—	0.100

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Revision History	R9A02G015 Data Sheet

Rev.	Date	Description	
		Page	Summary
0.10	Oct 31, 2018	—	First Draft of the Preliminary Data Sheet
0.20	Nov 9, 2018	15	Updated section 2.3.2
		44-45	Updated section 2.5.3
0.90	Feb 15, 2019	15	Updated section 2.3.2
		42-43	Updated section 2.5.3
		53	Updated section 3
1.00	Mar 29, 2019	—	First Edition issued.

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