REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change total supply voltage in 1.3. Change in table I; output voltage swings test limits, clock to center frequency ratio, with conditions sides A, B, C, and pin 17 high, also side D pin 17 high, test limits, Q accuracy test limits. Add clock to center frequency, side-to-side matching test. Change dc offset voltage test conditions and limits. Change power supply current test conditions and limits. Change subgroups for output voltage swing in table I and groups C and D end-point electricals in table II. Editorial changes throughout.	92-03-23	M. A. FRYE
B	For f_{CLK}/f_O, Q_{ACC}, f_O vs f_O tests under Table I, delete subgroups 7, 8A, 8B and substitute 1, 2, 3. For V_{OS1}, V_{OS2}, V_{OS3} tests under table I, delete subgroups 4, 5, 6 and substitute 1, 2, 3. Add subgroups 7, 8A, and 8B to paragraph 4.3.1. Delete subgroups 7, 8A, and 8B from Table II. Changes in accordance with N.O.R. 5962-R017-93.	92-12-15	M. A. FRYE
C	For the total supply voltage specified under paragraph 1.3, delete 16.5 V dc and substitute 16.0 V dc. Changes in accordance with N.O.R. 5962-R149-95.	95-06-02	M. A. FRYE
D	For the I_{CC} test under Table I, subgroup 1, delete 22 mA and substitute 23 mA. Changes in accordance with N.O.R. 5962-R105-96.	96-04-16	M. A. FRYE
E	Drawing updated to reflect current requirements. Redrawn. - ro	08-07-08	R. HEBER

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E				
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10				

PMIC N/A

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DRAWING APPROVAL DATE
90-10-30

REVISION LEVEL
E

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, LINEAR, CMOS, QUAD, UNIVERSAL FILTER BUILDING BLOCK, MONOLITHIC SILICON

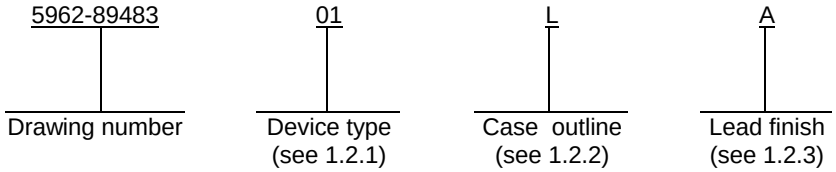
SIZE	CAGE CODE	
A	**67268**	**5962-89483**

SHEET 1 OF 10

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LTC1064	CMOS, quad, universal filter building block

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Total supply voltage ($+V_S$ to $-V_S$) ..... 16.0 V dc
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Power dissipation (P_D) ..... 500 mW
Junction temperature (T_J) ..... +175°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 60°C/W

1.4 Recommended operating conditions.

Supply voltage ($\pm V_S$) ..... ±5 V dc
Operating supply voltage range ..... ±2.37 V dc to ±8.0 V dc
Ambient operating temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Equivalent input offsets. The equivalent input offsets shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_S = \pm 5.0$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Internal operational amplifiers							
Output voltage swings	V_{OUT}	$R_L = 5.0$ kΩ	4	01	-3.2	+3.2	V
			5,6		-3.1	+3.1	
Complete filter (TTL clock input level, unless otherwise specified)							
Clock to center frequency ratio	f_{CLK} / f_O	Sides A, B, and C = mode 1, R1 = R3 = 50 kΩ, R2 = 5.0 kΩ, f_{CLK} = 1.0 MHz, Q = 10, f_O = 20 kHz, pin 17 high, (condition A)	1,2,3,	01	49.6	50.4	
		Side D = mode 3, R1 = R3 = 50 kΩ, R2 = R4 = 5.0 kΩ, f_{CLK} = 1.0 MHz, Q = 10, f_O = 20 kHz, pin 17 high, (condition B)			49.55	50.45	
		Sides A, B, and C = mode 1, R1 = R3 = 50 kΩ, R2 = 5.0 kΩ, f_{CLK} = 1.0 MHz, Q = 10, f_O = 10 kHz, pin 17 low, (condition C)			99.2	100.8	
		Side D = mode 3, R1 = R3 = 50 kΩ, R2 = R4 = 5.0 kΩ, f_{CLK} = 1.0 MHz, Q = 10, f_O = 10 kHz, pin 17 low, (condition D)			99.1	100.9	

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_S = \pm 5.0$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Complete filter (TTL clock input level, unless otherwise specified) - Continued.							
Q accuracy	Q_{ACC}	Sides A, B, and C = mode 1, f_{CLK} = 1.0 MHz, Q = 10	1,2,3	01	-6.0	6.0	%
		Side D = mode 3, f_{CLK} = 1.0 MHz, Q = 10			-8.0	8.0	
Clock to center frequency ratio; side-to-side matching	f_O vs f_O	f_{CLK} / f_O conditions A through D.	1,2,3	01	-1.0	1.0	%
DC offset voltage	V_{OS1}	f_{CLK}/f_O = 50:1, f_{CLK} = 1.0 MHz, see figure 3	1,2,3	01	-15	15	mV
	V_{OS2}	f_{CLK}/f_O = 50:1 and 100:1, f_{CLK} = 1.0 MHz, see figure 3			-45	45	
	V_{OS3}				-45	45	
Power supply current	I_{CC}	$V_S = \pm 5.0$ V	1	01		23	mA
			2,3			26	

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

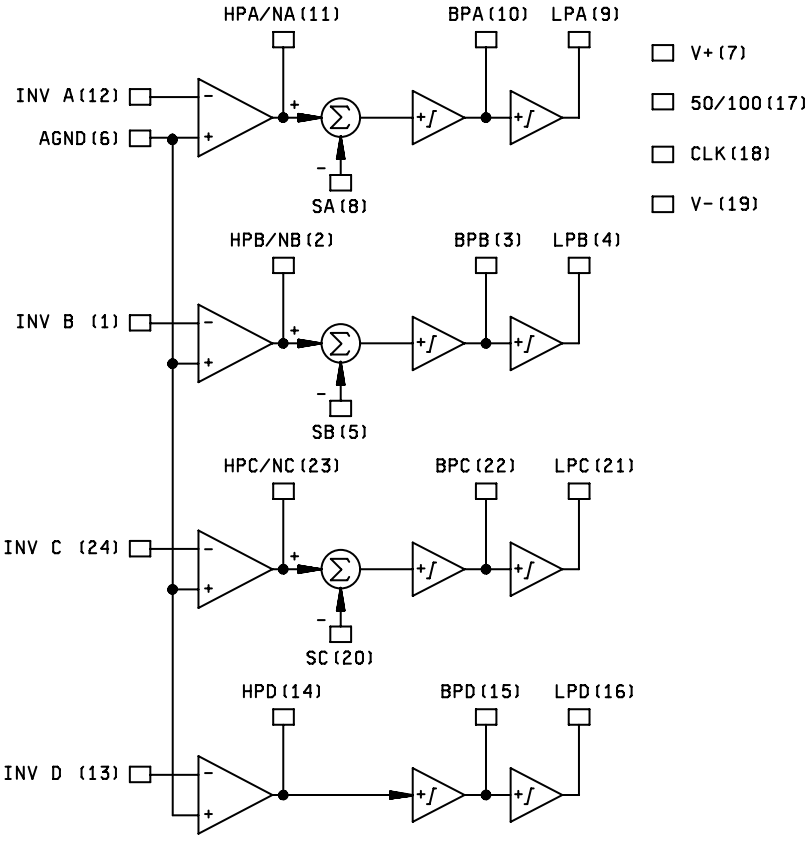
3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Device type	01
Case outline	L
Terminal number	Terminal symbol
1	INV B
2	HPB / NB
3	BPB
4	LPB
5	SB
6	AGND
7	$+V_S$
8	SA
9	LPA
10	BPA
11	HPA / NA
12	INV A
13	INV D
14	HPD
15	BPD
16	LPD
17	50 / 100
18	CLK
19	$-V_S$
20	SC
21	LPC
22	BPC
23	HPC / NC
24	INV C

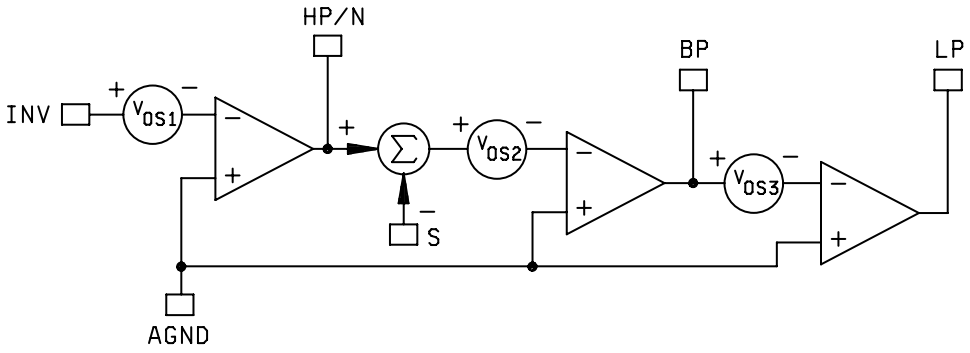
FIGURE 1. Terminal connections.



Operational notes.

1. By tying pin 17 to V+, all sections operate with (f_{CLK} / f_O) = (50:1).
2. By tying pin 17 to V-, all sections operate with (f_{CLK} / f_O) = (100:1).
3. By tying pin 17 to AGND, sections B and C operate with (f_{CLK} / f_O) = (50:1) and sections A and D operate at (100:1).

FIGURE 2. Block diagram.



NOTE: This represents one quarter of the filter building block.

FIGURE 3. Equivalent input offsets.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8A, 8B, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,4,5,6
Group A test requirements (method 5005)	1,2,3,4,5,6
Groups C and D end-point electrical parameters (method 5005)	1,4

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-07-08

Approved sources of supply for SMD 5962-89483 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8948301LA	3/	LTC1064MJ/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply. The last known supplier is listed below.

Vendor CAGE number	Vendor name and address
64155	Linear Technology Corporation 1630 McCarthy Blvd. Milpitas, CA 95035-7417

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.