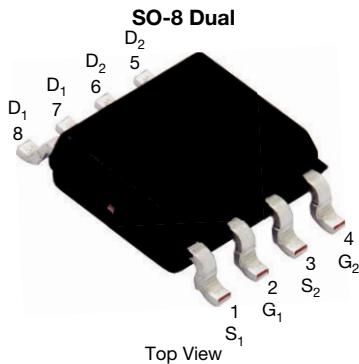


Dual N-Channel 20 V (D-S) MOSFET



FEATURES

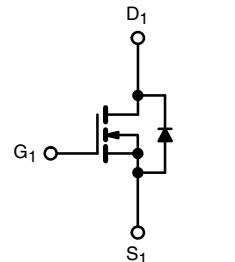
- TrenchFET® power MOSFET
- 100 % UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



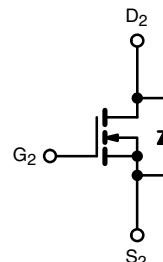
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- DC/DC converter
 - Game machine
 - PC



N-Channel MOSFET



N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.018
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5$ V	0.022
Q_g typ. (nC)	10
I_D (A) ^a	8
Configuration	Dual

ORDERING INFORMATION

Package	SO-8
Lead (Pb)-free	Si9926CDY-T1-E3
Lead (Pb)-free and halogen-free	Si9926CDY-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GS}	± 12	
Continuous drain current ($T_J = 150$ °C)	I_D	8 ^a	A
		8 ^a	
		8 a, b, c	
		6.7 b, c	
Pulsed drain current	I_{DM}	30	A
Continuous source-drain diode current	I_S	2.6	
		1.7 b, c	
Single pulse avalanche current	I_{AS}	5	mJ
Single pulse avalanche energy	E_{AS}	1.25	
Maximum power dissipation	P_D	3.1	W
		2	
		2 b, c	
		1.3 b, c	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient a, c, d	R_{thJA}	50	62.5	°C/W
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	40	

Notes

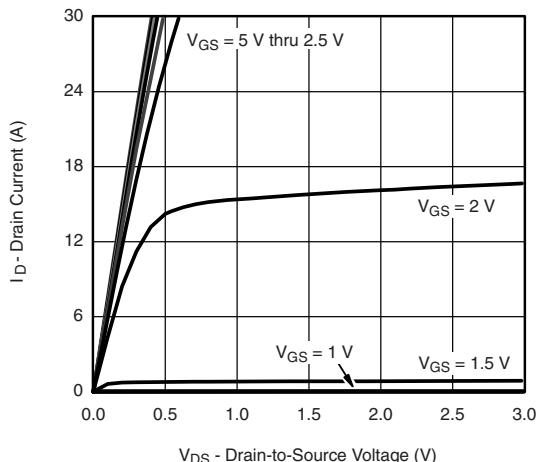
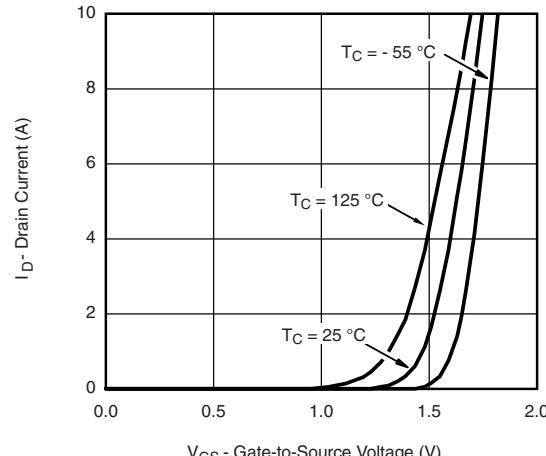
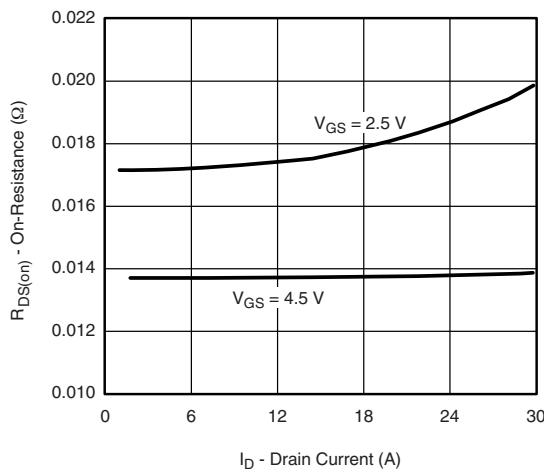
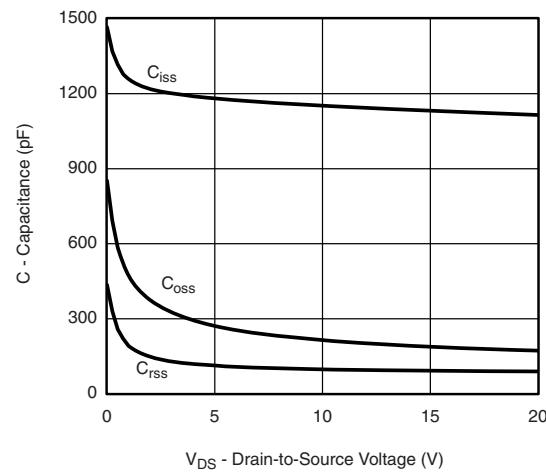
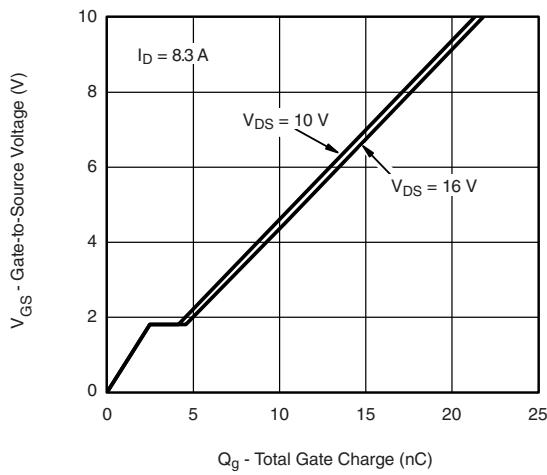
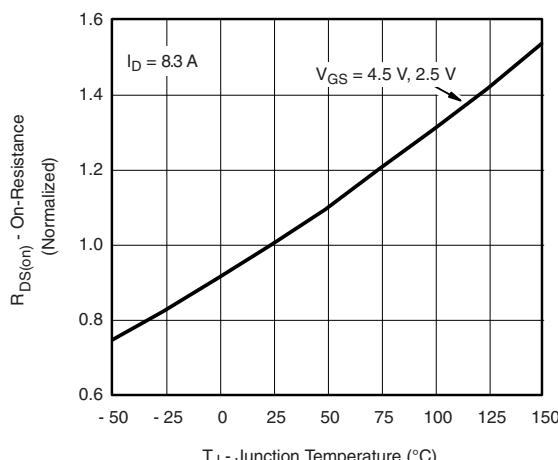
- Package limited, $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- Maximum under steady state conditions is 110 °C/W

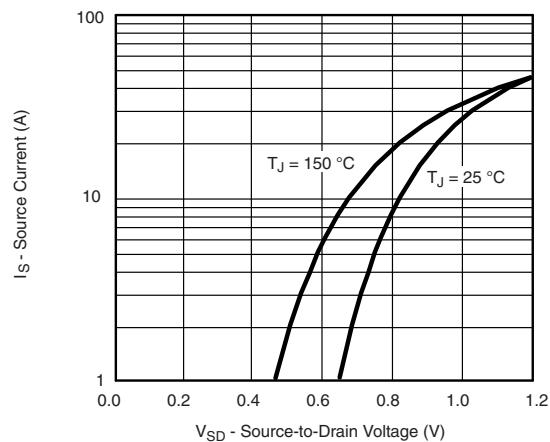
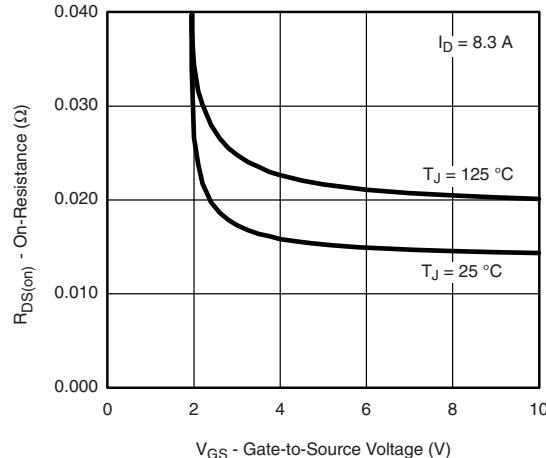
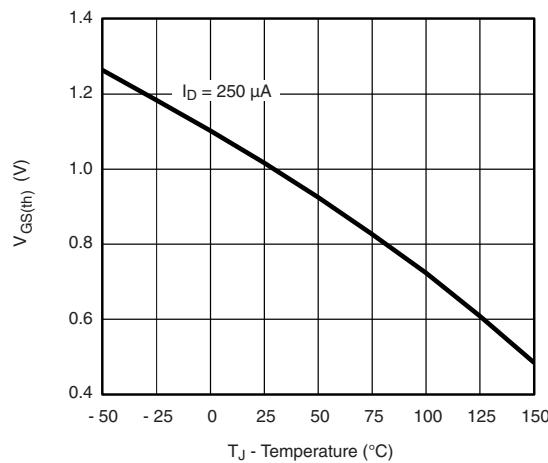
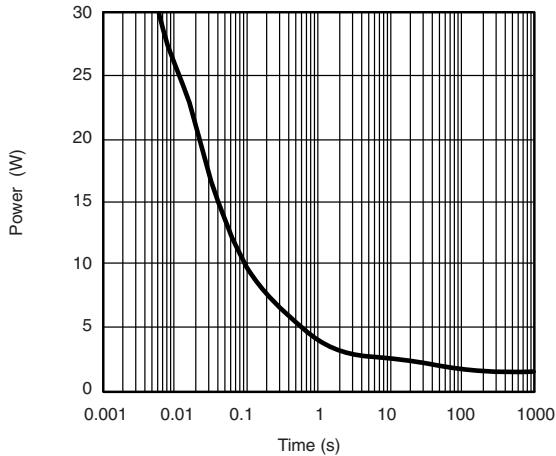
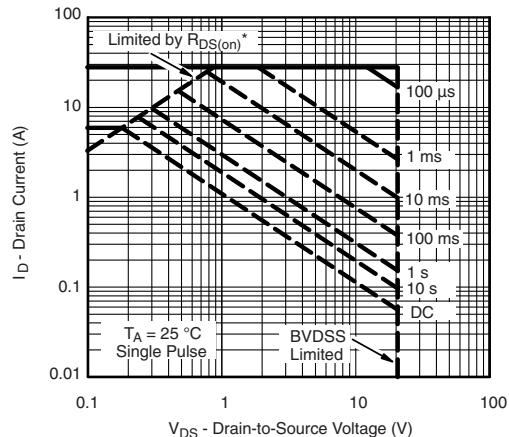
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	20	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	25	-	mV/°C
$V_{GS(\text{th})}$ temperature coefficient	$\Delta V_{GS(\text{th})}/T_J$		-	-4	-	
Gate-source threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	0.6	-	1.5	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 12\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55^\circ\text{C}$	-	-	10	
On-state drain current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 4.5\text{ V}$	30	-	-	A
Drain-source on-state resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 4.5\text{ V}$, $I_D = 8.3\text{ A}$	-	0.015	0.018	Ω
		$V_{GS} = 2.5\text{ V}$, $I_D = 4.5\text{ A}$	-	0.017	0.022	
Forward transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 8.3\text{ A}$	-	45	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	-	1200	-	pF
Output capacitance	C_{oss}		-	220	-	
Reverse transfer capacitance	C_{rss}		-	100	-	
Total gate charge	Q_g	$V_{DS} = 10\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 8.3\text{ A}$	-	22	33	nC
		$V_{DS} = 10\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 8.3\text{ A}$	-	10	15	
Gate-source charge	Q_{gs}		-	2.5	-	
Gate-drain charge	Q_{gd}		-	1.7	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	-	2.4	-	Ω
Turn-on delay time	$t_{d(\text{on})}$	$V_{DD} = 10\text{ V}$, $R_L = 1.5\text{ }\Omega$ $I_D \geq 6.7\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	-	15	25	ns
Rise time	t_r		-	10	15	
Turn-off delay time	$t_{d(\text{off})}$		-	35	55	
Fall time	t_f		-	12	20	
Turn-on delay time	$t_{d(\text{on})}$		-	10	15	
Rise time	t_r		-	12	20	
Turn-off delay time	$t_{d(\text{off})}$		-	25	40	
Fall time	t_f		-	10	15	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25^\circ\text{C}$	-	-	2.6	A
Pulse diode forward current	I_{SM}		-	-	30	
Body diode voltage	V_{SD}	$I_S = 6.7\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.8	1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = 6.7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$	-	20	40	ns
Body diode reverse recovery charge	Q_{rr}		-	10	20	
Reverse recovery fall time	t_a		-	10	-	
Reverse recovery rise time	t_b		-	10	-	

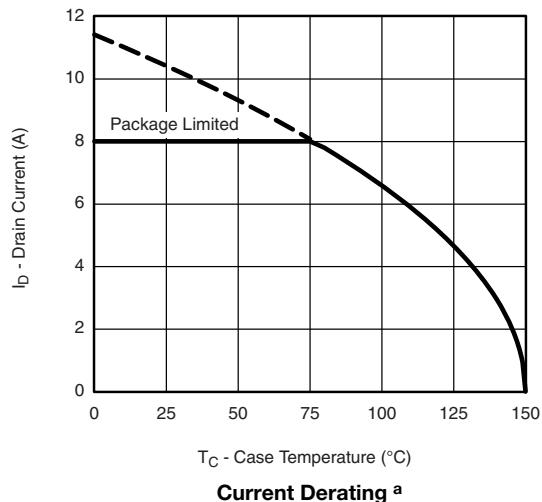
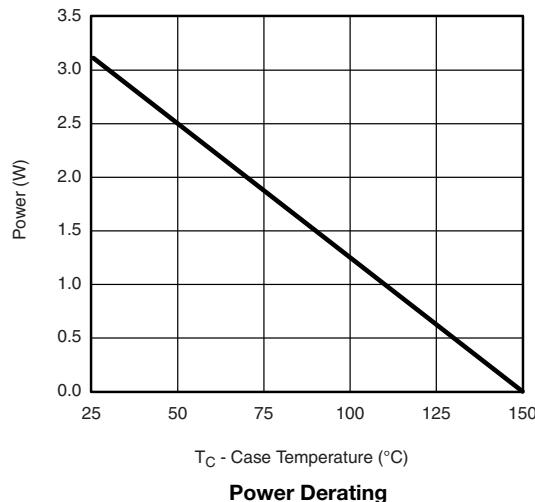
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\text{ \%}$
- b. Guaranteed by design, not subject to production testing

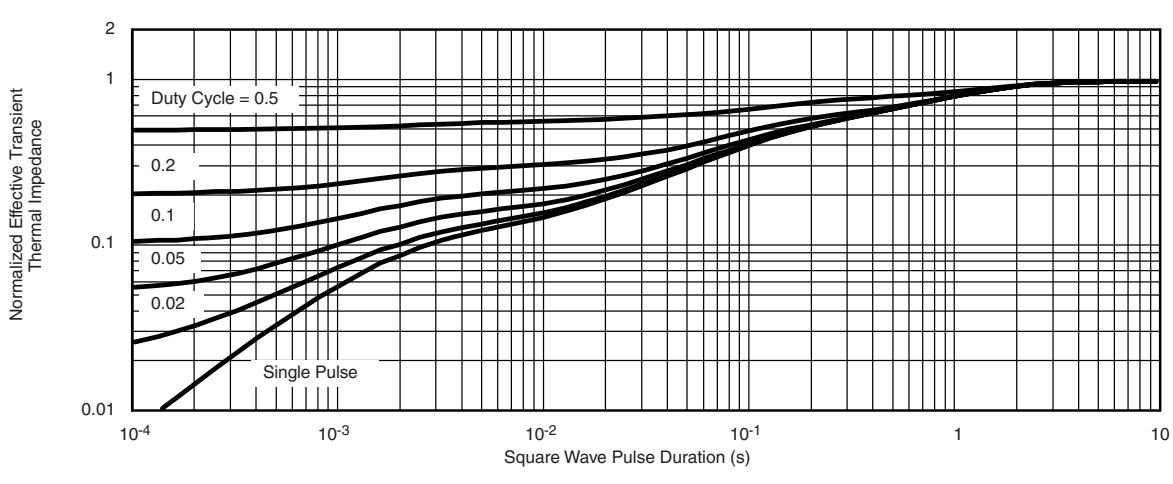
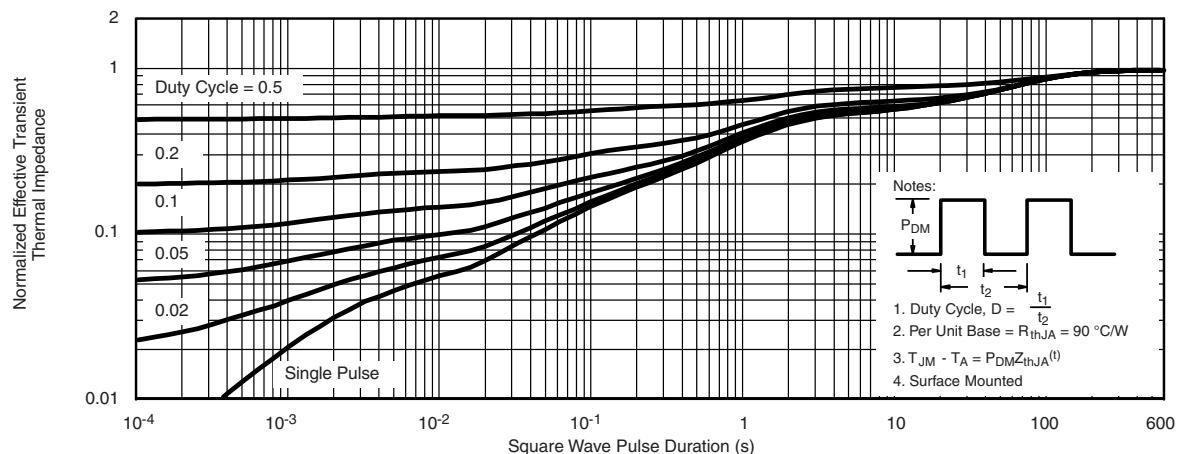
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power Derating
Notes

- The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68606.

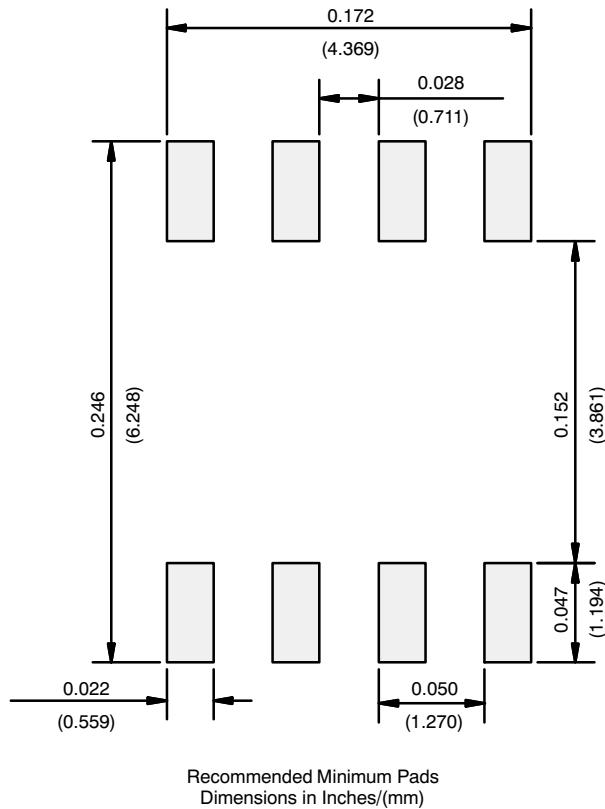
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



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