DATA SHEET

Si858x: Integrated Isolated RS-485 Transceivers

Industrial Applications

- Industrial automation systems
- Isolated switch mode supplies
- Inverters
- Data acquisition
- Motor control
- PLCs, distributed control systems

Safety Regulatory Approvals (Pending)

- UL 1577 recognized
  - Up to 5000 V_{RMS} for 1 minute
- CSA certification conformity
  - 62368-1 (Reinforced Insulation)
- VDE certification conformity
  - 60747-17 (Reinforced Insulation)
- CQC certification approval
  - GB4943.1

Key Features

- Compliance to TIA/EIA-485-A (RS-485), compatible with EN 50170 (ProfiBus)
- Industry standard footprint and logic operation
- Signaling rates of up to 10 Mbps
- HBM 15 kV bus pin ESD ratings
- Common mode voltage supported for operation: –7 V to +12 V
- Bus fault protection: ±30 V
- Thermal shutdown protection
- VDD1: 3.0 V to 5.5 V
- VDD2: 3.3 V or 5.0 V options
- 17 ns typical driver propagation delay
- 5 kV_{RMS} isolation UL 1577
- CMTI of 100 kV/µs (min)
- Unit loading: Up to 256 transceivers supported
- T_A: –40 to +125 °C
- JEDEC-qualified
- WB SOIC-16 RoHS-compliant package

Description

The Si858x products are devices that combine robust, fully compliant RS-485 transceivers with signal isolation. These devices are ideal for industrial automation applications that require isolated interfaces for FieldBus systems that form a communication network for connecting sensors, actuators, and controllers.

These devices are ideal for isolating nodes on FieldBuses based on the RS-485 standard, such as ProfiBus or ModBus. These transmission lines can be susceptible to electrical noise transients especially in harsh environments such as a factory floor, or in sensitive environments such as process control or data acquisition. Isolation provides a means of protection from such transients and noise that could corrupt signal integrity.

These isolated transceivers can operate with a 3.3 V or 5.0 V nominal power supply and have robust bus fault tolerance up-to ±30 V for protecting against harmful transients in noisy environment where such systems are often utilized. The bus pins are also protected up to 15 kV HBM ESD. Product options are available for half duplex and full duplex mode in industry standard footprints and incorporate slew rate controlled drivers with 1 Mbps data rate capability for reducing the EMI profile or options for high data rate up to 10 Mbps with no slew rate control implemented. These products also offer safety and protection features, such as receiver fail-safe and thermal protection.

These devices utilize Skyworks' proprietary silicon isolation technology, supporting up to 5 kV_{RMS} (for one minute) isolation voltage per UL1577. This technology enables high CMTI (>100 kV/µs), low propagation delays and skew, reduced variation with temperature, and age and tight part-to-part matching.

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

1. Pin Descriptions

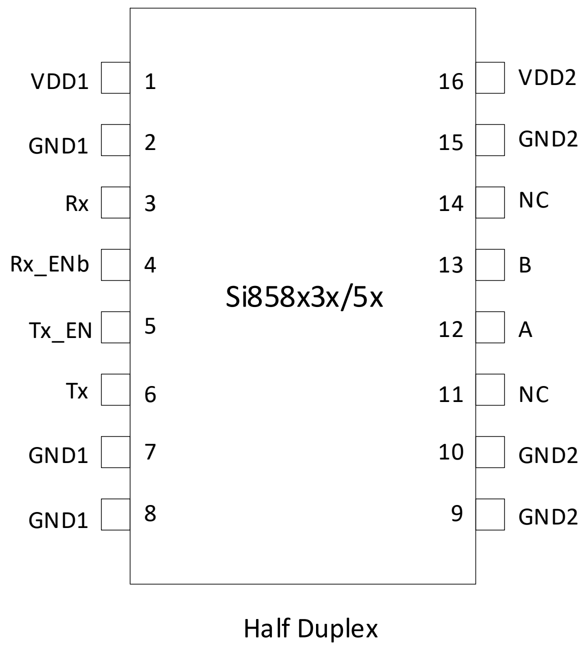

Figure 1. Pinout Diagram for Half Duplex Transceivers

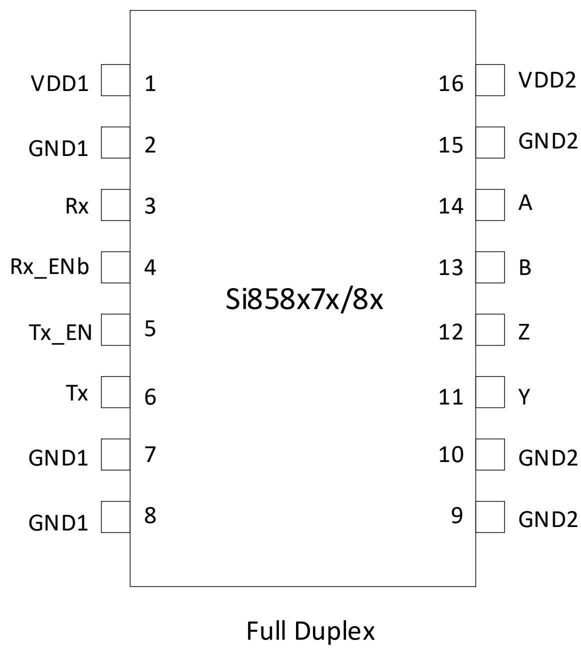

Figure 2. Pinout Diagram for Full Duplex Transceivers

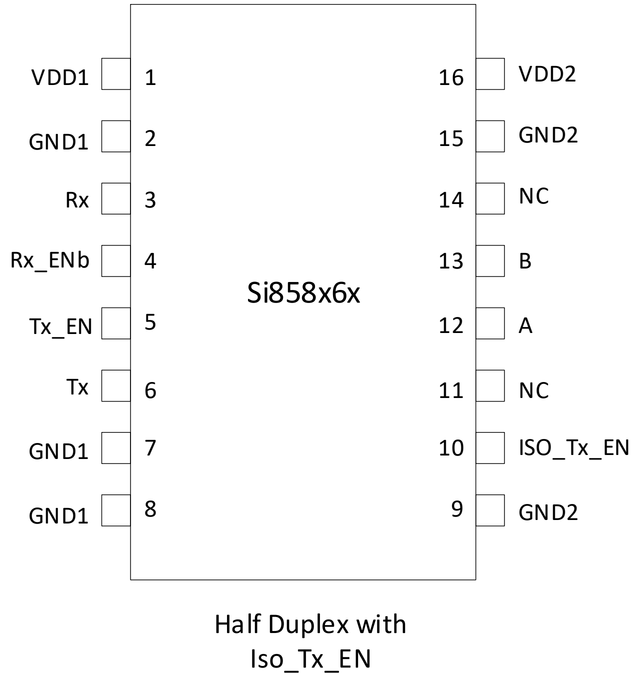

Figure 3. Pinout Diagram for Half Duplex with Isolated Tx_EN

Table 1. Pin Descriptions

Pin Name	Description
Logic Side	
VDD1	Logic side supply voltage.
NC	Not connected.
Tx	Driver input.
Tx_EN	Driver enable. When driven high, driver is enabled.
Rx_ENb	Rx enable (active low) with internal pull-down resistor. When open or driven low, the receiver is enabled.
Rx	Receiver output.
GND1	Logic side supply ground.
Transceiver (Bus) Side	
GND2	Bus side supply ground.
Y, Z	Driver output bus pins for full duplex (Si858x7, Si858x8).
A, B	Receiver input bus pins for full duplex (Si858x7, Si858x8) or driver/receiver bus pins for half duplex (Si858x3, Si858x5, Si858x6).
ISO_Tx_EN	Isolated Tx_EN feedthrough.
VDD2	Bus side supply voltage.

2. Functional Description

2.1. Theory of Operation

The Si858x family of products is capable of transmitting and receiving RS-485 signals from one power domain to an isolated domain with up to 5.0 kV_{RMS} of isolation.

2.2. Digital Isolation

The operation of an Si858x digital channel is analogous to that of a digital buffer, except an RF carrier transmits data across the isolation barrier. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at startup. Figure 4 shows a simplified block diagram for a single Si858x channel.

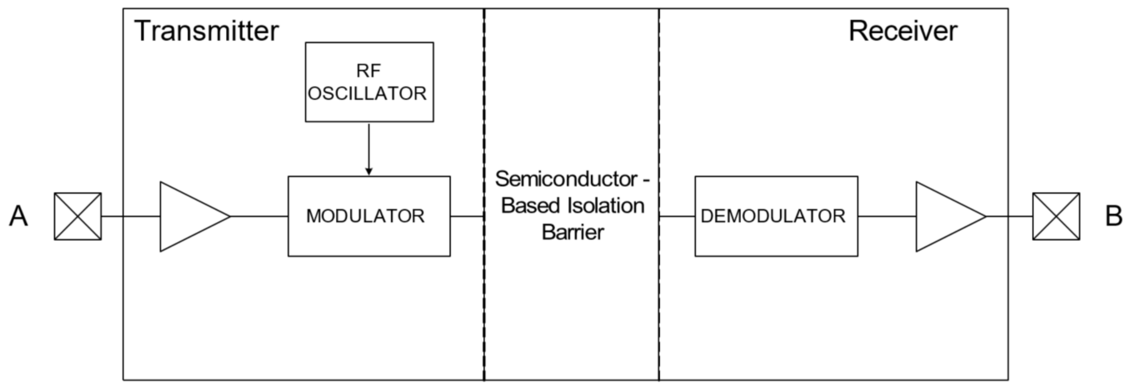

Figure 4. Simplified Si858x Channel Diagram

A channel consists of an RF transmitter and RF receiver separated by a silicon dioxide capacitive isolation barrier. In the transmitter, Input A modulates the carrier provided by an RF oscillator using On/Off keying. The receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to Output B via the output driver. This RF On/Off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 5 for more details.

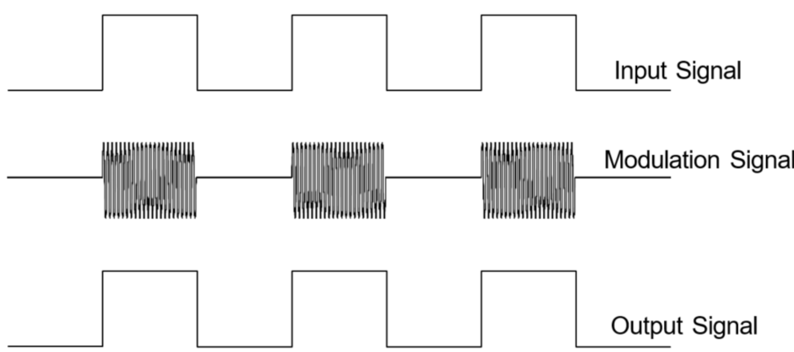

Figure 5. Modulation Scheme

2.3. RS-485 Signaling

These isolated transceivers are compliant to the TIA/EIA-485 standard. They are available in full-duplex as well as half-duplex configurations.

For the driver operation, when VDD1 and VDD2 are both powered up and the driver is enabled (Tx_EN pin is high), a logic high on driver input pin Tx produces a corresponding logic high on the isolated driver output bus Pin Y (Pin A for half duplex) and a logic low on Pin Z (Pin B for half duplex). A logic low on the Tx pin will invert the outputs. Thus, the differential output voltage on the bus, defined as $V_{OD} = VY/A – VB/Z$, is positive when Tx is high and negative when Tx is low. The Tx_EN pin is active high; driving it low will disable the driver function, and the bus pins will be high impedance.

The receiver enable is active low with an internal pull-down resistor. Leaving it open or driving it low enables the receiver while driving it high will disable it. With the receiver enabled, a differential input (defined as $V_{ID} = V_A – V_B$) greater than the input threshold (Referred to as V_{IT+} in Table 8, “Electrical Characteristics for 5.0 V Rated Part Numbers,” on page 11 and Table 9, “Electrical Characteristics for 3.3 V Rated Part Numbers,” on page 13) of the receiver produces a logic high on the receiver output pin Rx. A differential input that is lower than the receiver threshold (Referred to as $V_{IT–}$ in Table 8, “Electrical Characteristics for 5.0 V Rated Part Numbers,” on page 11 and Table 9, “Electrical Characteristics for 3.3 V Rated Part Numbers,” on page 13) will produce a logic low.

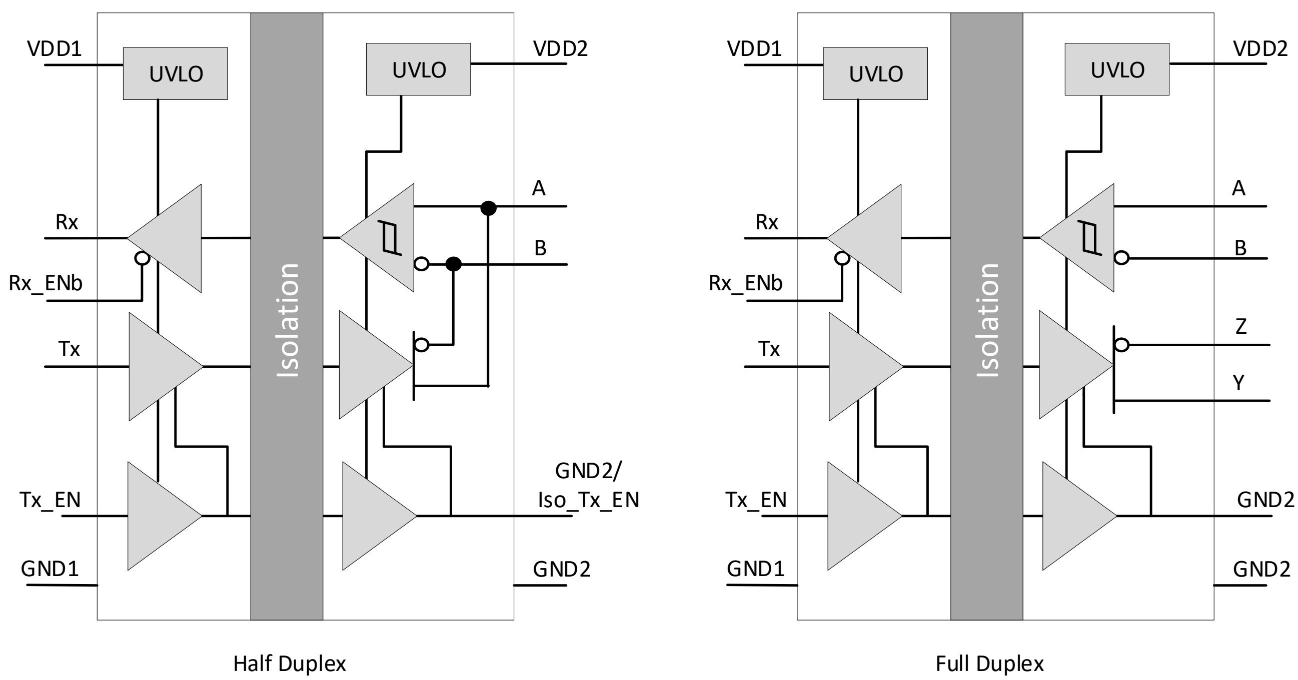

Figure 6. Isolated Transceiver Block Diagram

3. Device Operation

Table 2. Si858x Driver Operation

Input Tx[1]	Enable Tx_EN[1]	VDD1[2,3]	VDD2[2,3]	Output ISO_Tx_EN[1]	Output Y or A[1]	Output Z or B[1]
H	H	P	P	H	H	L
L	H	P	P	H	L	H
X	L or OPEN	P	P	L	Hi-Z	Hi-Z
OPEN	H	P	P	H	L	H
X[4]	X	UP[5]	P	L	Hi-Z	Hi-Z
X	X	P	UP[6]	UD	UD	UD
X	X	UP	UP	UD	UD	UD

1. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance, UD = undetermined.
2. VDD1 and VDD2 are the logic and transceiver side power supplies.
3. "Powered" state (P) is defined as > 2.5 V, "Unpowered" state (UP) is defined as VDD = 0 V.
4. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
5. For reliability reasons, it is highly recommended that the power supply (VDD1 or VDD2) not be powered down while TX_EN is asserted high or while it is in the transition to disable state.
6. When VDD2 is UP, ISO_Tx_EN pin may still follow the TX_EN state. It is recommended that while VDD2 is in the UP state, the status of ISO_TX_EN be ignored.

Table 3. Si858x Receiver Operation

Differential Input VID = VIA – VIB[1]	Enable Rx_ENb[2]	VDD1[3,4]	VDD2[3,4]	Output Rx[2]
VID ≥ –10 mV	L or OPEN	P	P	H
–200 mV < VID < –10 mV	L or OPEN	P	P	UD
VID ≤ –200 mV	L or OPEN	P	P	L
X	H	P	P	Hi-Z
OPEN	L	P	P	H
SHORT	L	P	P	H
IDLE (terminated)	L	P	P	H
X	X[5]	UP	P	UD
X	L or open	P	UP	H
X	H	P	UP	Hi-Z

1. Open = transceiver disconnected from bus, Short = bus shorted, Idle = bus not actively driven.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance, UD = undetermined.
3. VDD1 and VDD2 are the logic and transceiver side power supplies.
4. "Powered" state (P) is defined as > 2.5 V, "Unpowered" state (UP) is defined as VDD = 0 V.
5. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.

3.1. Layout Considerations

To ensure safety in the end-user application, high-voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low-voltage circuits (SELV is a circuit with <30 VAC) by a certain distance (creepage/clearance). If a component, such as an isolated transceiver, straddles this isolation barrier, it must meet those creepage/clearance requirements and provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). These requirements also detail the component standards (UL1577, IEC 60747-17), which are readily accepted by certification bodies to provide proof for end-system specification requirements. Refer to the end-system specification (61010-1, 62368-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.2. Supply Bypass

The Si858x family requires 0.1 µF and 10 µF bypass capacitor between VDD1 and GND1 and VDD2 and GND2. The capacitors should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50 to 300 Ω) in series with the logic inputs and outputs (excluding the bus pins) if the system is excessively noisy.

4. Electrical Specifications

Table 4. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage temperature	T_{STG}	–65	+150	°C
Junction temperature	T_J	—	+150	°C
Input supply voltage	VDD1, VDD2	–0.6	6.0	V
Supply voltage ramp-up	VDD1, VDD2	—	1.0	V/µs
Voltage on any digital pin with respect to ground, Tx, TX_EN, Rx, RX_ENb, ISO_Tx_En	V_{IN}	–0.5	VDD + 0.5	V
Bus fault protection, voltage on bus pin with respect to GND2	V_{OC}	–30	30	V
Receiver output current	I_O		10	mA
Lead solder temperature (10 s)		—	260	°C
ESD per JEDEC	HBM, bus pins only	—	15	kV
	CDM, bus pins only	—	2	kV
	HBM, all other pins	—	2.5	kV
	CDM, all other pins	—	1.5	kV

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 5. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient operating temperature[1]	T_A	–40	25	125	°C
Logic supply voltage	VDD1	2.5	—	5.5	V
Si8583x Transceiver supply voltage	VDD2	3.135	3.3	3.465	V
Si8585x Transceiver supply voltage		4.75	5.0	5.25	V
Voltage on bus pins A, B, Y, Z	V_{OC}	–7	—	12	V
High level input voltage on Tx, TX_EN, Rx_ENb	V_{IH}	0.7 x VDD1	—	—	V
Low level input voltage	V_{IL}	—	—	0.3 x VDD1	V
Differential input voltage	V_{ID}	–5	—	10	V
Differential load resistance	R_D	54	—	—	Ω
Driver output current	I_{OD}	–60	—	60	mA
Receiver output current	I_{OR}	–4	—	4	mA

1. The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 6. Supply Current for 5.0 V Rated Part Numbers

Parameter	Symbol	Test Condition	Min	Typ[1]	Max	Unit
Supply current (receiver enabled, driver disabled)	IDD1	Rx_ENb = 0, Tx_EN = 0, Bus open	—	2.3	2.6	mA
		Rx_ENb = 0 , Tx_EN = 0, Bus @ 1 Mbps	—	1.9	2.2	mA
		Rx_ENb = 0 , Tx_EN = 0, Bus @ 10 Mbps	—	4.7	6.0	mA
	IDD2	Rx_ENb = 0, Tx_EN = 0, Bus open	—	10.9	14.5	mA
		Rx_ENb = 0, Tx_EN = 0, Bus = 1 to 10 Mbps	—	11.5	17.1	mA
Supply current (receiver disabled, driver enabled, over specified bus common mode voltage range)	IDD1	Rx_ENb = 1, Tx_EN = 1, Tx = 0	—	2.9	3.5	mA
		Rx_ENb = 1, Tx_EN = 1, Tx = 1	—	3.5	4.0	mA
		Rx_ENb = 1, Tx_EN = 1, Tx = 1 to 10 Mbps	—	3.2	3.8	mA
	IDD2	Rx_ENb = 1, Tx_EN = 1, Tx = 0, 1	—	53.4	89.5	mA
		Rx_ENb = 1, Tx_EN = 1, Tx = 1 Mbps	—	53.7	90.5	mA
		Rx_ENb = 1, Tx_EN = 1, Tx = 1 Mbps (Si85853, Si85857 only)	—	63.7	99	mA
		Rx_ENb = 1, Tx_EN = 1, Tx = 10 Mbps	—	64	103	mA
Supply current (receiver and driver enabled, over specified bus common mode voltage range)	IDD1	Rx_ENb = 0, Tx_EN = 1, Bus open, Tx = 0	—	2.3	2.8	mA
		Rx_ENb = 0, Tx_EN = 1, Bus open, Tx = 1	—	2.9	3.7	mA
		Rx_ENb = 0, Tx_EN = 1, Tx = 1 Mbps (loop-back mode)	—	2.9	3.7	mA
		Rx_ENb = 0, Tx_EN = 1, Tx = 10 Mbps (loopback mode)	—	5.7	7.5	mA
	IDD2	Rx_ENb = 0, Tx_EN = 1 (loopback mode), Tx = 0, 1	—	40.8	50	mA
		Rx_ENb = 0, Tx_EN = 1, Tx = 1 Mbps (loopback mode)	—	54.4	91	mA
		Rx_ENb = 0, Tx_EN = 1, Tx = 1 Mbps (loopback mode; Si85853, Si85857 only)	—	64.4	100	mA
		Rx_ENb = 0, Tx_EN = 1, Tx = 10 Mbps	—	64.8	103	mA
Supply current (receiver and driver disabled)	IDD1	Rx_ENb = 1, Tx_EN = 0, Bus open	—	2.2	2.6	mA
		Rx_ENb = 1, Tx_EN = 0, Bus @ 1 to 10 Mbps	—	2	3.1	mA
	IDD2	Rx_ENb = 1, Tx_EN = 0, Bus open, or 1 to 10 Mbps	—	11.8	16	mA

1. Typical specifications at 25 °C.

Table 7. Supply Current for 3.3 V Rated Part Numbers

Parameter	Symbol	Test Condition	Min	Typ[1]	Max	Unit
Supply current (receiver enabled, driver disabled)	IDD1	Rx_ENb = 0, Tx_EN = 0, Bus open	—	2.3	2.6	mA
		Rx_ENb = 0 , Tx_EN = 0, Bus @ 1 Mbps	—	1.9	2.2	mA
		Rx_ENb = 0 , Tx_EN = 0, Bus @ 10 Mbps	—	4.7	6.0	mA
	IDD2	Rx_ENb = 0, Tx_EN = 0, Bus open	—	10.2	14.5	mA
		Rx_ENb = 0 , Tx_EN = 0, Bus = 1 to 10 Mbps	—	11	15.3	mA
Supply current (receiver disabled, driver enabled, over specified bus common mode voltage range)	IDD1	Rx_ENb = 1, Tx_EN = 1, Tx = 0	—	2.9	3.5	mA
		Rx_ENb = 1, Tx_EN = 1, Tx = 1	—	3.5	4.0	mA
		Rx_ENb = 1, Tx_EN = 1, Bus = 1 to 10 Mbps	—	3.2	3.8	mA
	IDD2	Rx_ENb = 1, Tx_EN = 1 , Tx = 0,1	—	49.4	84.5	mA
		Rx_ENb = 1, Tx_EN = 1, Tx = 1 Mbps	—	49.5	85.5	mA
		Rx_ENb = 1, Tx_EN = 1, Tx = 1 Mbps (Si85833, Si85837 only)	—	57.5	92	mA
		Rx_ENb = 1, Tx_EN = 1, Tx = 10 Mbps	—	59.7	98	mA
Supply current (receiver and driver enabled, over specified bus common mode voltage range)	IDD1	Rx_ENb = 0, Tx_EN = 1, Bus open, Tx = 0	—	2.3	2.8	mA
		Rx_ENb = 0, Tx_EN = 1, Bus open, Tx = 1	—	2.9	3.5	mA
		Rx_ENb = 0, Tx_EN = 1, Tx = 1 Mbps (loop-back mode)	—	2.9	3.5	mA
		Rx_ENb = 0, Tx_EN = 1, Tx = 10 Mbps (loopback mode)	—	5.7	7.2	mA
	IDD2	Rx_ENb = 0, Tx_EN = 1, (loopback mode), Tx = 0, 1	—	35.3	40	mA
		Rx_ENb = 0, Tx_EN = 1, Tx = 1 Mbps (loopback mode)	—	50.5	85.3	mA
		Rx_ENb = 0, Tx_EN = 1, Tx = 1 Mbps (loopback mode; Si85833, Si85837 only)	—	58.5	93.3	mA
		Rx_ENb = 0, Tx_EN = 1, Tx = 10 Mbps (loopback mode)	—	60.5	98	mA
Supply current (receiver and driver disabled)	IDD1	Rx_ENb = 1, Tx_EN = 0, Bus open	—	2.2	2.5	mA
		Rx_ENb = 1, Tx_EN = 0, Bus @ 1 to 10 Mbps	—	2	3.1	mA
	IDD2	Rx_ENb = 1, Tx_EN = 0, Bus open, or 1 to 10 Mbps	—	10.9	14	mA

1. Typical specifications at 25 °C.

Table 8. Electrical Characteristics for 5.0 V Rated Part Numbers

Parameter	Symbol	Test Condition	Min	Typ[1]	Max	Unit
VDD1 positive-going undervoltage threshold	$VDD1_{UV+}$		2	2.2	2.4	V
VDD1 negative-going undervoltage threshold	$VDD1_{UV–}$		1.9	2.1	2.3	V
VDD1 undervoltage threshold hysteresis	$VDD1_{UVHYS}$		—	120	—	mV
VDD2 positive-going undervoltage threshold	$VDD2_{UV+}$		3.8	4.3	4.5	V
VDD2 negative-going undervoltage threshold	$VDD2_{UV–}$		3.7	4.2	4.4	V
VDD2 undervoltage threshold hysteresis	$VDD2_{UVHYS}$		—	120	—	mV
Driver						
Open circuit differential output voltage	V_{OD}	No Load, see Figure 7, “Measurement for Driver Differential Voltage V_{OD}, No Load,” on page 15.	3.4	3.9	4.8	V
Differential output voltage steady state	$V_{OD(SS)}$	RL = 54 Ω, see Figure 8, “Measurement for Driver Differential Voltage, V_{OD} with Load,” on page 15.	1.8	2.3	2.7	V
Change in differential output steady state	$\Delta V_{OD(SS)}$	RL = 54 Ω, see Figure 8, “Measurement for Driver Differential Voltage, V_{OD} with Load,” on page 15.	–0.2	0	0.2	V
Common mode output voltage steady state	$V_{OC(SS)}$	RL = 54 Ω, see Figure 9, “Measurement for Driver Common-Mode Voltage V_{OC},” on page 15.	1.7	2.5	3.3	V
Change in common mode output voltage steady state	$\Delta V_{OC(SS)}$	RL = 54 Ω, see Figure 9, “Measurement for Driver Common-Mode Voltage V_{OC},” on page 15.	–0.2	0	0.2	V
Short circuit steady state output current	$I_{OS(SS)}$	Tx_EN = 1, see Figure 10, “Short Circuit Current Measurement,” on page 15.	–250	—	250	mA
Receiver						
Positive going differential input threshold voltage	V_{IT+}	IO = –8 mA	–156	–91	–20	mV
Negative-going differential input threshold voltage	$V_{IT–}$	IO = –8 mA	–197	–142	–76	mV
Input hysteresis voltage	$V_{(HYS)}$		—	50.5	—	mV
Single ended input resistance	R_A, R_B		86	134	223	kΩ
Differential input resistance	R_{ID}		174	269	439	kΩ
High level output voltage: Rx	V_{OH}	V_{ID} = 200 mV, I_{OH} = –4 mA	VDD1 – 0.4	—	—	V
High level output voltage: Rx	V_{OH}	V_{ID} = 200 mV, I_{OH} = –20 µA	VDD1 – 0.1	—	—	V
Low level output voltage: Rx	V_{OL}	V_{ID} = –200 mV I_{OL} = 4 mA	—	—	0.4	V
Low level output voltage: Rx	V_{OL}	V_{ID} = –200 mV I_{OL} = 20 µA	—	—	0.1	V
Bus input current	I_A, I_B		–150	—	150	µA
Low level input current: Tx, Tx_EN, Rx_ENb			–10	—	—	µA
High level input current: Tx, Tx_EN, Rx_ENb			—	—	10	µA
Switching Characteristics						
Data rate (Si85855/56/58)			—	—	10	Mbps
Data rate (Si85853/57)			—	—	1	Mbps
Driver propagation delay (Si85855/56/58)	Tx_t_{PLH}, Tx_t_{PHL}	R_L = 54 Ω, C_L = 50 pF, see Figure 11, “Measurement for Driver Timing Characteristics,” on page 16.	—	17	26	ns
Driver rise/fall time (Si85855/56/58)	Tx_t_r, Tx_t_f	R_L = 54 Ω, C_L = 50 pF, see Figure 11, “Measurement for Driver Timing Characteristics,” on page 16.	—	8.5	13.5	ns
Driver pulse skew $\vert(t_{PHL}–t_{PLH}\vert$ (Si85855/56/58)	Tx_t_{PSK}	R_L = 54 Ω, C_L = 50 pF, see Figure 11, “Measurement for Driver Timing Characteristics,” on page 16.	—	0.5	5	ns

Table 8. Electrical Characteristics for 5.0 V Rated Part Numbers (Continued)

Parameter	Symbol	Test Condition	Min	Typ[1]	Max	Unit
Driver propagation delay (Si85853/57)	Tx_t_{PLH}, Tx_t_{PHL}	RL = 54 Ω, CL = 50 pF, see Figure 11, "Measurement for Driver Timing Characteristics," on page 16.	—	101	140	ns
Driver rise/fall time (Si85853/57)	Tx_t_r, Tx_t_f	RL = 54 Ω, CL = 50 pF, see Figure 11, "Measurement for Driver Timing Characteristics," on page 16.	—	95	145	ns
Driver pulse skew (t_{PHL}–t_{PLH}) (Si85853/57)	Tx_t_{PSK}	R_L = 54 Ω, C_L = 50 pF, see Figure 11, "Measurement for Driver Timing Characteristics," on page 16.	—	3	10	ns
Driver enable time	Tx_t_{PZH}, Tx_t_{PZL}	Pullup/down 4 mA, see Figure 12, "Enable/Disable Delay Measurements," on page 16.	—	30	70	ns
Driver disable delay time	Tx_t_{PHZ}, Tx_t_{PLZ}	Pullup/down 4 mA, see Figure 12, "Enable/Disable Delay Measurements," on page 16.	—	300	500	ns
Receiver propagation delay (Si85855/56/58)	Rx_t_{PLH}, Rx_t_{PHL}	C_L = 15 pF, see Figure 13, "Measurement for Receiver Output and Timing Characteristics," on page 16.	—	67	89	ns
Receiver pulse skew (t_{PHL}-t_{PLH}) (Si85855/56/58)	Rx_t_{PSK}	C_L = 15 pF, see Figure 13, "Measurement for Receiver Output and Timing Characteristics," on page 16.	—	1.5	8.3	ns
Receiver propagation delay (Si85853/57)	Rx_t_{PLH}, Rx_t_{PHL}	C_L = 15 pF, see Figure 13, "Measurement for Receiver Output and Timing Characteristics," on page 16.	—	42	64	ns
Receiver pulse skew (t_{PHL}-t_{PLH}) (Si85853/57)	Rx_t_{PSK}	C_L = 15 pF, see Figure 13, "Measurement for Receiver Output and Timing Characteristics," on page 16.	—	1.2	7.8	ns
Receiver rise/fall time	Rx_t_r, Rx_t_f	C_L = 15 pF, see Figure 13, "Measurement for Receiver Output and Timing Characteristics," on page 16.	—	3	8.7	ns
Receiver enable/disable delay time	Rx_t_{PZH}, Rx_t_{PZL}, Rx_t_{PHZ}, Rx_t_{PLZ}	C_L = 15 pF	—	20	25	ns
Delay from VDD2 power loss to Rx = 1			—	—	6	µs
Common mode transient immunity	CMTI	V_I = VDD or 0 V V_{CM} = 1500 V (See Figure 14, "Common-Mode Transient Immunity," on page 17)	100	—	—	kV/µs
Start-up time	t_{START}		—	—	300	µs

1. Typical specifications at 25 °C.

Table 9. Electrical Characteristics for 3.3 V Rated Part Numbers

Parameter	Symbol	Test Condition	Min	Typ[1]	Max	Unit
VDD1 positive-going undervoltage threshold	$VDD1_{UV+}$		2	2.2	2.4	V
VDD1 negative-going undervoltage threshold	$VDD1_{UV–}$		1.9	2.1	2.3	V
VDD1 undervoltage threshold hysteresis	$VDD1_{UVHYS}$		—	120	—	mV
VDD2 positive-going undervoltage threshold	$VDD2_{UV+}$		2.85	3.0	3.15	V
VDD2 negative-going undervoltage threshold	$VDD2_{UV–}$		2.8	2.95	3.1	V
VDD2 undervoltage threshold hysteresis	$VDD2_{UVHYS}$		—	50	—	mV
Driver						
Open-circuit differential output voltage	V_{OD}	No Load, see Figure 7, "Measurement for Driver Differential Voltage V_{OD}, No Load," on page 15.	3	3.3	3.5	V
Differential output voltage steady state	$V_{OD(SS)}$	RL = 54 Ω, see Figure 8, "Measurement for Driver Differential Voltage, V_{OD} with Load," on page 15.	1.5	2	2.6	V
Change in differential output steady state	$\Delta V_{OD(SS)}$	RL = 54 Ω, see Figure 8, "Measurement for Driver Differential Voltage, V_{OD} with Load," on page 15.	–0.2	0	0.2	V
Common-mode output voltage steady state	$V_{OC(SS)}$	RL = 54 Ω, see Figure 9, "Measurement for Driver Common-Mode Voltage V_{OC}," on page 15.	1	1.7	2.5	V
Change in common-mode output voltage steady state	$\Delta V_{OC(SS)}$	RL = 54 Ω, see Figure 9, "Measurement for Driver Common-Mode Voltage V_{OC}," on page 15.	–0.2	0	0.2	V
Short-circuit steady-state output current	$I_{OS(SS)}$	Tx_EN = 1, see Figure 10, "Short Circuit Current Measurement," on page 15.	–250	—	250	mA
Receiver						
Positive-going differential input threshold voltage	V_{IT+}	IO = –8 mA	–178	–90	–4	mV
Negative-going differential input threshold voltage	$V_{IT–}$	IO = –8 mA	–200	–140	–73	mV
Input hysteresis voltage	$V_{(HYS)}$		—	50.5	—	mV
Single ended input resistance (Si85833/5/6)	R_A, R_B		60	90	193	kΩ
Differential input resistance (Si85833/5/6)	R_{ID}		130	180	386	kΩ
Single ended input resistance (Si85837/8)	R_A, R_B		86	134	223	kΩ
Differential input resistance (Si85837/8)	R_{ID}		174	269	439	kΩ
High-level output voltage: Rx	V_{OH}	V_{ID} = 200 mV, I_{OH} = –4 mA	VDD1 – 0.4	—	—	V
High-level output voltage: Rx	V_{OH}	V_{ID} = 200 mV, I_{OH} = –20 µA	VDD1 – 0.1	—	—	V
Low-level output voltage: Rx	V_{OL}	V_{ID} = –200 mV I_{OL} = 4 mA	—	—	0.4	V
Low-level output voltage: Rx	V_{OL}	V_{ID} = –200 mV I_{OL} = 20 µA	—	—	0.1	V
Bus input current	I_A, I_B		–220	—	220	µA
Low level input current: TX, TX_EN, Rx_ENb			–10	—	—	µA
High level input current: TX, TX_EN, Rx_ENb			—	—	10	µA
Switching Characteristics						
Data rate (Si85835/36/38)			—	—	10	Mbps
Data rate (Si85833/37)			—	—	1	Mbps
Driver propagation delay (Si85835/36/38)	Tx_t_{PLH}, Tx_t_{PHL}	R_L = 54 Ω, C_L = 50 pF, see Figure 11, "Measurement for Driver Timing Characteristics," on page 16.	—	20	30	ns

Table 9. Electrical Characteristics for 3.3 V Rated Part Numbers (Continued)

Parameter	Symbol	Test Condition	Min	Typ[1]	Max	Unit
Driver rise/fall time (Si85835/36/38)	Tx_t_r, Tx_t_f	R_L = 54 Ω, C_L = 50 pF, see Figure 11, "Measurement for Driver Timing Characteristics," on page 16.	—	10.5	14.5	ns
Driver pulse skew |(t_{PHL}–t_{PLH})| (Si85835/36/38)	Tx_t_{PSK}	R_L = 54 Ω, C_L = 50 pF, see Figure 11, "Measurement for Driver Timing Characteristics," on page 16.	—	0.6	5	ns
Driver propagation delay (Si85833/37)	Tx_t_{PLH}, Tx_t_{PHL}	R_L = 54 Ω, C_L = 50 pF, see Figure 11, "Measurement for Driver Timing Characteristics," on page 16.	—	83	130	ns
Driver rise/fall time (Si85833/37)	Tx_t_r, Tx_t_f	R_L = 54 Ω, C_L = 50 pF, see Figure 11, "Measurement for Driver Timing Characteristics," on page 16.	—	118	165	ns
Driver pulse skew (t_{PHL}–t_{PLH}) (Si85833/37)	Tx_t_{PSK}	R_L = 54 Ω, C_L = 50 pF, see Figure 11, "Measurement for Driver Timing Characteristics," on page 16.	—	1	10	ns
Driver enable time	Tx_t_{PZH}, Tx_t_{PZL}	Pullup/down 4 mA, see Figure 12, "Enable/Disable Delay Measurements," on page 16.	—	30	84	ns
Driver disable delay time	Tx_t_{PHZ}, Tx_t_{PLZ}	Pullup/down 4 mA, see Figure 12, "Enable/Disable Delay Measurements," on page 16.	—	300	500	ns
Receiver propagation delay (Si85835/36/38)		C_L = 15 pF, see Figure 13, "Measurement for Receiver Output and Timing Characteristics," on page 16.	—	73	91	ns
Receiver pulse skew (t_{PHL}–t_{PLH}) (Si85835/36/38)	Rx_t_{PSK}	C_L = 15 pF, see Figure 13, "Measurement for Receiver Output and Timing Characteristics," on page 16.	—	1.5	10	ns
Receiver propagation delay (Si85833/37)	Rx_t_{PLH}, Rx_t_{PHL}	C_L = 15 pF, see Figure 13, "Measurement for Receiver Output and Timing Characteristics," on page 16.	—	43	61	ns
Receiver pulse skew (t_{PHL}–t_{PLH}) (Si85833/37)	Rx_t_{PSK}	C_L = 15 pF, see Figure 13, "Measurement for Receiver Output and Timing Characteristics," on page 16.	—	1.2	10	ns
Receiver rise/fall time	Rx_t_r, Rx_t_f	C_L = 15 pF, see Figure 13, "Measurement for Receiver Output and Timing Characteristics," on page 16.	—	3	8.7	ns
Receiver enable/disable delay time	Rx_t_{PZH}, Rx_t_{PZL}, Rx_t_{PHZ}, Rx_t_{PLZ}	CL = 15 pF	—	25	30	ns
Delay from VDD2 power loss to Rx = 1			—	—	6	µs
Common mode transient immunity	CMTI	V_I = VDD or 0 V V_{CM} = 1500 V (See Figure 14, "Common-Mode Transient Immunity," on page 17)	100	—	—	kV/µs
Start-up time	t_{START}		—	—	300	µs

1. Typical specifications at 25 °C.

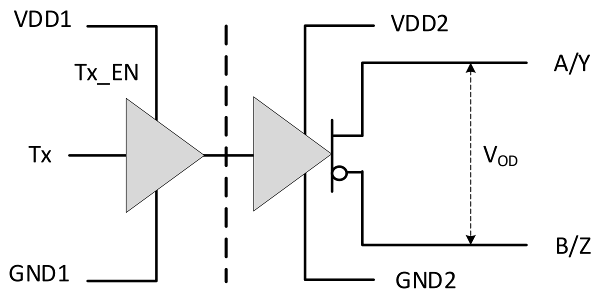

Figure 7. Measurement for Driver Differential Voltage V_{OD}, No Load

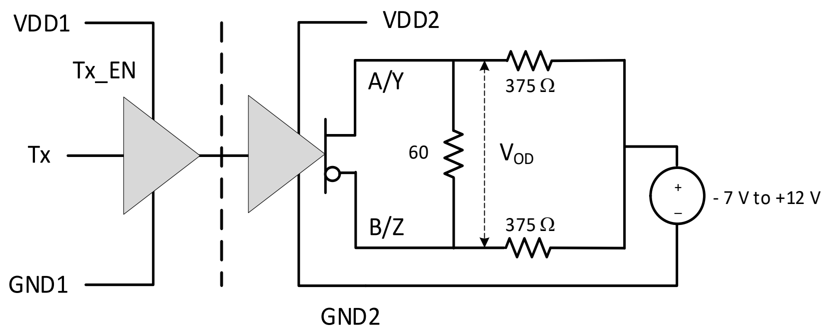

Figure 8. Measurement for Driver Differential Voltage, V_{OD} with Load

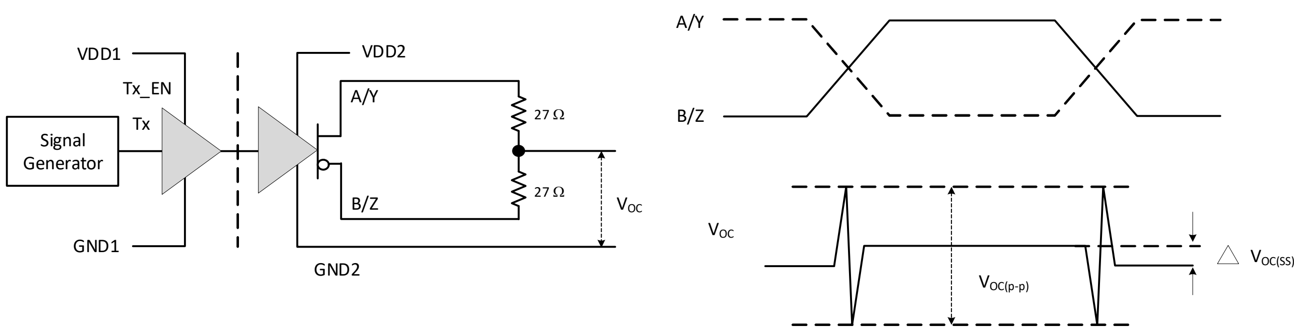

Figure 9. Measurement for Driver Common-Mode Voltage V_{OC}

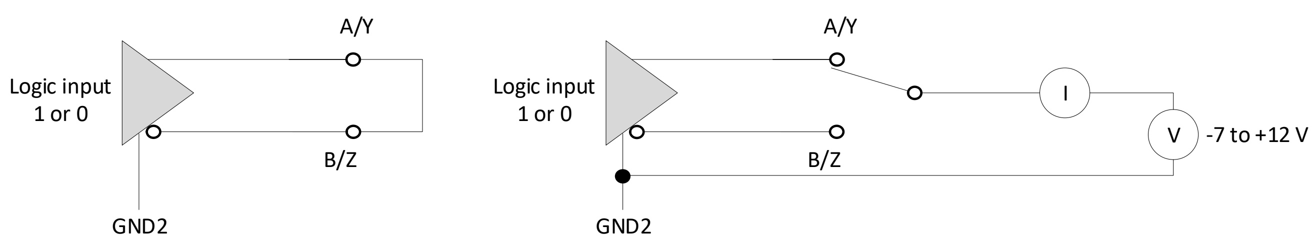

Figure 10. Short Circuit Current Measurement

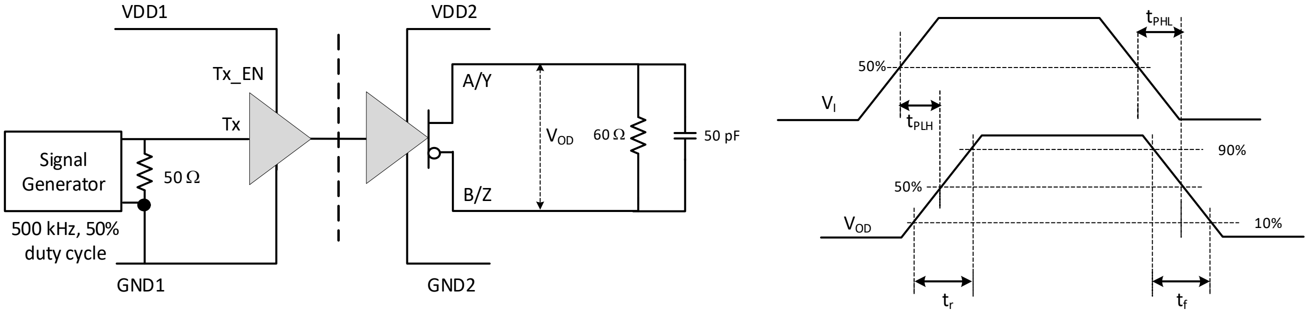

Figure 11. Measurement for Driver Timing Characteristics

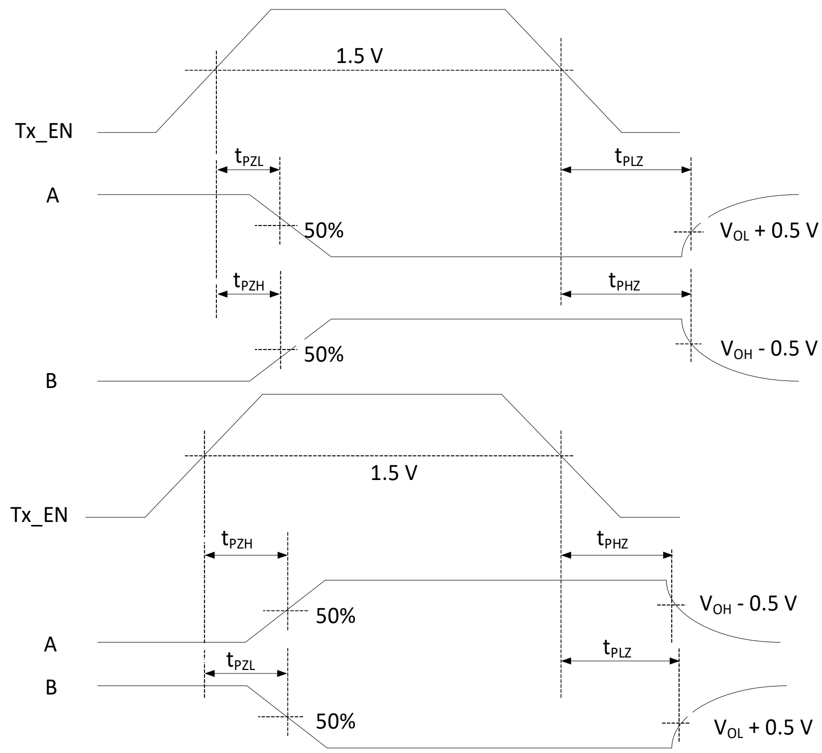

Figure 12. Enable/Disable Delay Measurements

2

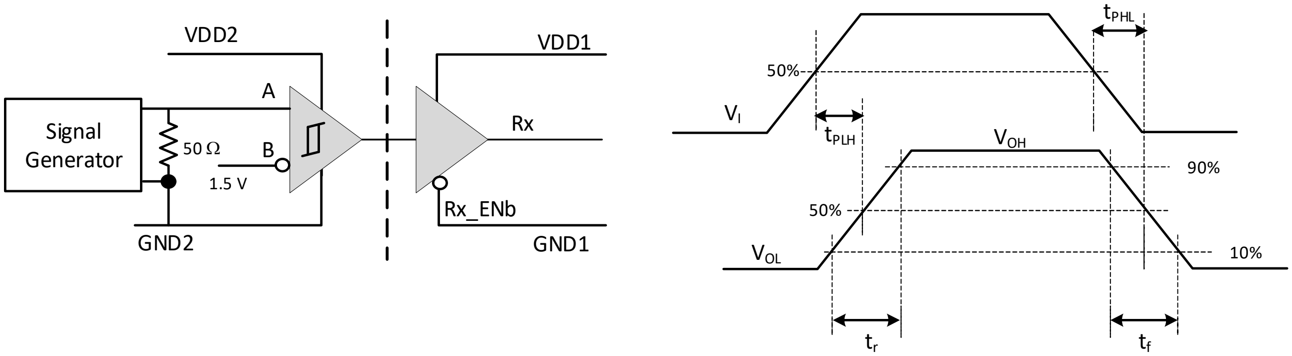

Figure 13. Measurement for Receiver Output and Timing Characteristics

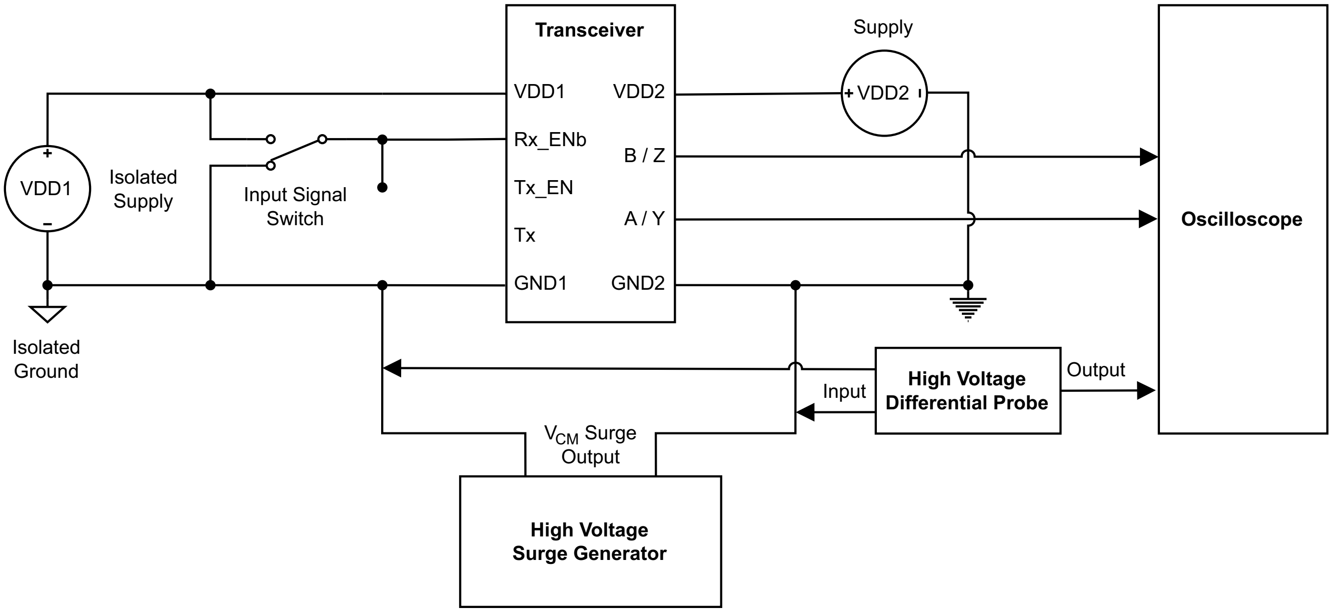

Figure 14. Common-Mode Transient Immunity

5. Safety Certifications and Specifications

Table 10. Regulatory Information (Pending)[1]

CSA
The Si858x is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si858x is certified under VDE. For more details, see File 5028467.
60747-17: Up to 2121 Vpeak for reinforced insulation working voltage.
UL
The Si858x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5.0 kV_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si858x is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see "11. Ordering Information" on page 29.

Table 11. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
Nominal external air gap (clearance)	CLR		7.6	mm
Nominal external tracking (creepage)	CRP		7.6	mm
Minimum internal gap (internal clearance)	DTI		0.036	mm
Tracking resistance	CTI or PTI	IEC60112	600	V_{RMS}
Erosion depth	ED		0.122	mm
Resistance (input-output)[1]	R_{IO}	Test voltage = 500 V, 25 °C	10^{12}	Ω
Capacitance (input-output)[1]	C_{IO}	f = 1 MHz	2.0	pF
Input capacitance[2]	C_I		4.0	pF

1. To determine resistance and capacitance, the Si858x is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 12. IEC 60664-1 Ratings

Parameter	Test Condition	Specification
Material group		I
Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–IV
	Rated mains voltage ≤ 600 V_{RMS}	I–IV
	Rated mains voltage ≤ 1000 V_{RMS}	I–III

Table 13. IEC 60747-17 Insulation Characteristics for Si858x[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	1500	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	2121	V_{peak}
Apparent charge	q_{pd}	Method b: At routine test (100% production) and preconditioning (type test); V_{ini} = 1.2 x V_{IOTM}, tini = 1 s; $V_{pd(m)}$ = 1.875 x V_{IORM}, tm = 1 s (method b1) or $V_{pd(m)}$ = V_{ini}, tm = tini (method b2)	≤ 5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	7070	V_{peak}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile	10400	V_{peak}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile	8000	V_{peak}
Isolation resistance	R_{IO_S}	T_{AMB} = T_S, V_{IO} = 500 V	>10^9	Ω
Pollution degree			2	
Climatic category			40/125/21	

1. This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 14. UL 1577 Insulation Characteristics for Si858x

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum withstanding isolation voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100% production)	5000	V_{RMS}

Table 15. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	WB SOIC-16	Unit
Safety temperature	T_S		150	°C
Safety input, output, or supply current	I_S	θ_{JA} = 73 °C/W (WB SOIC-16), $V_{DD1/2}$ = 5.5 V, T_J = 150 °C, T_A = 25 °C	311	mA
Safety input, output, or total power	P_S		1.71	W

1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 15 below.

Table 16. Thermal Characteristics

Parameter	Symbol	WB SOIC-16	Unit
IC junction-to-air thermal resistance	θ_{JA}	73	°C/W
IC junction-to-board thermal resistance	θ_{JB}	43	°C/W
IC junction-to-case thermal resistance	θ_{JC}	15	°C/W
Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.	Ψ_{JB}	41	°C/W

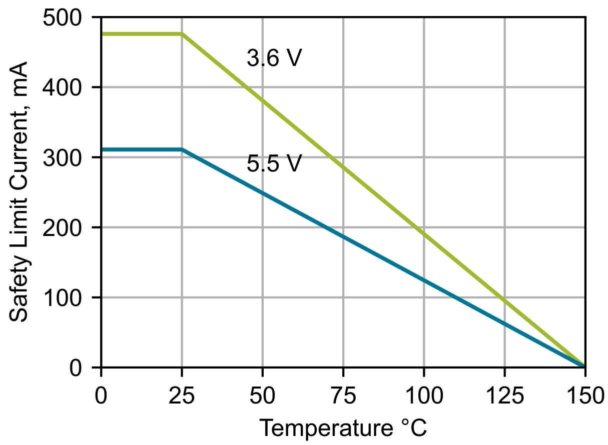

Figure 15. WB SOIC-16 Thermal Derating Curve (Dependence of Safety Limiting Current)

6. Typical Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Supply Current and Electrical Characteristics tables for actual specification limits. All typical characteristics data is valid for nominal VDD and ambient temperature of 25 °C unless specified otherwise.

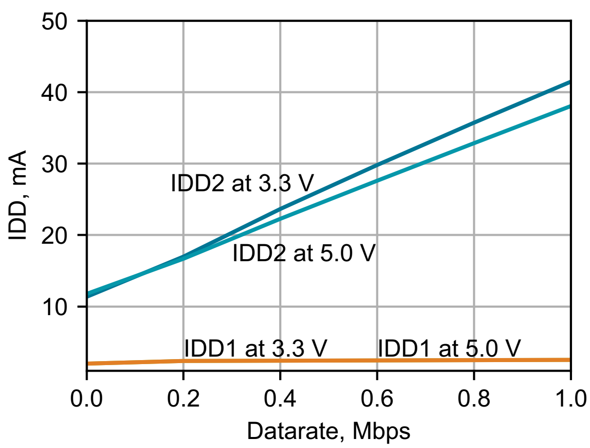

Figure 16. Si858x3/7 Supply Current vs. Data Rate, No Load

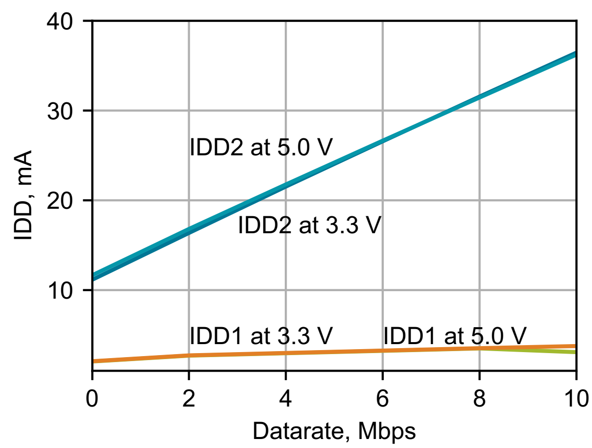

Figure 17. Si858x5/6/8 Supply Current vs. Data Rate, No Load

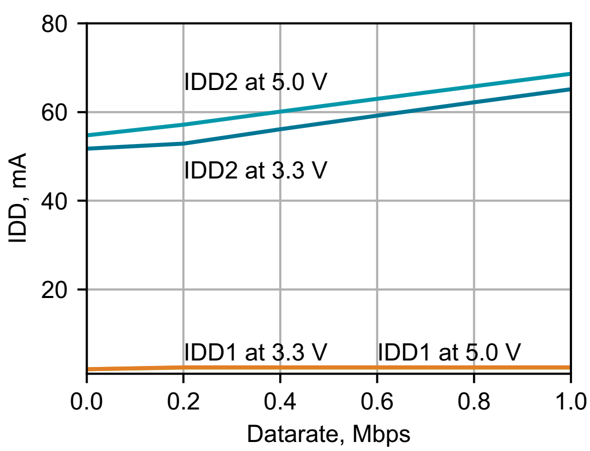

Figure 18. Si858x3/7 Supply Current vs. Data Rate, 54 Ω, 50 pF Load

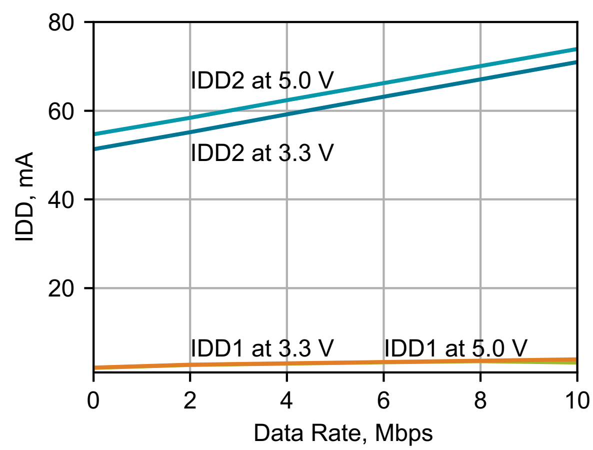

Figure 19. Si858x5/6/8 Supply Current vs. Data Rate, 54 Ω, 50 pF Load

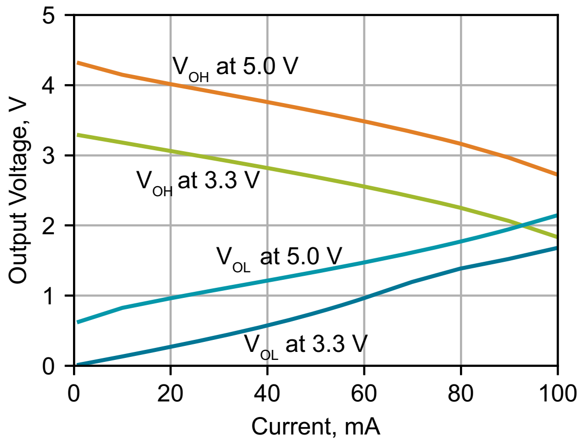

Figure 20. Driver Output Voltage vs. Current

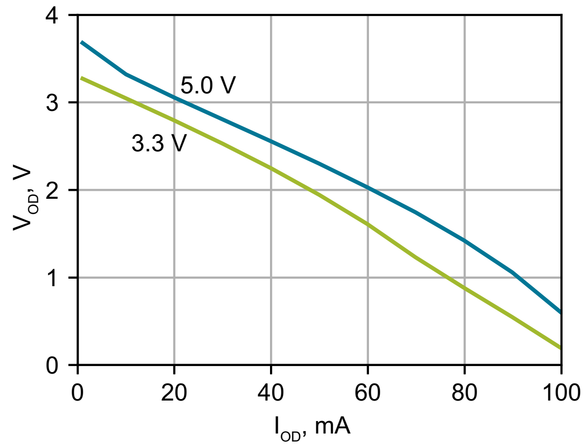

Figure 21. Driver Differential Output Voltage vs. Current

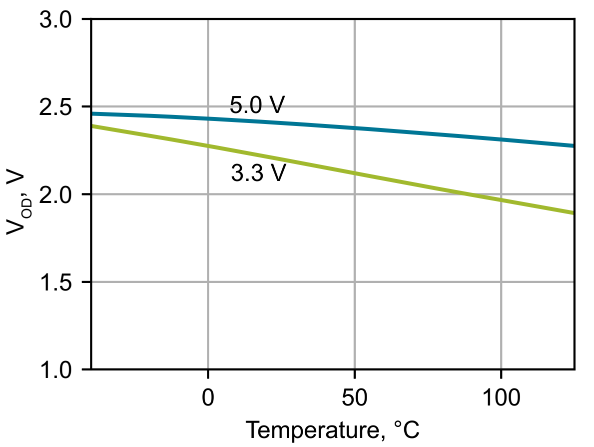

Figure 22. Driver Differential Output Voltage vs. Temperature

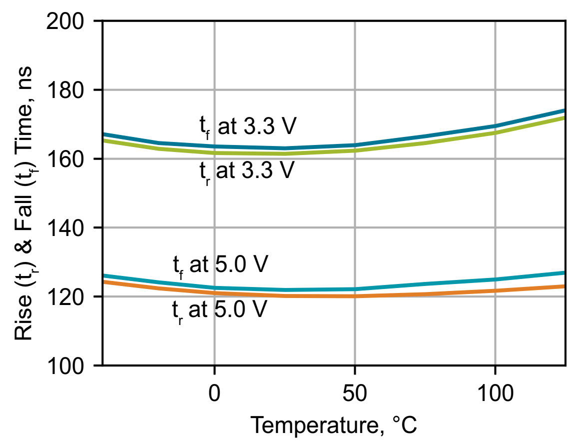

Figure 23. Si858x3/7 Driver Rise/Fall Time vs. Temperature

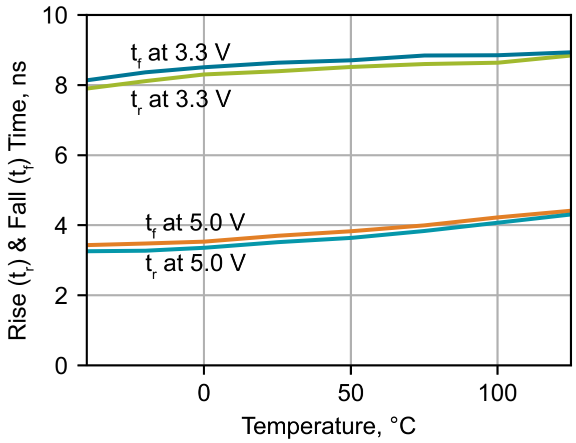

Figure 24. Si858x5/6/8 Driver Rise/Fall Time vs. Temperature

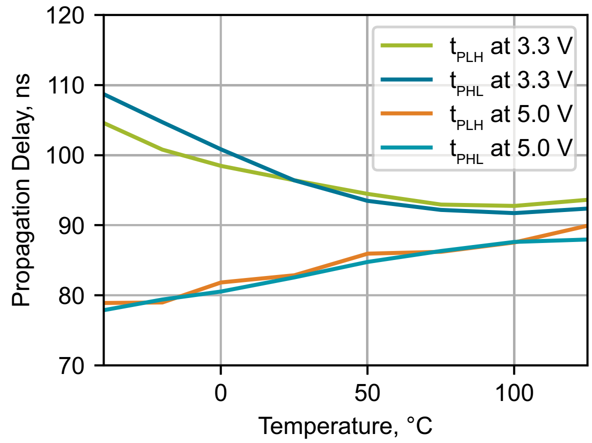

Figure 25. Si858x3/7 Driver Propagation Delay vs. Temperature

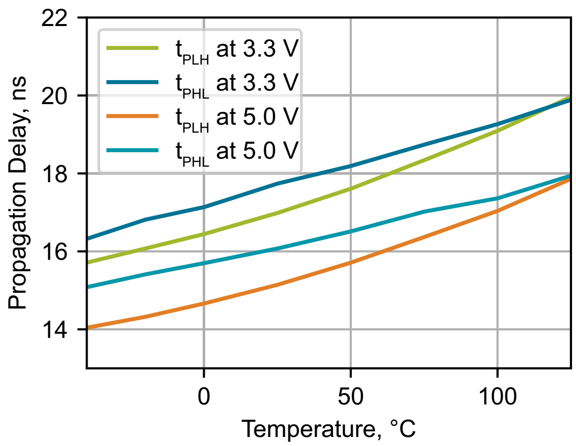

Figure 26. Si858x5/6/8 Driver Propagation Delay vs. Temperature

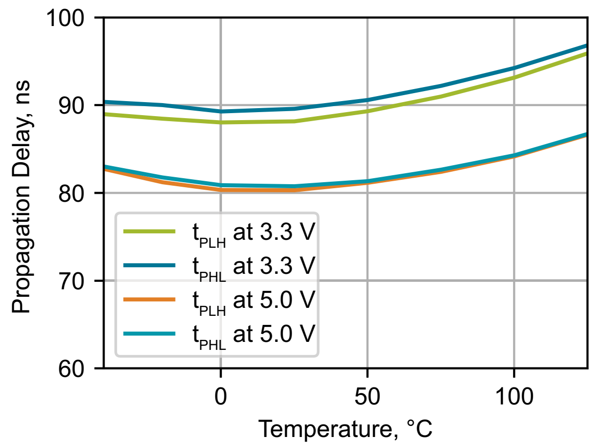

Figure 27. Receiver Propagation Delay vs. Temperature

7. Package Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The Si858x devices are rated to Moisture Sensitivity Level 2A (MSL2A) at 260 °C.

All devices can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, "PCB Design and SMT Assembly/Rework Guidelines," Document Number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Refer to Standard SMT Reflow Profiles: JEDEC Standard J-STD-020.

8. Package Outline

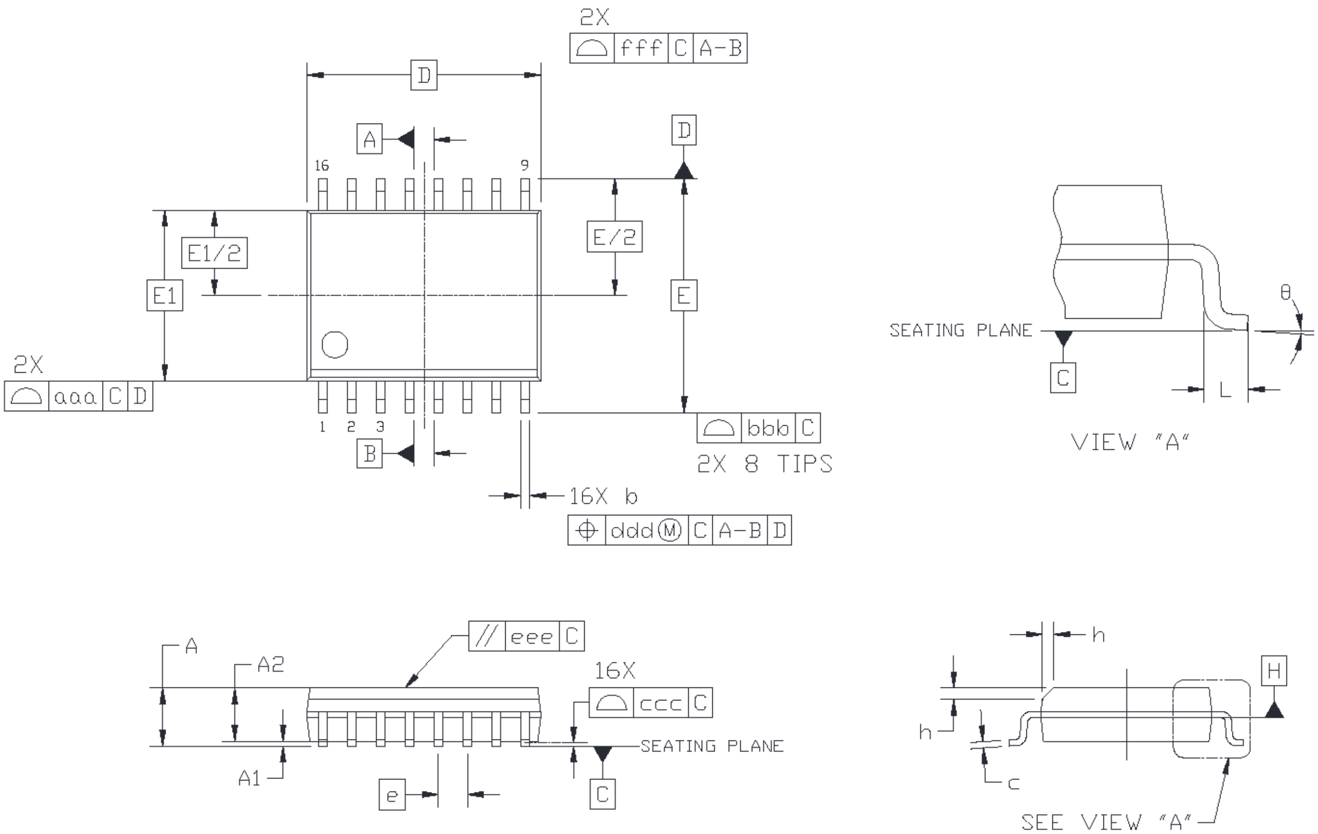

Figure 28. WB SOIC-16 Package

Table 17. Package Diagram Dimensions[1,2,3,4]

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	θ°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSIY14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. All dimensions shown are in millimeters (mm) unless otherwise noted.

9. Land Pattern

The following figure illustrates the recommended land pattern details for the Si858x in a WB SOIC-16. The table lists the values for the dimensions shown in the illustration.

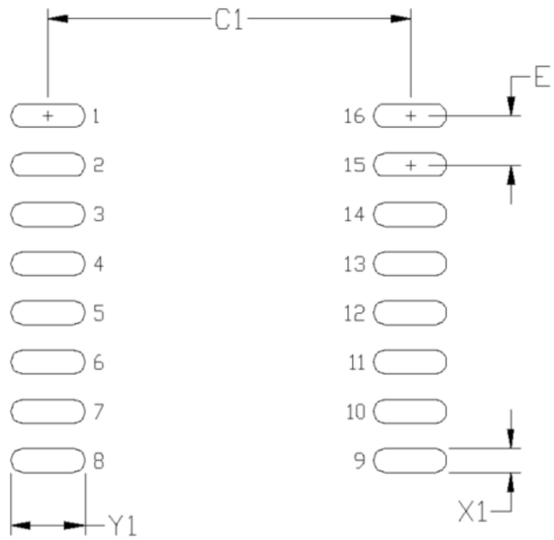

Figure 29. WB SOIC-16 PCB Land Pattern

Table 18. WB SOIC-16 Land Pattern Dimensions[1,2]

Dimension	Feature	(mm)
C1	Pad column spacing	9.40
E	Pad row pitch	1.27
X1	Pad width	0.60
Y1	Pad length	1.90

1. This land pattern design is based on IPC-7351 pattern SOIC127P1032X265-16AN for density level B (median land protrusion).
2. All feature sizes shown are at maximum material condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Top Marking

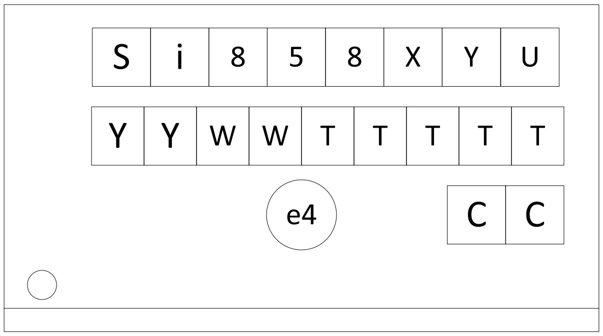

Table 19. WB SOIC-16 Top Marking Explanation

Line 1 Marking:	Base part number ordering options (See "11. Ordering Information" on page 29 for more information).	Si858 = Isolated RS-485 Transceiver X = VDD2 nominal supply voltage: 3 = 3.3 V 5 = 5.0 V Y = Transceiver type: 3 = 1 Mbps half duplex 5 = 10 Mbps half duplex 6 = 10 Mbps half duplex with isolated Tx_EN pin 7 = 1 Mbps full duplex 8 = 10 Mbps full duplex U = Isolation rating: D = 5.0 kV
Line 2 Marking:	YY = Year WW = workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	TTTTT = mfg code	Manufacturing code from assembly purchase order form.
Line 3 Marking:	Circle = 1.5 mm diameter (center-justified)	"e4" Pb-Free Symbol
	Country of origin ISO code abbreviation	TW = Taiwan

11. Ordering Information

See 10. Top Marking for product name decoder.

Table 20. Ordering Guide[1,2,3,4]

Ordering Part Number (OPN)	RS-485 Configuration	Transceiver Nodes Supported on Bus	Slew Rate Control	Data Rate (Mbps)	VDD2 (V)	Isolation Rating (kV_{RMS})
Si85853D-IS	Half duplex	256	Yes	1	5.0	5.0
Si85833D-IS	Half duplex	128	Yes	1	3.3	5.0
Si85855D-IS	Half duplex	256	No	10	5.0	5.0
Si85835D-IS	Half duplex	128	No	10	3.3	5.0
Si85856D-IS	Half duplex with isolated Tx_EN pin	256	No	10	5.0	5.0
Si85836D-IS	Half duplex with isolated Tx_EN pin	128	No	10	3.3	5.0
Si85857D-IS	Full duplex	256	Yes	1	5.0	5.0
Si85837D-IS	Full duplex	256	Yes	1	3.3	5.0
Si85858D-IS	Full duplex	256	No	10	5.0	5.0
Si85838D-IS	Full duplex	256	No	10	3.3	5.0

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An “R” at the end of the part number denotes tape and reel packaging option.
4. The temperature range is –40 to +125 °C.

12. Revision History

Revision	Date	Description
B	August, 2023	Corrected Note 1 and removed Note 2 in Table 4, “Absolute Maximum Ratings,” on page 8.
A	June, 2023	Production release.