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POWER SEQUENCER

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Rev.1.1_00

The S-77100/77101 Series is a power sequencer.
The S-77100 Series can output enable signals of 4 channels, and controls the external power supply circuit. The S-77100 Series turns on and off the enable signals successively by changing "H" and "L" of the ON pin.
The S-77101 Series can output enable signals of 3 channels, and controls the external power supply circuit. The S-77101 Series turns on the enable signals successively by changing the ON pin from "L" to "H", and turns off the enable signals successively by changing $\overline{\text{OFF}}$ pin from "H" to "L".
The delay time for each enable signal can be set by the external capacitor.
Also, the small 8-Pin TSSOP or SNT-8A package makes high-density mounting possible.

■ Features

- Easy support for sequencing of multiple power supplies.
- Delay time can be set by the external capacitor.
- Sequence operations of 4 channels can be controlled by 1 input signal. (S-77100 Series)
- On-sequence operation and off-sequence operation can be controlled by the separate input signal. (S-77101 Series)
- Enable output can be increased by cascade connection.
- Low current consumption: 3.0 μA typ. (Off period, power-good period, V_{DD} = 3.3 V, Ta = +25°C)
- Wide range of operation voltage: 2.2 V to 5.5 V
- Operation temperature range: Ta = −40°C to +85°C
- Output form is selectable: CMOS output, Nch open-drain output
- Output logic is selectable: Active "H", active "L"
- Lead-free (Sn 100%), halogen-free:

■ Applications

- Power sequencing for multiple devices
- Sequencing for microprocessor and microcontroller
- Power sequencing for FPGA
- Power sequencing for TV, camera, printer, etc.

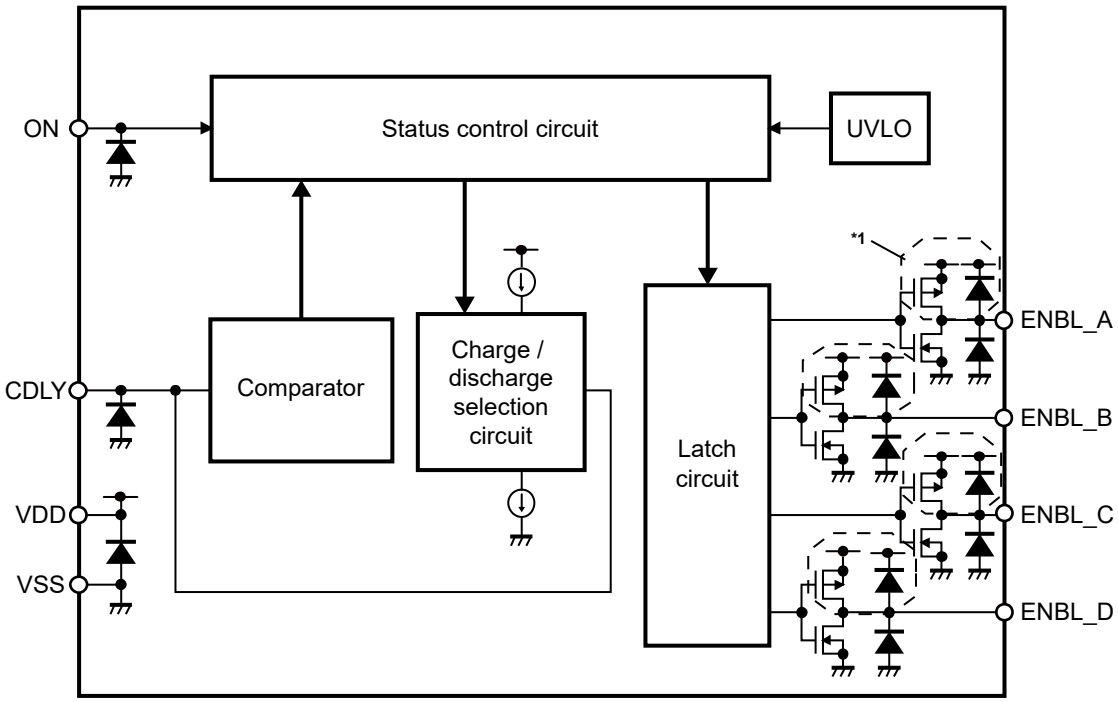
■ Packages

- 8-Pin TSSOP
- SNT-8A

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■ Block Diagrams

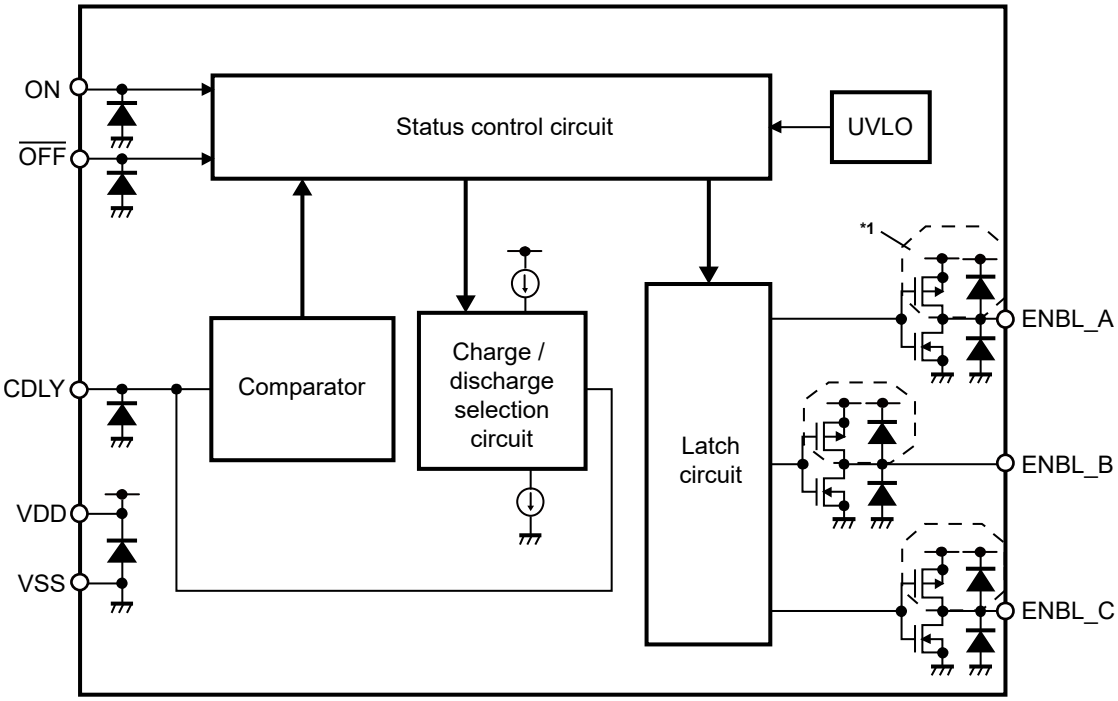
1. S-77100 Series



*1. Selectable as the option

Figure 1

2. S-77101 Series



*1. Selectable as the option

Figure 2

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■ Product Name Structure

1. Product name

S-7710 x x xx - xxxx U 4

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - T8T1: 8-Pin TSSOP, Tape
  - I8T1: SNT-8A, Tape
- Option code*2
- Order of enable output*3
  - A: Reverse type
  - B: Forward type
- Number of channel
  - 0: 4 channels (without $\overline{\text{OFF}}$ pin)
  - 1: 3 channels (with $\overline{\text{OFF}}$ pin)

***1.** Refer to the tape drawing.

***2.** Refer to "**2. Product option list**".

***3.** The order that the enable output (ENBL_x pin) inverts during off-sequence period can be selected.
The S-77100 Series
A: The ENBL_D pin, the ENBL_C pin, the ENBL_B pin and the ENBL_A pin change to "L" in turn.
B: The ENBL_A pin, the ENBL_B pin, the ENBL_C pin and the ENBL_D pin change to "L" in turn.
The S-77101 Series
A: The ENBL_C pin, the ENBL_B pin and the ENBL_A pin change to "L" in turn.
B: The ENBL_A pin, the ENBL_B pin and the ENBL_C pin change to "L" in turn.

2. Product option list

Table 1

Option Code	Number of Times of External Capacitor (C_{DLY}) Charge and Discharge*1	Input Level*2	Output Form*3	Output Logic*4
01	4	Schmitt trigger input	CMOS output	Active "H"
02	4	Schmitt trigger input	Nch open-drain output	Active "H"
11	4	Comparator input	CMOS output	Active "H"
12	4	Comparator input	Nch open-drain output	Active "H"
31	4	Comparator input	CMOS output	Active "L"

***1.** Option for the delay time (t_{DLY}) adjustment. The number of times of C_{DLY} charge and discharge can be selected.
This datasheet describes the example when "4 times" is selected.
2 times / 4 times

***2.** Input level of the ON pin and the $\overline{\text{OFF}}$ pin can be selected.
Schmitt trigger input / Comparator input

***3.** Output form of the ENBL_x pin can be selected.
CMOS output / Nch open-drain output

***4.** Output logic of the ENBL_x pin can be selected.
This datasheet describes the example when active "H" is selected.
Active "H": The type which is "H" during power-good period. /
Active "L": The type which is "L" during power-good period.

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3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
8-Pin TSSOP	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-S1	–
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

4. Product name list

4. 1 8-Pin TSSOP

Table 3

Product Name	Number of Channel	Order of Enable Output	Number of Times of C_{DLY} Charge and Discharge	Input Level	Output Form	Output Logic
S-77100A01-T8T1U4	4	Reverse type	4	Schmitt trigger input	CMOS output	Active "H"
S-77100A02-T8T1U4	4	Reverse type	4	Schmitt trigger input	Nch open-drain output	Active "H"
S-77100A12-T8T1U4	4	Reverse type	4	Comparator input	Nch open-drain output	Active "H"

4. 2 SNT-8A

Table 4

Product Name	Number of Channel	Order of Enable Output	Number of Times of C_{DLY} Charge and Discharge	Input Level	Output Form	Output Logic
S-77100A01-I8T1U4	4	Reverse type	4	Schmitt trigger input	CMOS output	Active "H"
S-77100A02-I8T1U4	4	Reverse type	4	Schmitt trigger input	Nch open-drain output	Active "H"
S-77100A31-I8T1U4	4	Reverse type	4	Comparator input	CMOS output	Active "L"
S-77100B02-I8T1U4	4	Forward type	4	Schmitt trigger input	Nch open-drain output	Active "H"
S-77100A12-I8T1U4	4	Reverse type	4	Comparator input	Nch open-drain output	Active "H"
S-77100B01-I8T1U4	4	Forward type	4	Schmitt trigger input	CMOS output	Active "H"
S-77100A11-I8T1U4	4	Reverse type	4	Comparator input	CMOS output	Active "H"

Remark Please contact our sales representatives for products other than the above.

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■ Pin Configurations

1. 8-Pin TSSOP

Top view

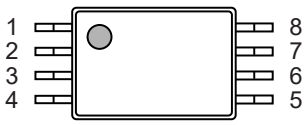


Figure 3

Table 5

Pin No.	Symbol	Description
1	ENBL_A	Enable signal output pin
2	ENBL_B	Enable signal output pin
3	CDLY	External capacitor (C_{DLY}) connection pin
4	VSS	GND pin
5	ON	Enable trigger input pin
6	ENBL_D*1	Enable signal output pin
	$\overline{OFF}$*2	Disable trigger input pin
7	ENBL_C	Enable signal output pin
8	VDD	Positive power supply pin

***1.** The S-77100 Series only
***2.** The S-77101 Series only

2. SNT-8A

Top view

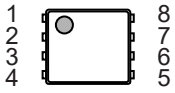


Figure 4

Table 6

Pin No.	Symbol	Description
1	ENBL_A	Enable signal output pin
2	ENBL_B	Enable signal output pin
3	CDLY	External capacitor (C_{DLY}) connection pin
4	VSS	GND pin
5	ON	Enable trigger input pin
6	ENBL_D*1	Enable signal output pin
	$\overline{OFF}$*2	Disable trigger input pin
7	ENBL_C	Enable signal output pin
8	VDD	Positive power supply pin

***1.** The S-77100 Series only
***2.** The S-77101 Series only

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■ Pin Functions

1. ON pin

This is a trigger input pin to start the sequence operation.
In the S-77100 Series, the on-sequence operation is performed when the rising signal is detected. The off-sequence operation is performed when the falling signal is detected.
In the S-77101 Series, the on-sequence operation is performed when the rising signal is detected.
Refer to "**1. Sequence operation**" in "**■ Operation**" for details.

2. $\overline{\text{OFF}}$ pin (S-77101 Series only)

This is a trigger input pin to start the off-sequence operation. The off-sequence operation is performed when the falling signal is detected. Refer to "**1. Sequence operation**" in "**■ Operation**" for details.

3. ENBL_A, ENBL_B, ENBL_C, ENBL_D pins (ENBL_D pin is S-77100 Series only)

These are pins to output the enable signals to the external power supply circuits.
The ENBL_x pin output form of Nch open-drain output / CMOS output can be selected as the option. Moreover, the ENBL_x pin output logic of active "H" / active "L" can be selected as the option.
Refer to "**1. Sequence operation**" in "**■ Operation**" for the sequence operation, "**2. Product option list**" in "**■ Product Name Structure**" for the options.

4. CDLY pin

This is a pin for connecting the external capacitor (C_{DLY}) in order to generate the delay time (t_{DLY}) of the on-sequence operation and the off-sequence operation. C_{DLY} is charged and discharged by the constant current circuit.
The charge-discharge operation starts when the ON pin rises, the period from the starting to the ENBL_A pin rising is t_{DLY} which is generated by the S-77100/77101 Series.
Refer to "**1. Sequence Operation**" in "**■ Operation**" for the operation timing, "**■ Relation between Delay Time and External Capacitor**" for the delay time.

5. VDD pin

Connect this pin with a positive power supply. Refer to "**■ Electrical Characteristics**" for the values of voltage to be applied.

6. VSS pin

Connect this pin to GND.

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■ Absolute Maximum Ratings

Table 7

Item	Symbol	Applicable Pin	Absolute Maximum Rating		Unit
Power supply voltage	V_{DD}	VDD	V_{SS} – 0.3 to V_{SS} + 6.5		V
Input voltage	V_{IN}	ON, $\overline{OFF}$ (S-77101 Series only)	V_{SS} – 0.3 to V_{DD} + 0.3*1		V
Output voltage	V_{OUT}	ENBL_A, ENBL_B, ENBL_C, ENBL_D (S-77100 Series only)	Nch open-drain output	V_{SS} – 0.3 to V_{SS} + 6.5	V
			CMOS output	V_{SS} – 0.3 to V_{DD} + 0.3*1	V
Operation ambient temperature*2	T_{opr}	–	–40 to +85		°C
Storage temperature	T_{stg}	–	–55 to +150		°C

***1.** Be sure not to exceed 6.5 V.

***2.** Conditions with no condensation or frost. Condensation or frost causes short-circuiting between pins, resulting in a malfunction.

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

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■ Electrical Characteristics

Table 8

(Ta = –40°C to +85°C, V_{DD} = 2.2 V to 5.5 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Applied Pin	Condition	Min.	Typ.*1	Max.	Unit
Operation power supply voltage	V_{DD}	VDD	–	2.2	–	5.5	V
Current consumption 1 (Off period)	I_{DD1}	VDD	V_{DD} = 3.3 V, ON pin, $\overline{OFF}$ pin*2 = V_{SS}, ENBL_x pin = Open	–	3.0	6.0	µA
Current consumption 2 (Power-good period)	I_{DD2}	VDD	V_{DD} = 3.3 V, ON pin, $\overline{OFF}$ pin*2 = V_{DD}, ENBL_x pin = Open	–	3.0	6.0	µA
Current consumption 3 (On-sequence period, off-sequence period)	I_{DD3}	VDD	V_{DD} = 3.3 V, ON pin, $\overline{OFF}$ pin*2 = V_{DD} or V_{SS}, ENBL_x pin = Open	–	–	8.0	µA
Low voltage detection voltage	V_{UVLO}	VDD	–	1.85	2.0	2.13	V
High level input leakage current	I_{IZH}	ON, $\overline{OFF}$*2	V_{IN} = V_{DD}	–0.3	–	0.3	µA
Low level input leakage current	I_{IZL}	ON, $\overline{OFF}$*2	V_{IN} = V_{SS}	–0.3	–	0.3	µA
Input voltage (When Schmitt trigger input is selected)	V_{IL}	ON, $\overline{OFF}$*2	–	V_{SS} – 0.3	–	0.2 × V_{DD}	V
	V_{IH}	ON, $\overline{OFF}$*2	–	0.8 × V_{DD}	–	V_{DD} + 0.3	V
Input threshold voltage (When comparator input is selected)	V_{IT_ON}	ON, $\overline{OFF}$*2	–	0.3	0.8	1.3	V
High level output leakage current*3	I_{OZH}	ENBL_A, ENBL_B, ENBL_C, ENBL_D*4	V_{OUT} = V_{DD}	–0.3	–	0.3	µA
Low level output leakage current*3	I_{OZL}	ENBL_A, ENBL_B, ENBL_C, ENBL_D*4	V_{OUT} = V_{SS}	–0.3	–	0.3	µA
Low level output voltage	V_{OL}	ENBL_A, ENBL_B, ENBL_C, ENBL_D*4	I_{OL} = 2.0 mA	–	–	0.4	V
High level output voltage*5	V_{OH}	ENBL_A, ENBL_B, ENBL_C, ENBL_D*4	I_{OH} = –0.4 mA	0.8 × V_{DD}	–	–	V
Delay time*6	t_{DLY}	ENBL_A, ENBL_B, ENBL_C, ENBL_D*4	Ta = +25°C, V_{DD} = 3.3 V, The period from ENBL_A pin rising to ENBL_B pin rising, C_{DLY} = 10 nF, The number of times of C_{DLY} charge and discharge = 4 times	40	45	50	ms

***1.** Typ. values are the values at the time of Ta = +25°C.
***2.** The S-77101 Series only
***3.** When Nch open-drain output is selected as the option.
***4.** The S-77100 Series only
***5.** When CMOS output is selected as the option.
***6.** The delay time varies depending on the usage environment. Perform thorough evaluation using the actual application to set the constant. Refer to "■ **Relation between Delay Time and External Capacitors**" for details.

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■ Operation

1. Sequence operation

1. 1 S-77100A (Reverse type), S-77100B (Forward type)

The S-77100 Series has enable outputs of 4 channels (the ENBL_A pin, the ENBL_B pin, the ENBL_C pin and the ENBL_D pin). The order of the off-sequence operation is different in reverse type and forward type.

1. 1. 1 Sequence operation outline

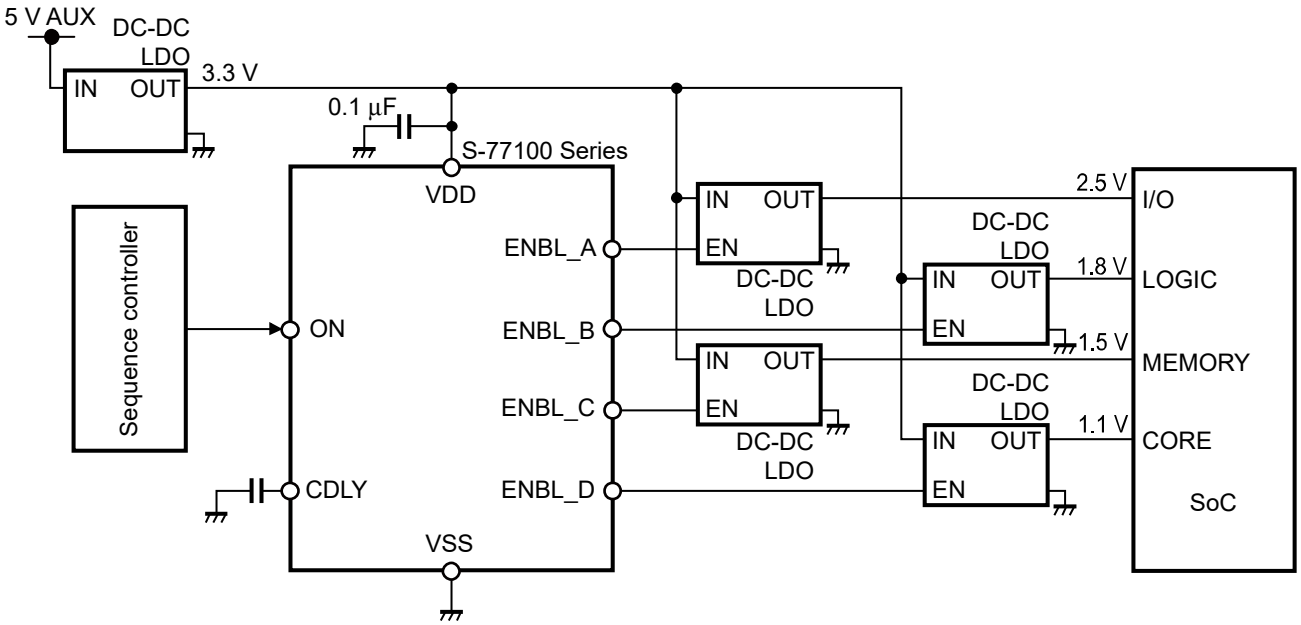
(1) On-sequence operation

After the ON pin changes from "L" to "H", the external capacitor (C_{DLY}) charge operation is started, and the discharge operation is performed when C_{DLY} is fully charged. The period during which this is repeated n times is the delay time (t_{DLY}), and the ENBL_A pin changes to "H". Similarly, each time t_{DLY} elapses, the ENBL_B pin, the ENBL_C pin and the ENBL_D pin change to "H" in turn. The period from when the ON pin changes from "L" to "H" to when the ENBL_D pin changes to "H" is called "on-sequence period".

(2) Off-sequence operation

After the ON pin changes from "H" to "L", C_{DLY} charge operation is started, and the discharge operation is performed when C_{DLY} is fully charged. The period during which this is repeated n times is t_{DLY}, and the ENBL_D pin, the ENBL_C pin, the ENBL_B pin and the ENBL_A pin change to "L" in turn in S-77100A. The ENBL_A pin, the ENBL_B pin, the ENBL_C pin and the ENBL_D pin change to "L" in turn in S-77100B. The period from when the ON pin changes from "H" to "L" to when the ENBL_A pin in S-77100A or the ENBL_D pin in S-77100B changes to "L" is called "off-sequence period".

Do not change the ON pin during on-sequence period and off-sequence period in order to perform the sequence operation normally.
The number of times of C_{DLY} charge and discharge which determines t_{DLY} can be selected from 2 times / 4 times as the option.
C_{DLY} charge operation and discharge operation to generate t_{DLY} are performed by the constant current circuit. Refer to "**■ Relation between Delay Time and External Capacitor**" for the relation of C_{DLY} and t_{DLY}.
In addition, the period from when the ENBL_A pin, the ENBL_B pin, the ENBL_C pin and the ENBL_D pin all change to "H" to when the off-sequence operation starts is called "power-good period", and the period from when the ENBL_A pin, the ENBL_B pin, the ENBL_C pin and the ENBL_D pin all change to "L" to when the on-sequence operation starts is called "off period".
Refer to **Figure 5** for the peripheral circuit connection example.
Timing charts are shown in **Figure 6** and **Figure 7** for S-77100A and S-77100B, respectively.

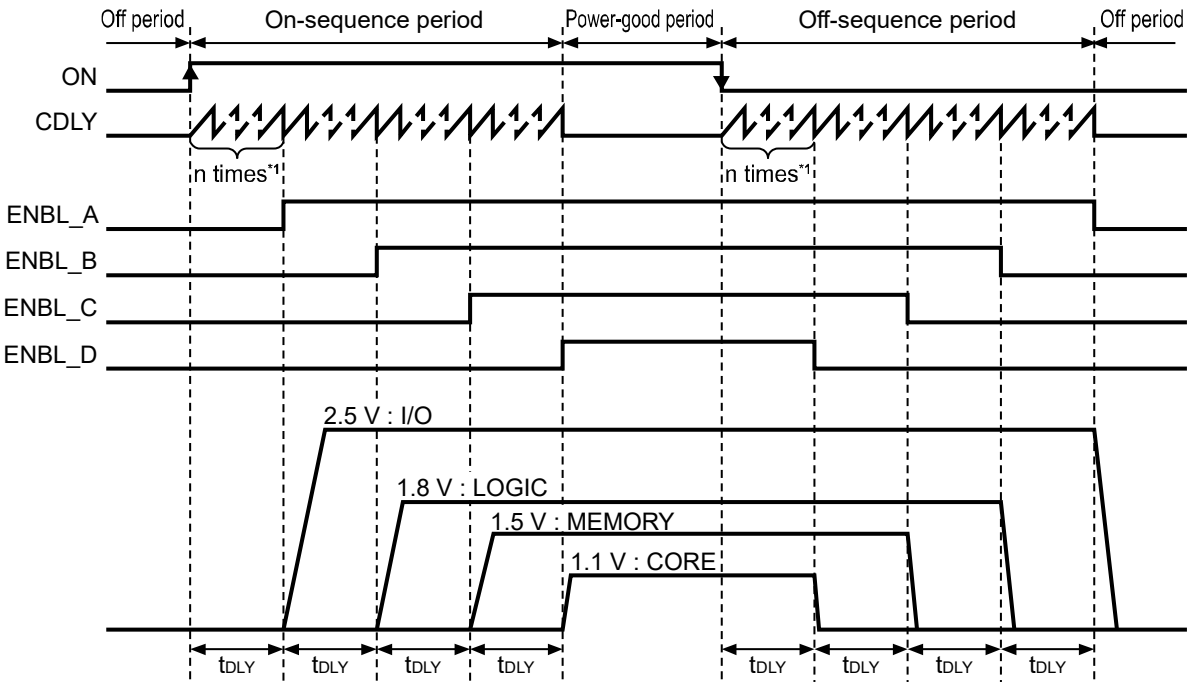


Remark The ENBL_x pin is CMOS output.

Figure 5 Peripheral Circuit Connection Example (S-77100A: Reverse type, S-77100B: Forward type)

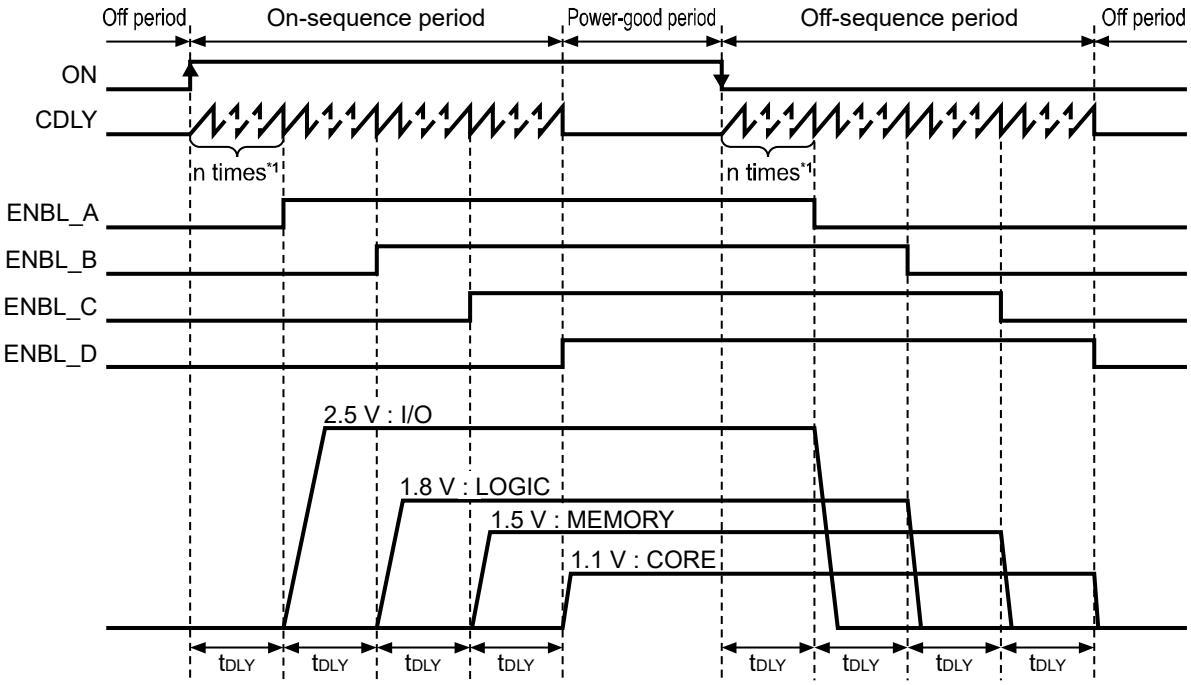
Caution 1. The input should be performed after the power supply voltage applied to the S-77100 Series becomes stable condition.
2. The above connection diagram does not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

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***1.** Selectable as the option: 2 times / 4 times

Figure 6 Timing Chart (S-77100A: Reverse Type)



***1.** Selectable as the option: 2 times / 4 times

Figure 7 Timing Chart (S-77100B: Forward type)

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1. 2 S-77101A (Reverse type, with $\overline{\text{OFF}}$ pin), S-77101B (Forward type, with $\overline{\text{OFF}}$ pin)

The S-77101 Series has enable outputs of 3 channels (the ENBL_A pin, the ENBL_B pin and the ENBL_C pin) and the $\overline{\text{OFF}}$ pin. The order of the off-sequence operation is different in reverse type and forward type.

1. 2. 1 Sequence operation outline

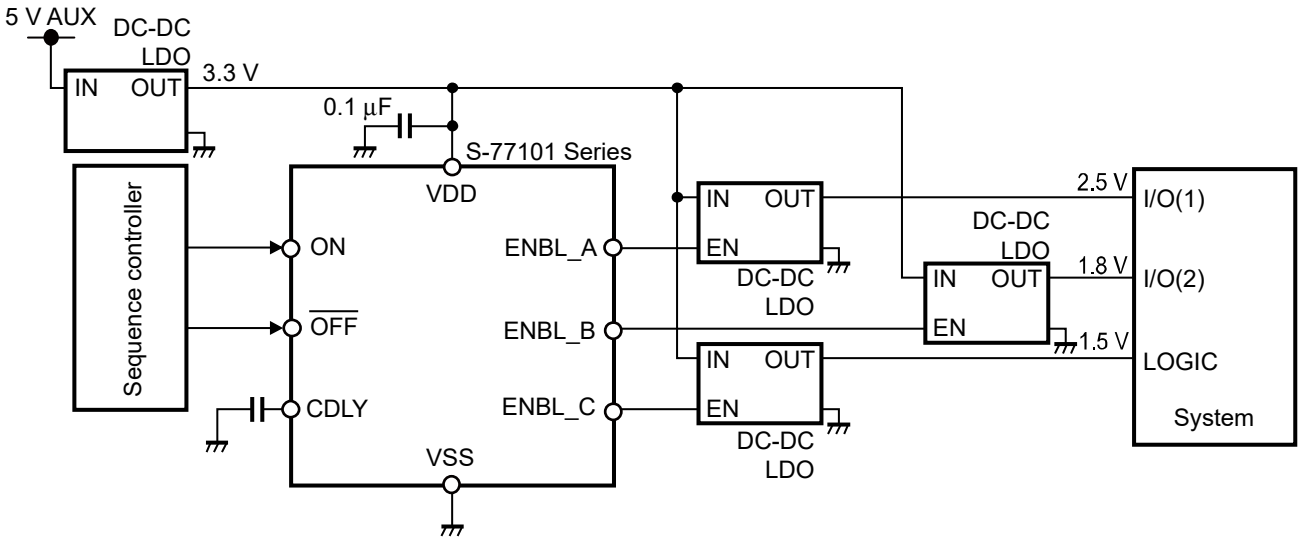
(1) On-sequence operation

After the ON pin changes from "L" to "H", the external capacitor (C_{DLY}) charge operation is started, and the discharge operation is performed when C_{DLY} is fully charged. The period during which this is repeated n times is the delay time (t_{DLY}), and the ENBL_A pin changes to "H". Similarly, each time t_{DLY} elapses, the ENBL_B pin and the ENBL_C pin change to "H" in turn. The period from when the ON pin changes from "L" to "H" to when the ENBL_C pin changes to "H" is called "on-sequence period".

(2) Off-sequence operation

After the $\overline{\text{OFF}}$ pin changes from "H" to "L", C_{DLY} charge operation is started, and the discharge operation is performed when C_{DLY} is fully charged. The period during which this is repeated n times is t_{DLY}, and the ENBL_C pin, the ENBL_B pin and the ENBL_A pin change to "L" in turn in S-77101A. The ENBL_A pin, the ENBL_B pin and the ENBL_C pin change to "L" in turn in S-77101B. The period from when the $\overline{\text{OFF}}$ pin changes from "H" to "L" to when the ENBL_A pin in S-77101A or the ENBL_C pin in S-77101B changes to "L" is called "off-sequence period".

Do not change the ON pin and the $\overline{\text{OFF}}$ pin during on-sequence period and off-sequence period in order to perform the sequence operation normally.
The number of times of C_{DLY} charge and discharge which determines t_{DLY} can be selected from 2 times / 4 times as the option. C_{DLY} charge operation and the discharge operation to generate the t_{DLY} are performed by the constant current circuit. Refer to "**■ Relation between Delay Time and External Capacitor**" for the relation of C_{DLY} and t_{DLY}.
In addition, the period from when the ENBL_A pin, the ENBL_B pin and the ENBL_C pin all change to "H" to when the off-sequence operation starts is called "power-good period", and the period from when the ENBL_A pin, the ENBL_B pin and the ENBL_C pin all change to "L" to when the on-sequence operation starts is called "off period". The sequence operation is not affected even if the ON pin changes from "H" to "L" during power-good period or the $\overline{\text{OFF}}$ pin changes from "L" to "H" during off period.
Refer to **Figure 8** for the peripheral circuit connection example.
Timing charts are shown in **Figure 9** and **Figure 10** for S-77101A and S-77101B, respectively.

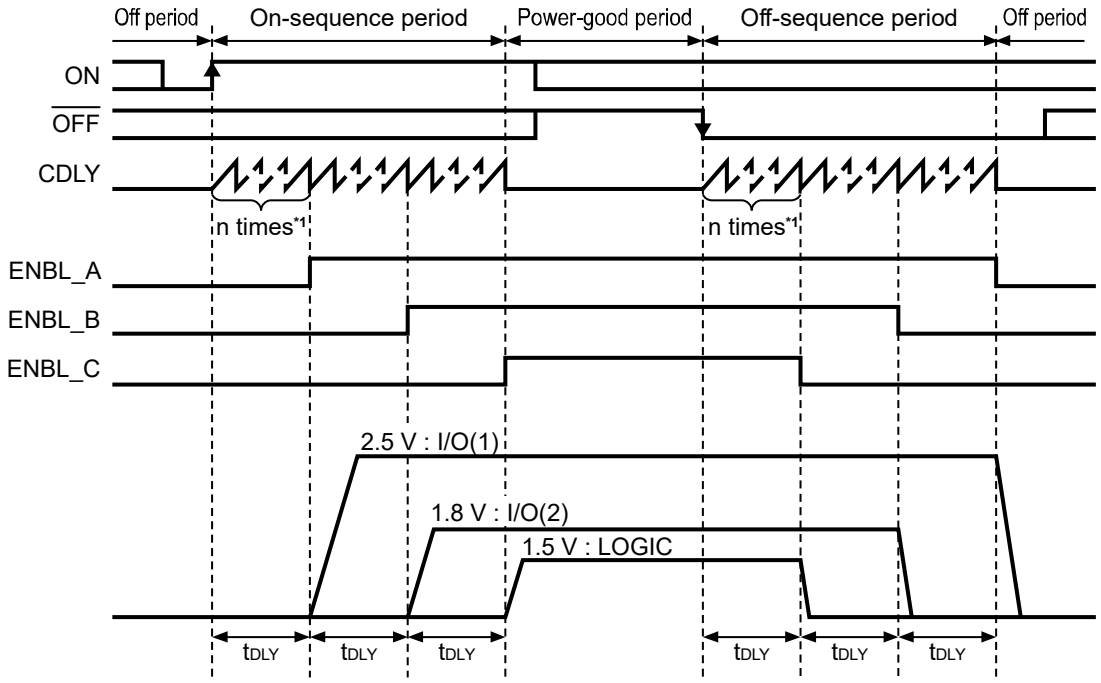


Remark The ENBL_x pin is CMOS output.

Figure 8 Peripheral Circuit Connection Example
(S-77101A: Reverse Type, with $\overline{\text{OFF}}$ pin, S-77101B: Forward Type, with $\overline{\text{OFF}}$ pin)

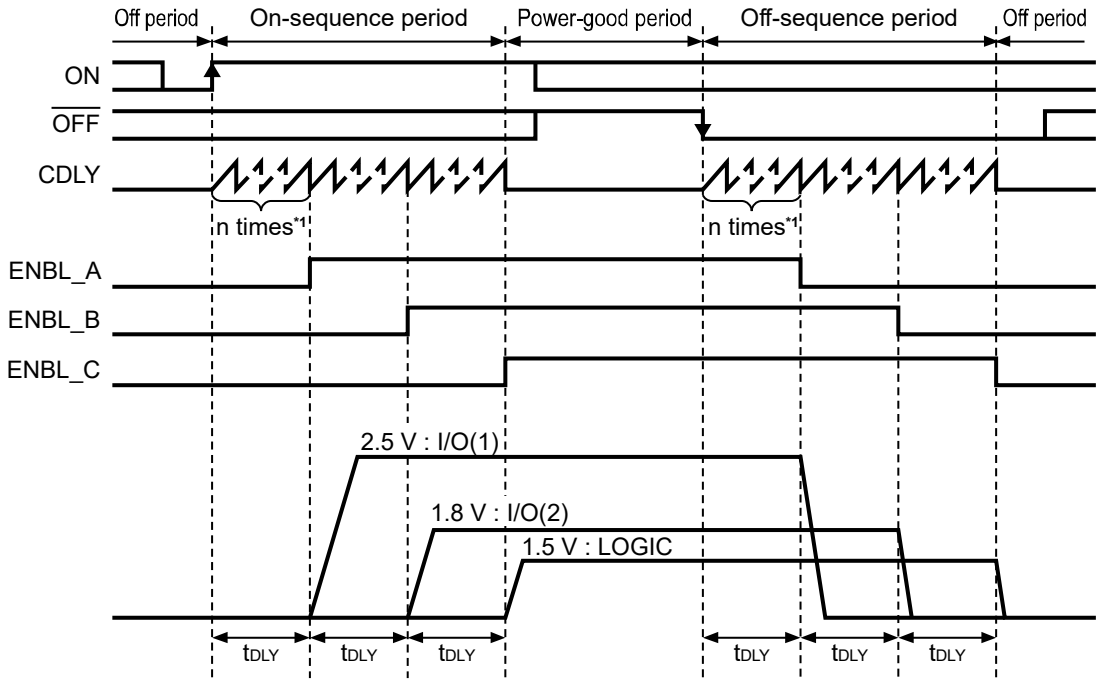
Caution 1. The input should be performed after the power supply voltage applied to the S-77101 Series becomes stable condition.
2. The above connection diagram does not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

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***1.** Selectable as the option: 2 times / 4 times

Figure 9 Timing Chart (S-77101A: Reverse Type, with $\overline{\text{OFF}}$ pin)



***1.** Selectable as the option: 2 times / 4 times

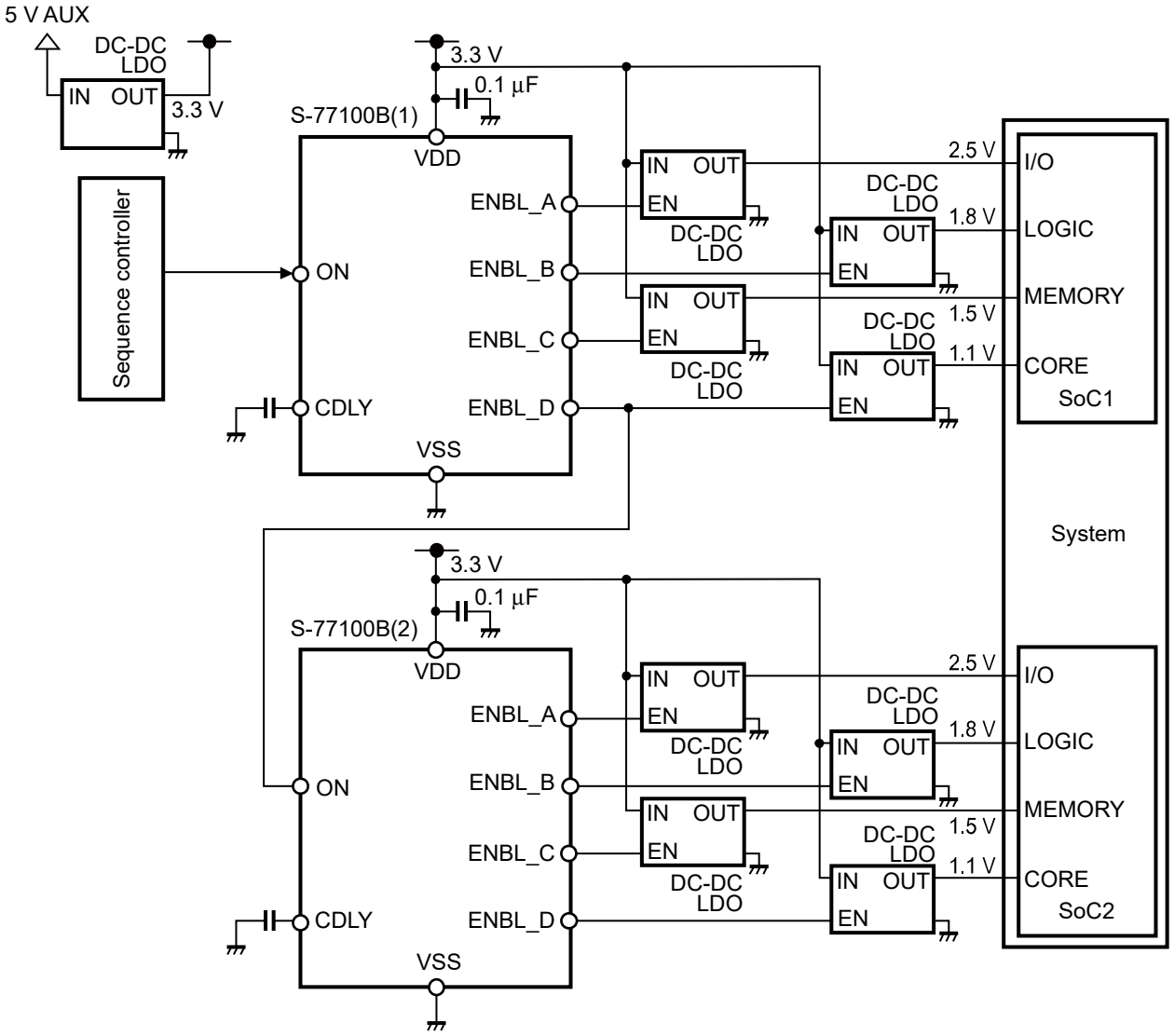
Figure 10 Timing Chart (S-77101B: Forward Type, with $\overline{\text{OFF}}$ pin)

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2. Cascade connection

2. 1 S-77100B (Forward type)

The enable output can be increased by connecting S-77100B in cascade. The peripheral circuit connection example how two S-77100B devices are connected in cascade is shown in **Figure 11**.
Connect the ENBL_D pin of S-77100B(1) and the ON pin of S-77100B(2).
Figure 12 shows the timing chart.



Remark The ENBL_x pin is CMOS output.

Figure 11 Peripheral Circuit Connection Example (S-77100B: Forward Type)

Caution 1. The input should be performed after the power supply voltage applied to S-77100B becomes stable condition.
2. The above connection diagram does not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. The external capacitors (C_{DLY}) connected to the CDLY pin of S-77100B(1) and S-77100B(2) cannot use the same capacitor.

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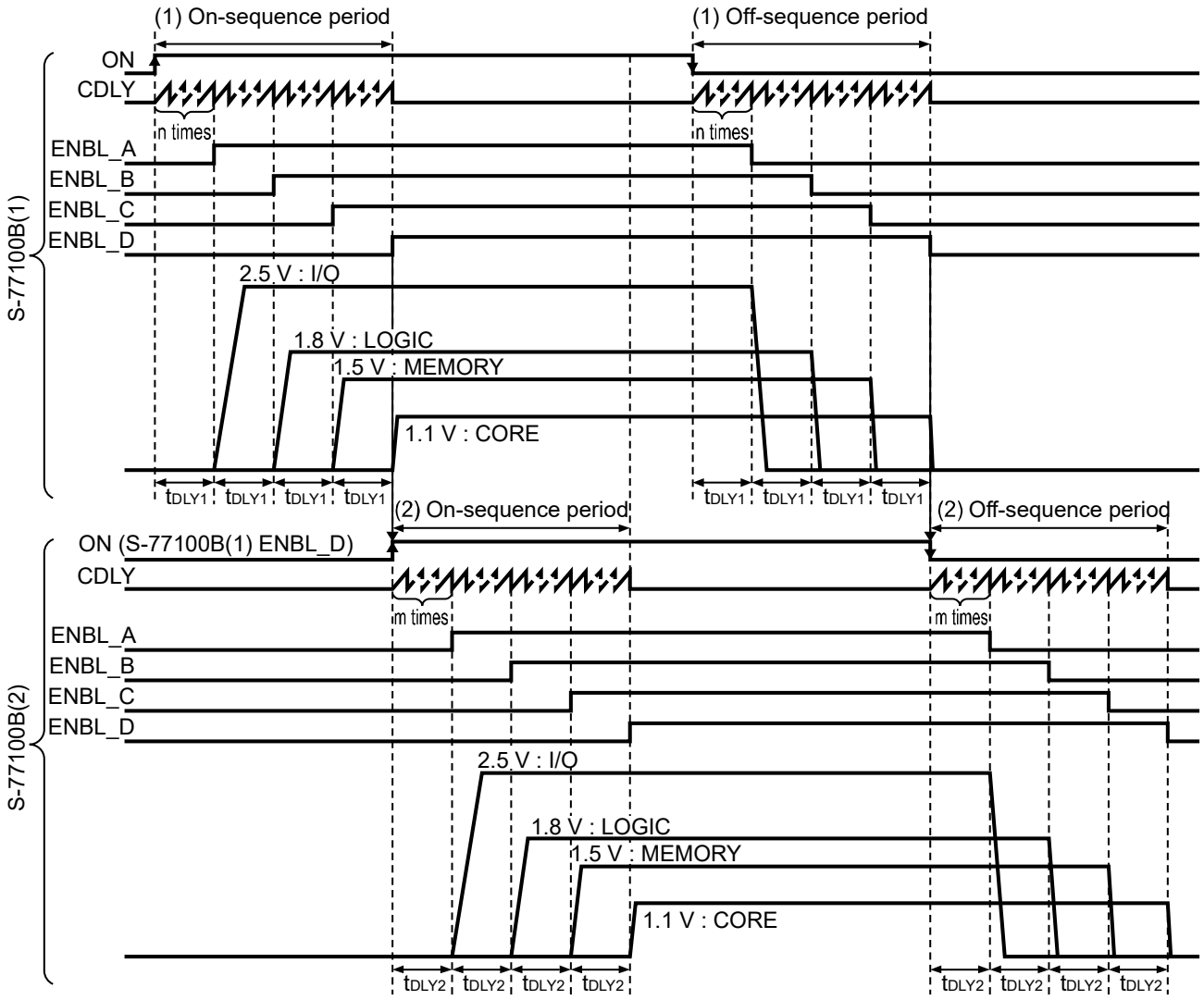


Figure 12 Timing Chart at Cascade Connection (S-77100B: Forward Type)

After the ON pin of S-77100B(1) changes from "L" to "H", the ENBL_A pin, the ENBL_B pin, the ENBL_C pin and the ENBL_D pin of S-77100B(1) change to "H" in turn.
After the ENBL_D pin of S-77100B(1) changes from "L" to "H", the ENBL_A pin, the ENBL_B pin, the ENBL_C pin and the ENBL_D pin of S-77100B(2) change to "H" in turn.

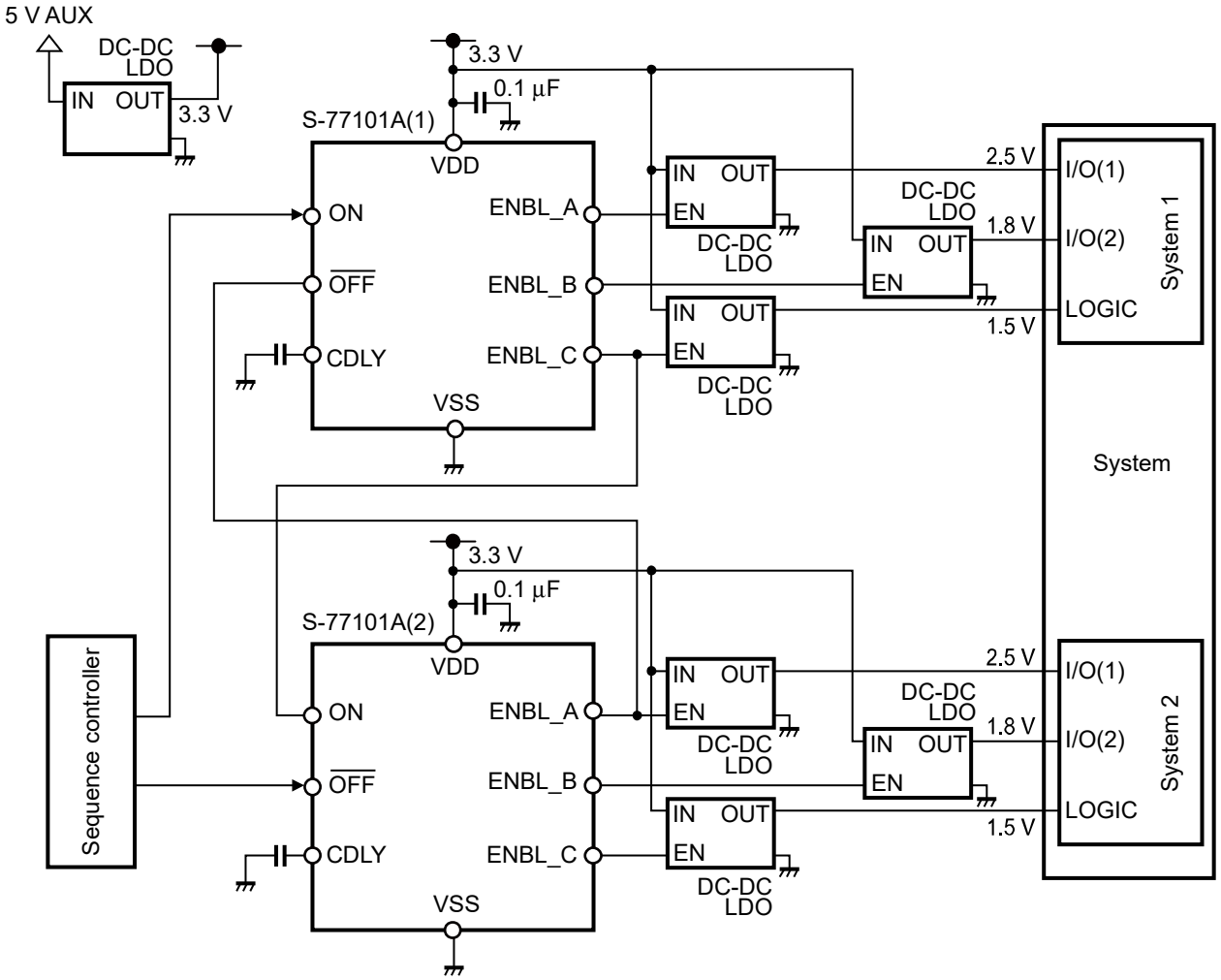
After the ON pin of S-77100B(1) changes from "H" to "L", the ENBL_A pin, the ENBL_B pin the ENBL_C pin and the ENBL_D pin of S-77100B(1) change to "L" in turn.
After the ENBL_D pin of S-77100B(1) changes from "H" to "L", the ENBL_A pin, the ENBL_B pin, the ENBL_C pin and the ENBL_D pin of S-77100B(2) change to "L" in turn.

Do not change the ON pin during on-sequence period and off-sequence period in order to perform the sequence operation normally.

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2. 2 S-77101A (Reverse type, with $\overline{\text{OFF}}$ pin)

The enable output can be increased by connecting S-77101A in cascade. The peripheral circuit connection example how two S-77101A devices are connected in cascade is shown in **Figure 13**.
Connect the ENBL_C pin of S-77101A(1) and the ON pin of S-77101A(2), and the $\overline{\text{OFF}}$ pin of S-77101A(1) and the ENBL_A pin of S-77101A(2).
Figure 14 shows the timing chart.



Remark The ENBL_x pin is CMOS output.

Figure 13 Peripheral Circuit Connection Example (S-77101A: Reverse Type, with $\overline{\text{OFF}}$ pin)

Caution 1. The input should be performed after the power supply voltage applied to S-77101A becomes stable condition.
2. The above connection diagram does not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. The external capacitors (C_{DLY}) connected to the CDLY pin of S-77101A(1) and S-77101A(2) cannot use the same capacitor.

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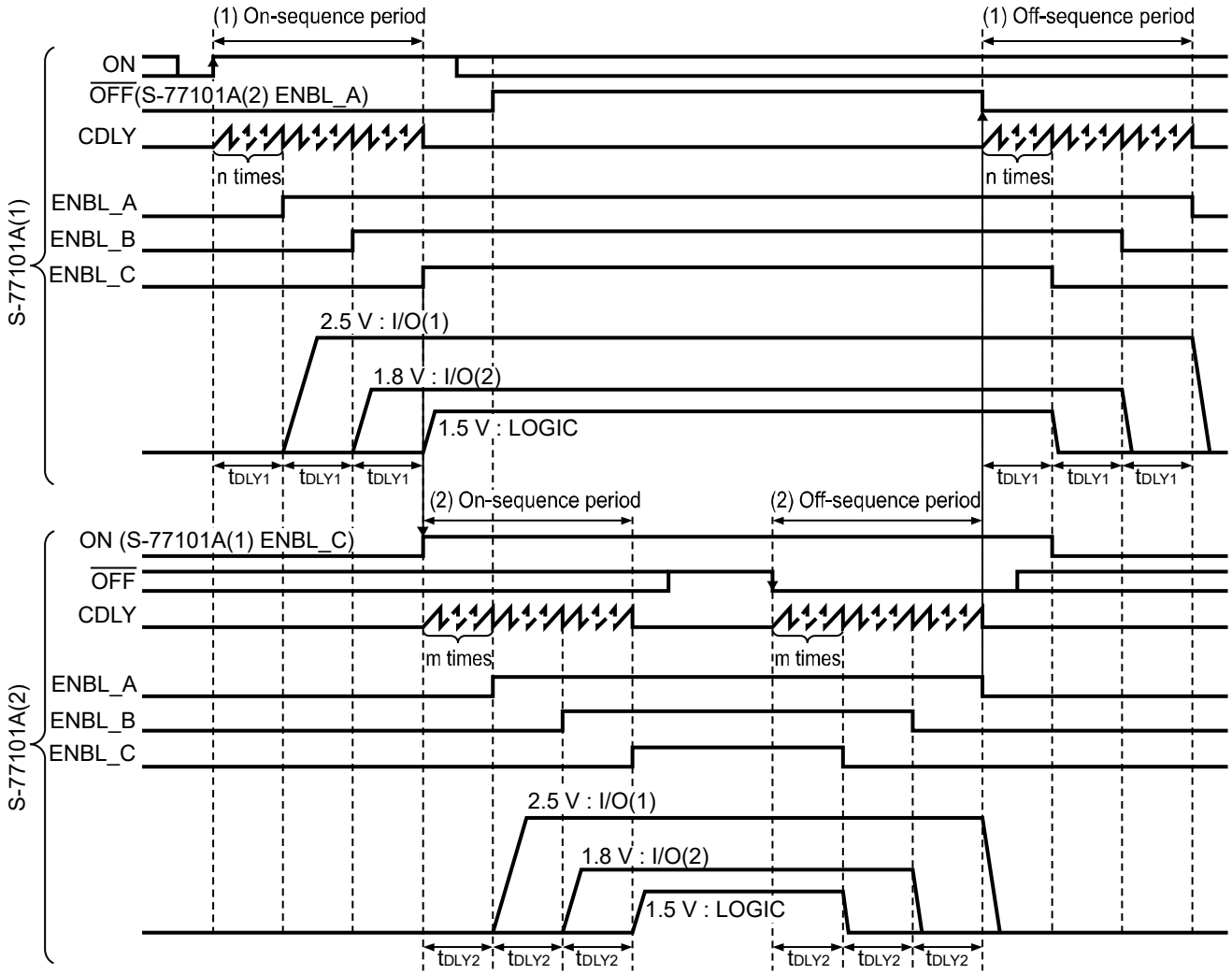


Figure 14 Timing Chart at Cascade Connection (S-77101A: Reverse Type, with $\overline{\text{OFF}}$ pin)

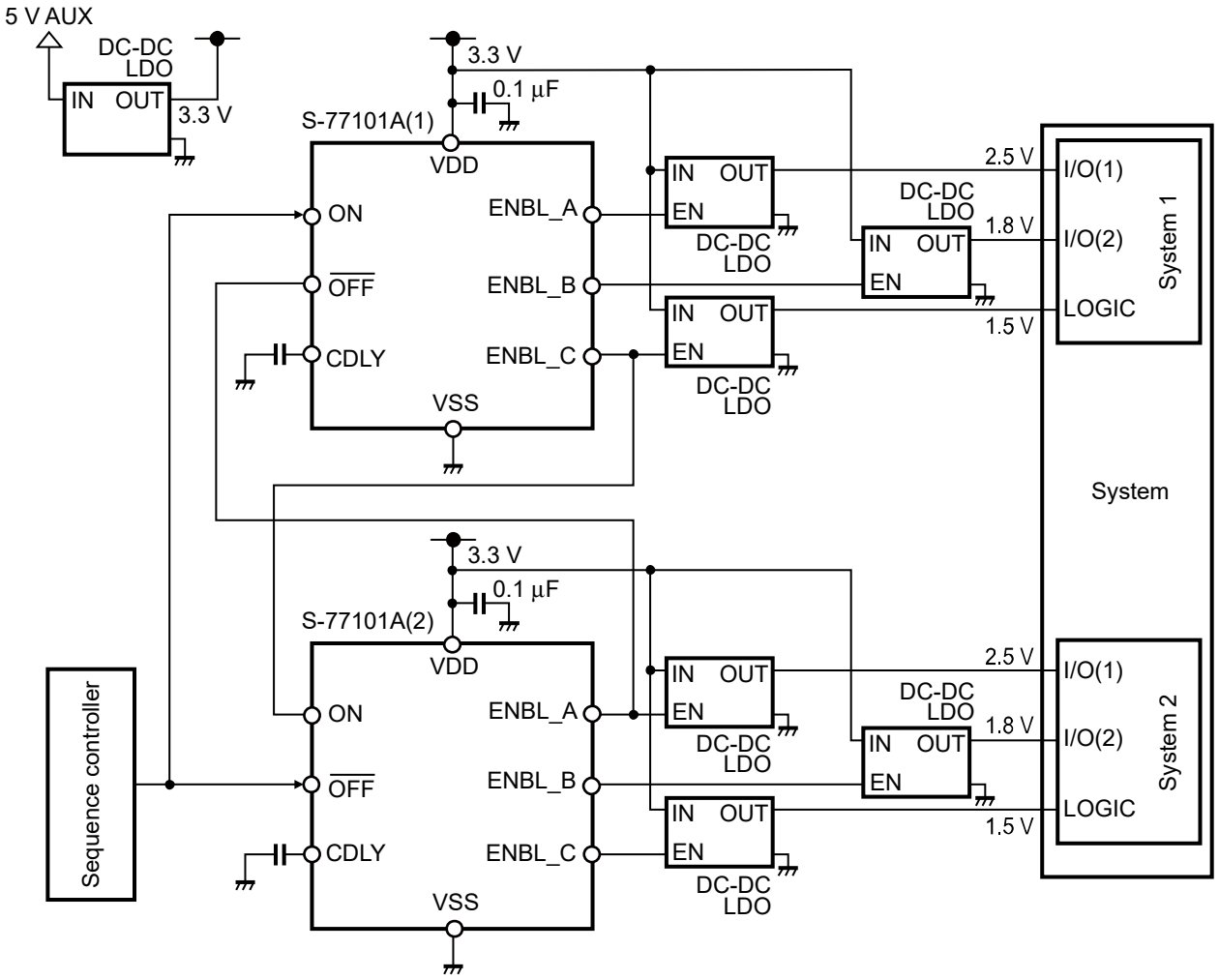
After the ON pin of S-77101A(1) changes from "L" to "H", the ENBL_A pin, the ENBL_B pin and the ENBL_C pin of S-77101A(1) change to "H" in turn.
After the ENBL_C pin of S-77101A(1) changes from "L" to "H", the ENBL_A pin, the ENBL_B pin and the ENBL_C pin of S-77101A(2) change to "H" in turn.

After the $\overline{\text{OFF}}$ pin of S-77101A(2) changes from "H" to "L", the ENBL_C pin, the ENBL_B pin and the ENBL_A pin of S-77101A(2) change to "L" in turn.
After the ENBL_A pin of S-77101A(2) changes from "H" to "L", the ENBL_C pin, the ENBL_B pin and the ENBL_A pin of S-77101A(1) change to "L" in turn.

Do not change the ON pin and the $\overline{\text{OFF}}$ pin during on-sequence period and off-sequence period in order to perform the sequence operation normally.

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As shown in **Figure 14**, after the ON pin of S-77101A(1) changes from "L" to "H", the on-sequence operation is performed if the $\overline{\text{OFF}}$ pin of S-77101A(2) is either "H" or "L". Similarly, after the $\overline{\text{OFF}}$ pin of S-77101A(2) changes from "H" to "L", the off-sequence operation is performed if the ON pin of S-77101A(1) is either "H" or "L". Therefore, due to connecting the control signal pin of the sequence controller, the ON pin of S-77101A(1) and the $\overline{\text{OFF}}$ pin of S-77101A(2), it is possible to control S-77101A(1) and S-77101A(2) with 1 signal.
Figure 15 shows the connection example.



Remark The ENBL_x pin is CMOS output.

Figure 15 Cascade Connection Example (S-77101A: Reverse Type, with $\overline{\text{OFF}}$ pin)

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3. Special Operation

3. 1 S-77100 Series special operation

The Operation when the sequence operation is not completed normally, the power supply voltage drops significantly or connecting the VDD pin and the ON pin is a special operation.

3. 1. 1 Special operations during on-sequence period and off-sequence period

Do not change the ON pin during on-sequence period and off-sequence period in order to perform the sequence operation normally.

(1) When ON pin changes from "H" to "L" during on-sequence period

Since the ENBL_x pins all change to "L", the off-sequence operation timing is not guaranteed. In addition, C_{DLY} charge operation is stopped, and the automatic discharge operation is started. The operation example is shown in **Figure 16**.

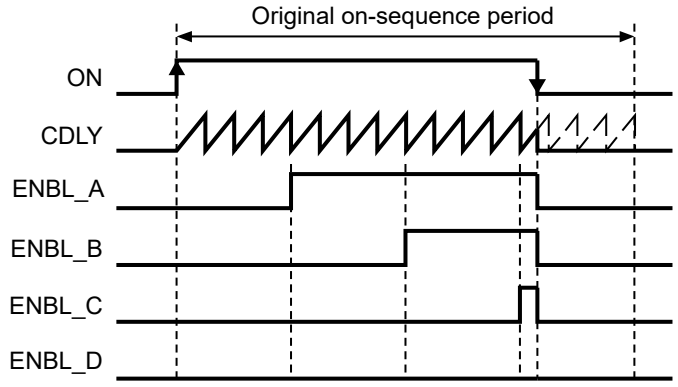


Figure 16

(2) When ON pin changes from "L" to "H" during off-sequence period

Since the ENBL_x pins all change to "L", the off-sequence operation timing is not guaranteed. In addition, C_{DLY} charge operation is stopped and the automatic discharge operation is started. In order to perform the on-sequence operation again, change the ON pin to "H" after setting the pin "L" once. The operation example is shown in **Figure 17**.

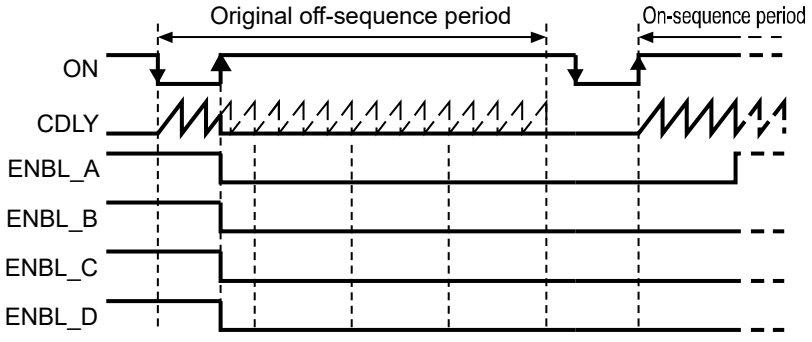


Figure 17

Remark Refer to "**3. Automatic discharge time (t_{DCHG}) approximate calculation formula**" in "**■ Relation between Delay Time and External Capacitor**" for the automatic discharge operation.

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3. 1. 2 Operation when low voltage is detected

(1) When low voltage is detected during power-good period

Since the ENBL_x pins all change to "L" when the power supply voltage (V_{DD}) is equal to or lower than the low voltage detection voltage (V_{UVLO}), the off-sequence operation timing is not guaranteed. Thereafter, if the ON pin is "H" when V_{DD} exceeds V_{UVLO}, the on-sequence operation is performed automatically. If the ON pin is "L" when V_{DD} exceeds V_{UVLO}, the on-sequence operation is not performed. In order to perform the on-sequence operation, set the ON pin to "H" again. The operation example is shown in **Figure 18**.

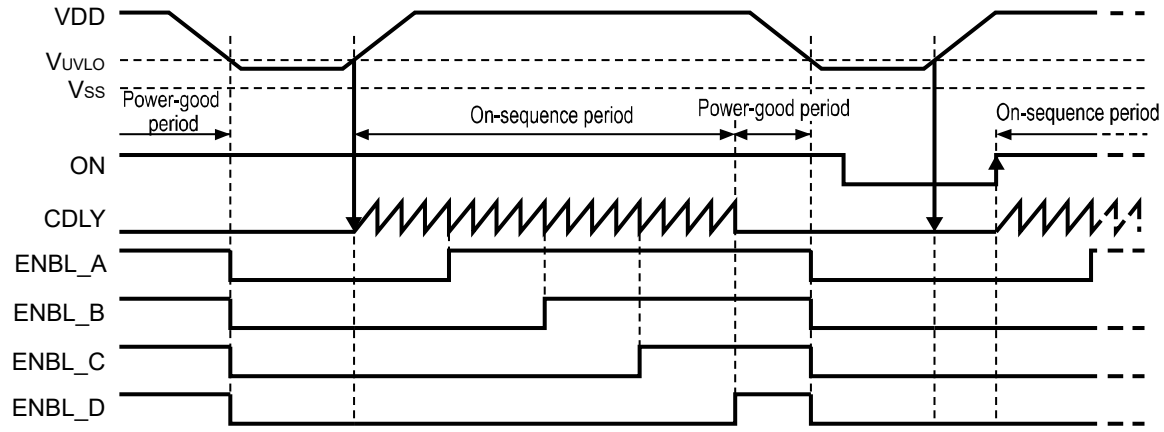


Figure 18

(2) When low voltage is detected during on-sequence period and off-sequence period

Since the ENBL_x pins all change to "L" when V_{DD} is equal to or lower than V_{UVLO} during on-sequence period or off-sequence period, the off-sequence operation timing is not guaranteed. In addition, C_{DLY} charge operation is stopped and the automatic discharge operation is started. The operation example is shown in **Figure 19**.

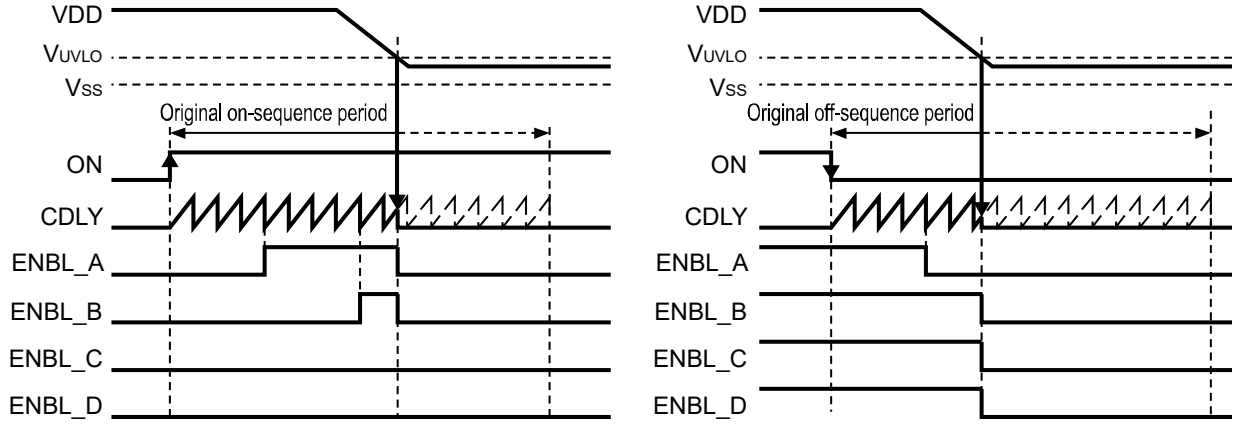


Figure 19

Remark Refer to "**3. Automatic discharge time (t_{DCHG}) approximate calculation formula**" in "**■ Relation between Delay Time and External Capacitor**" for the automatic discharge operation.

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3. 1. 3 Operation when connecting VDD pin and ON pin

The on-sequence operation is performed automatically when connecting the VDD pin and the ON pin and the power supply is raised. However, since the ENBL_x pins all change to "L" if V_{DD} is equal to or lower than V_{UVLO} when the power supply is fallen, the off-sequence operation timing is not guaranteed. The operation example is shown in **Figure 20**.

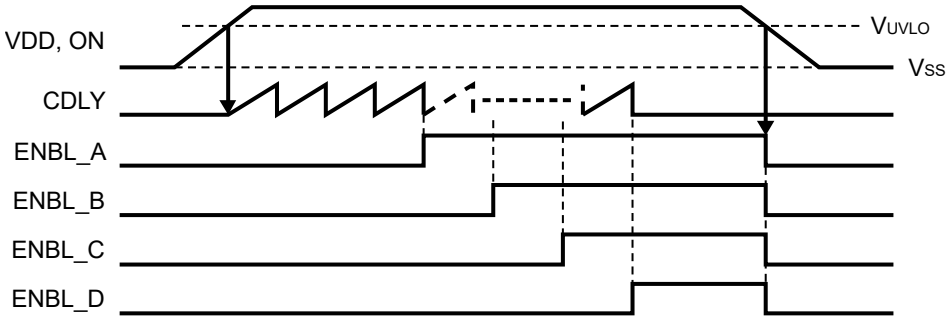


Figure 20

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3. 2 S-77101 Series special operation

The Operation when the sequence operation is not completed normally, the power supply voltage drops significantly or connecting the VDD pin, the ON pin and the $\overline{OFF}$ pin is a special operation.

3. 2. 1 Special operations during on-sequence period and off-sequence period

Do not change the ON pin and the $\overline{OFF}$ pin during on-sequence period and off-sequence period in order to perform the sequence operation normally.

(1) When ON pin or $\overline{OFF}$ pin changes from "H" to "L" during on-sequence period

Since the ENBL_x pins all change to "L" when the ON pin changes from "H" to "L" during on-sequence period, the off-sequence operation timing is not guaranteed. In addition, C_{DLY} charge operation is stopped and the automatic discharge operation is started. When the $\overline{OFF}$ pin changes from "H" to "L" during on-sequence period, the off-sequence operation is performed after the on-sequence operation is completed. The operation example is shown in **Figure 21**.

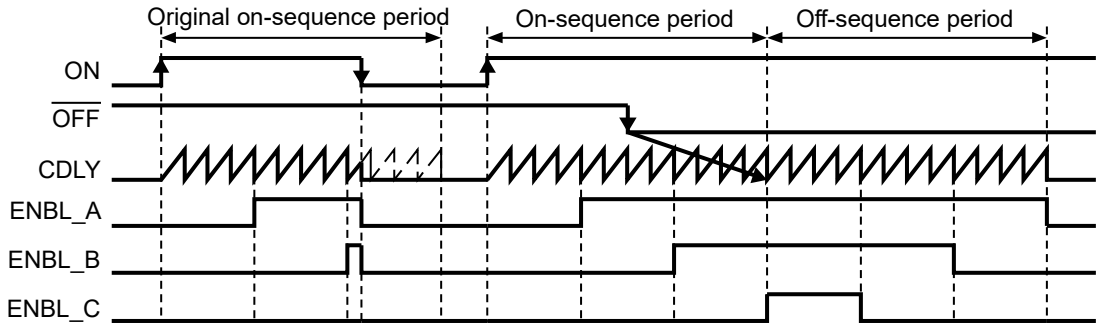


Figure 21

(2) When $\overline{OFF}$ pin or ON pin changes from "L" to "H" during off-sequence period

Since the ENBL_x pins all change to "L" when the $\overline{OFF}$ pin changes from "L" to "H" during off-sequence period, the off-sequence operation timing is not guaranteed. In addition, C_{DLY} charge operation is stopped and the automatic discharge operation is started. When the ON pin changes from "L" to "H" during off-sequence period, the on-sequence operation is performed after the off-sequence operation is completed. The operation example is shown in **Figure 22**.

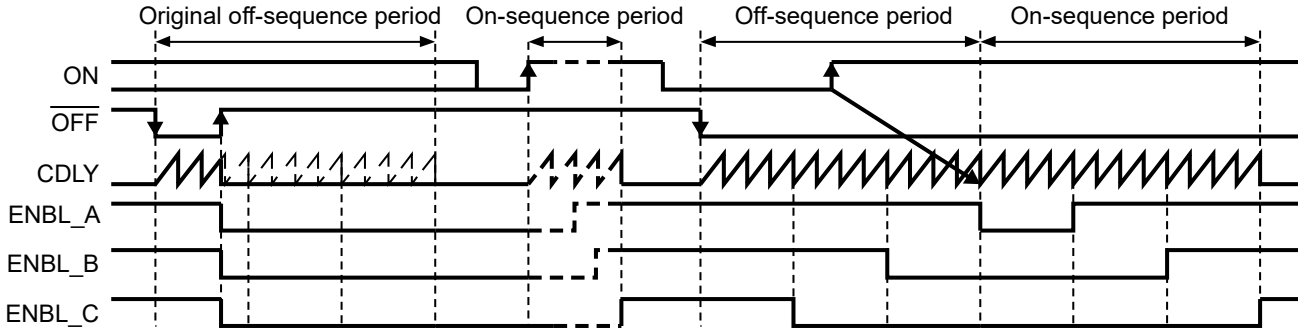


Figure 22

Remark Refer to "**3. Automatic discharge time (t_{DCHG}) approximate calculation formula**" in "**■ Relation between Delay Time and External Capacitor**" for the automatic discharge operation.

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3. 2. 2 Operation when low voltage is detected

(1) When low voltage is detected during power-good period

Since the ENBL_x pins all change to "L" when the power supply voltage (V_{DD}) is equal to or lower than the low voltage detection voltage (V_{UVLO}), the off-sequence operation timing is not guaranteed. Thereafter, if the ON pin is "H" when V_{DD} exceeds V_{UVLO}, the on-sequence operation is performed automatically. If the ON pin is "L" when V_{DD} exceeds V_{UVLO}, the on-sequence operation is not performed. In order to perform the on-sequence operation, set the ON pin to "H" again. The operation example is shown in **Figure 23**.

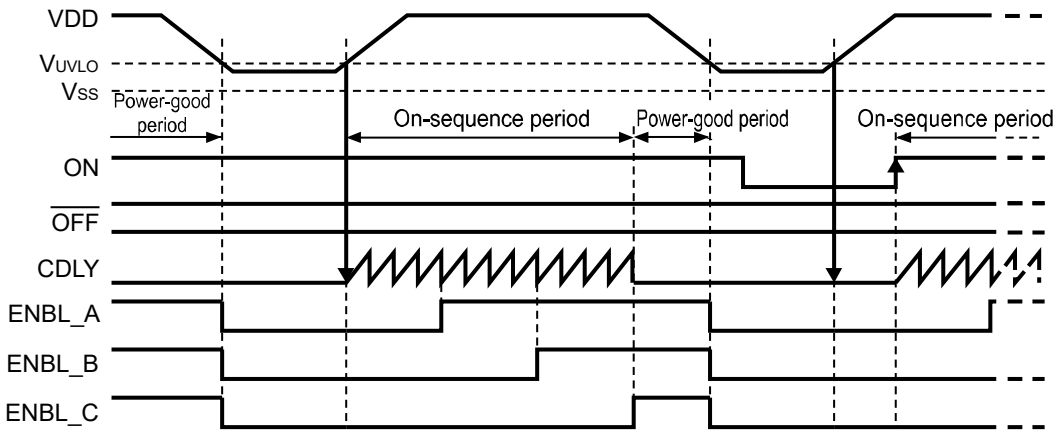


Figure 23

(2) When low voltage is detected during on-sequence period and off-sequence period

Since the ENBL_x pins all change to "L" when V_{DD} is equal to or lower than V_{UVLO} during on-sequence period or off-sequence period, the off-sequence operation timing is not guaranteed. In addition, C_{DLY} charge operation is stopped and the automatic discharge operation is started. The operation example is shown in **Figure 24**.

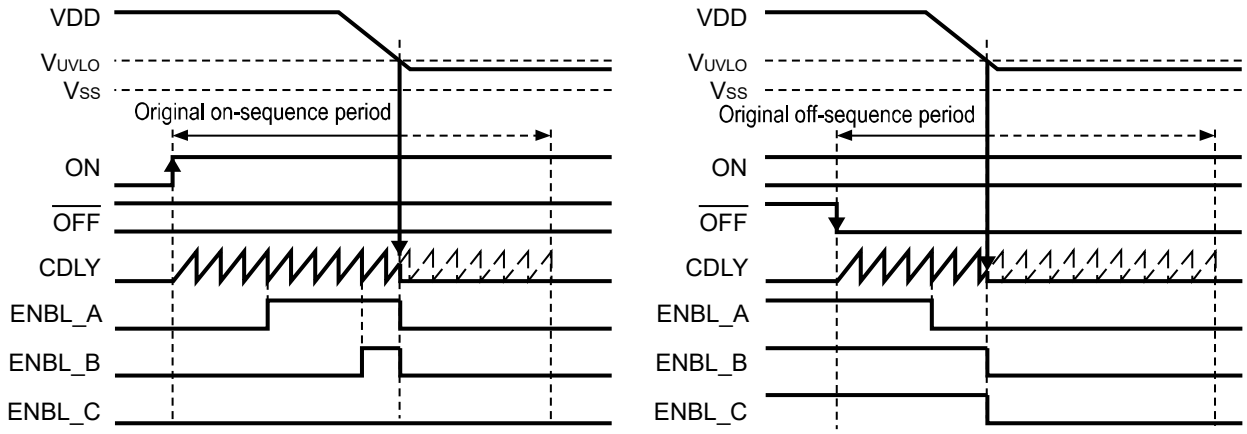


Figure 24

Remark Refer to "**3. Automatic discharge time (t_{DCHG}) approximate calculation formula**" in "**■ Relation between Delay Time and External Capacitor**" for the automatic discharge operation.

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3. 2. 3 Operation when connecting VDD pin, ON pin and $\overline{\text{OFF}}$ pin

The on-sequence operation is performed automatically when connecting the VDD pin, the ON pin and the $\overline{\text{OFF}}$ pin and the power supply is raised. However, since the ENBL_x pins all change to "L" if V_{DD} is equal to or lower than V_{UVLO} when the power supply is fallen, the off-sequence operation timing is not guaranteed. The operation example is shown in **Figure 25**.

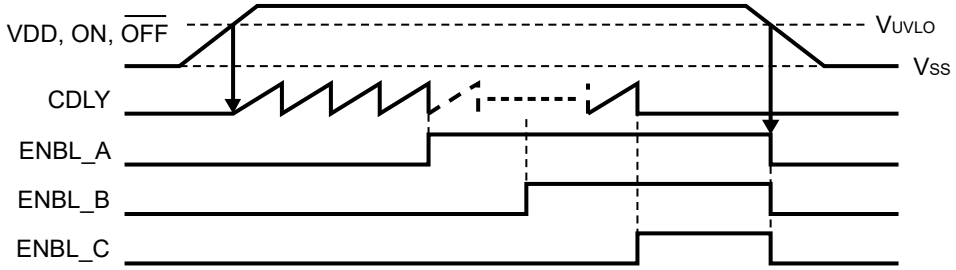


Figure 25

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■ Input of ON Pin and $\overline{\text{OFF}}$ Pin

1. Input level (Selectable as the option)

The input level of the ON pin in the S-77100 Series, the ON pin and the $\overline{\text{OFF}}$ pin in the S-77101 Series can be selected from the following 2 options.

1. 1 Schmitt trigger input

Schmitt trigger input has the power supply voltage dependency in the input voltage level. Refer to "**■ Electrical Characteristics**" for the input voltage.

1. 2 Comparator input

The input threshold voltage of the comparator input has almost no power supply voltage dependency. For this reason, the sequence operation control by I/O interface of the low voltage microcomputer is also available. Refer to "**■ Electrical Characteristics**" for the input threshold voltage of the comparator input.

2. Pulse width

In order to surely input the signal to the S-77100/77101 Series, the pulse width to the ON pin and the $\overline{\text{OFF}}$ pin should be 5 μs or longer.

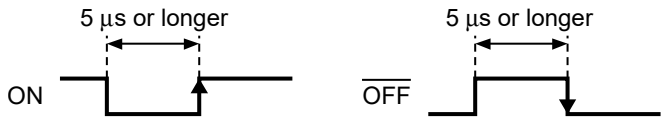


Figure 26

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■ Relation between Delay Time and External Capacitor

The S-77100/77101 Series sets the delay time (t_{DLY}) with an external capacitor (C_{DLY}).
t_{DLY} is generated by performing C_{DLY} charge-discharge operation.

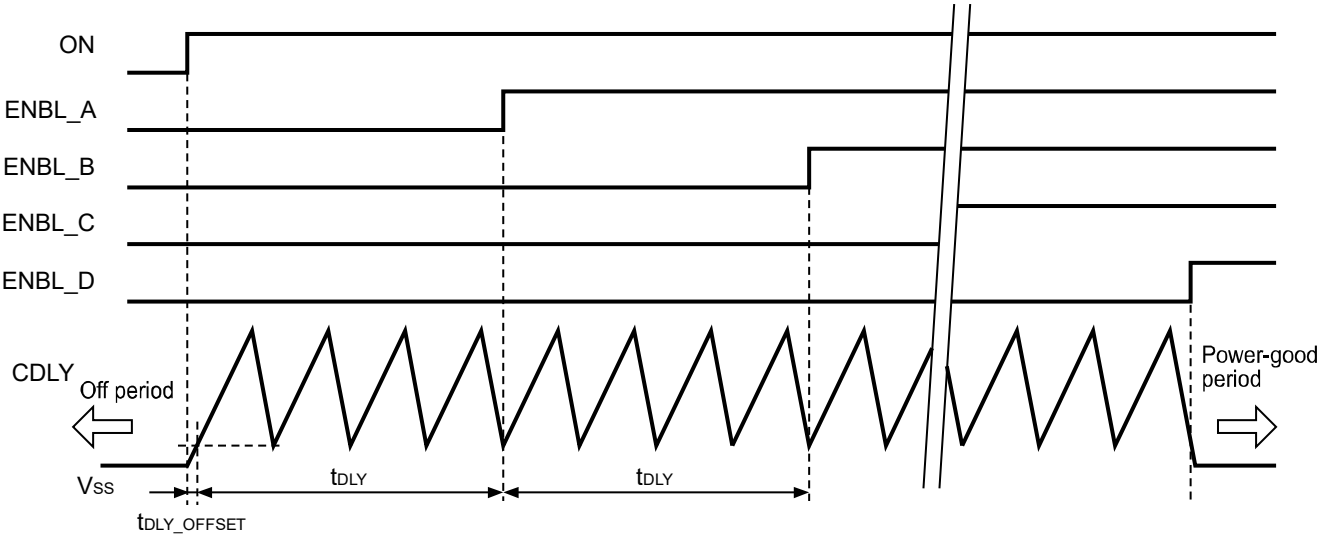


Figure 27

1. t_{DLY} approximate calculation formula

t_{DLY} is calculated by using the following approximate calculation formula.

When $C_{DLY} \leq 1$ nF
t_{DLY} [ms] = (1.206 × C_{DLY} [nF] + 0.023) × the number of times of charge and discharge
When $C_{DLY} > 1$ nF
t_{DLY} [ms] = (1.155 × C_{DLY} [nF] – 0.023) × the number of times of charge and discharge

2. Offset delay time (t_{DLY_OFFSET}) approximate calculation formula

As shown in **Figure 27**, the CDLY pin during off period or power-good period is discharged to the V_{SS} level. For this reason, there is an offset delay time (t_{DLY_OFFSET}) immediately after the transition from off period to on-sequence period or from power-good period to off-sequence period.
t_{DLY_OFFSET} varies depending on the capacitance of C_{DLY}. t_{DLY_OFFSET} is calculated by using the following approximate calculation formula.

When $C_{DLY} \leq 1$ nF
t_{DLY_OFFSET} [ms] = 0.241 × C_{DLY} [nF] – 0.024
When $C_{DLY} > 1$ nF
t_{DLY_OFFSET} [ms] = 0.299 × C_{DLY} [nF] – 0.150

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3. Automatic discharge time (t_{DCHG}) approximate calculation formula

Automatic discharge operation is the operation that electrical charge remained in C_{DLY} is discharged.
After the charge-discharge operation is completed, the automatic discharge operation is performed by the constant current circuit.

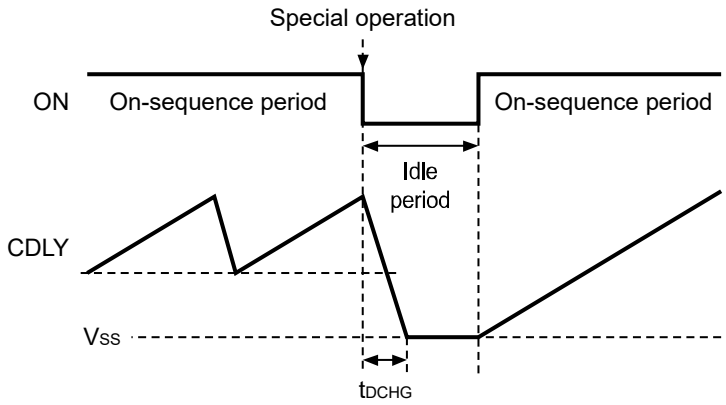


Figure 28

The automatic discharge operation of the S-77100/77101 Series is performed in the following cases.

- When the ON pin changes during on-sequence period. (Refer to **Figure 28**.)
- When on-sequence period is completed.
- When the ON pin changes during off-sequence period. (The S-77100 Series only)
- When the $\overline{OFF}$ pin changes during off-sequence period. (The S-77101 Series only)
- When off-sequence period is completed.
- When V_{DD} is equal to or lower than V_{UVLO} during on-sequence period or off-sequence period.

t_{DCHG} varies depending on the capacitance of C_{DLY} and is calculated by using the following approximate calculation formula.

$$t_{DCHG}\ [ms] = 0.219 \times C_{DLY}\ [nF]$$

The period from when the S-77100/77101 Series starts the automatic discharge operation to when it starts the next on-sequence operation or the off-sequence operation is called "idle period". The idle period should be equal to or longer than t_{DCHG}. The idle period is necessary in order to discharge the electrical charge in C_{DLY} completely and start the next on-sequence operation or off-sequence operation normally.
In addition, by setting power-good period and off period equal to or longer than t_{DCHG} during the sequence operation, the next off-sequence period and the on-sequence period will be the intended length.

Caution 1. The capacitor of 100 pF to 47 nF can be used as C_{DLY}.
C_{DLY} should be placed as close to the S-77100/77101 Series as possible since the CDLY pin internal impedance is high and the pin is easily affected by external noise etc.
2. t_{DLY}, t_{DLY_OFFSET} and t_{DCHG} may not match the calculation formula due to parasitic capacitance of the CDLY pin or internal delay in the IC. Perform thorough evaluation to determine the capacitance of C_{DLY}.

Remark All of the above are approximate calculation formulas at Ta = +25°C.

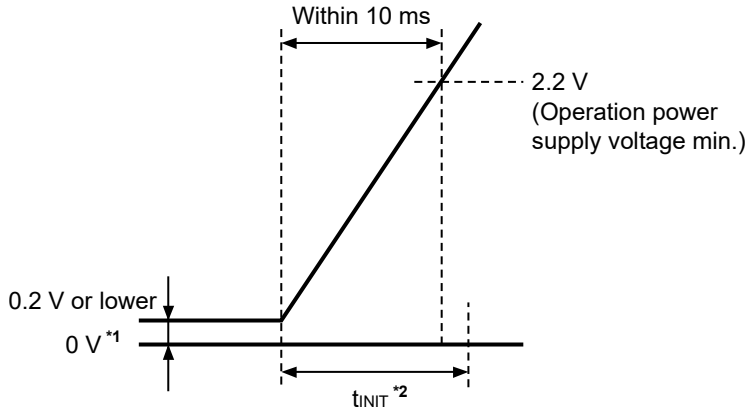
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■ Power-on

When the power supply is raised, the S-77100/77101 Series performs initialization due to the power-on reset circuit. If initialization is not performed normally, a malfunction may occur. In order to operate the power-on reset circuit normally, raise the power supply with the following method.

1. Power supply raising method

As shown in **Figure 29**, start to raise the power supply from 0.2 V or lower. Moreover, the time the voltage reaches to the operation power supply voltage min. should be within 10 ms.



***1.** 0 V indicates that there is no potential difference between the VDD pin and the VSS pin of the S-77100/77101 Series.

***2.** Initialization time (t_{INIT}) indicates the time that the S-77100/77101 Series performs the initialization internally. During this duration, the S-77100/77101 Series does not accept the input. Refer to "**2. Initialization time**" for the details.

Figure 29

If initialization is completed normally due to the power-on reset circuit, the S-77100/77101 Series becomes off period when the ON pin is "L", and on-sequence period when the ON pin is "H". When the operation conditions of the power-on reset circuit are not satisfied, a malfunction may occur since the S-77100/77101 Series cannot perform initialization. When the operation is unstable, raise the power supply voltage again so as to satisfy the condition of **Figure 29** after lowering the power supply voltage to the V_{SS} level.

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2. Initialization time

When the power supply is raised, the S-77100/77101 Series performs initialization. During initialization period, the S-77100/77101 Series does not accept the inputs to the ON pin and the $\overline{\text{OFF}}$ pin. The relation between the initialization time (t_{INIT}) and the power supply rising (0 V $\rightarrow$ 2.2 V) time (t_{RISE}) is shown in **Figure 30**.

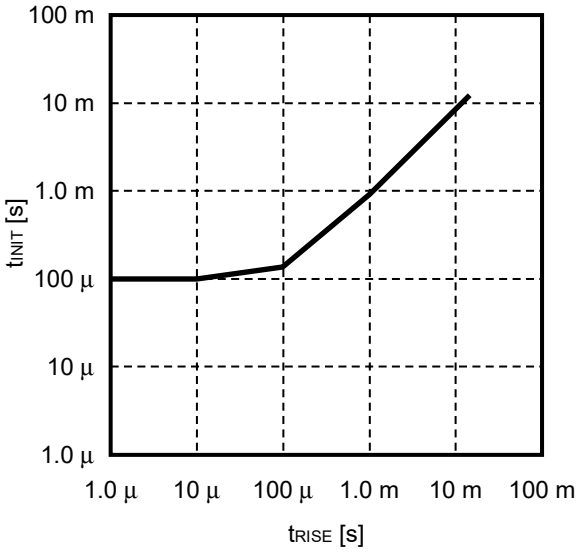


Figure 30

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■ UVLO (under voltage lock out) Operation

The power supply voltage range and the output pin status are shown in **Figure 31**.

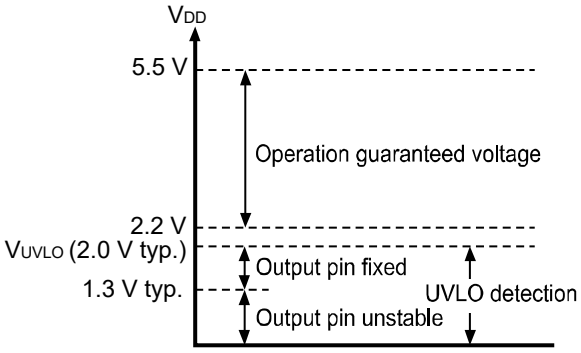


Figure 31

In the S-77100/77101 Series, the output pin status is not guaranteed when the power supply voltage (V_{DD}) is equal to or lower than 1.3 V typ. The output pin status is fixed when V_{DD} rises and exceeds 1.3 V typ.
The sequence operation is invalid when V_{DD} is equal to or lower than V_{UVLO}. V_{DD} is operation voltage when it exceeds V_{UVLO}, however, the operation guaranteed voltage as the power sequencer is 2.2 V to 5.5 V.

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■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

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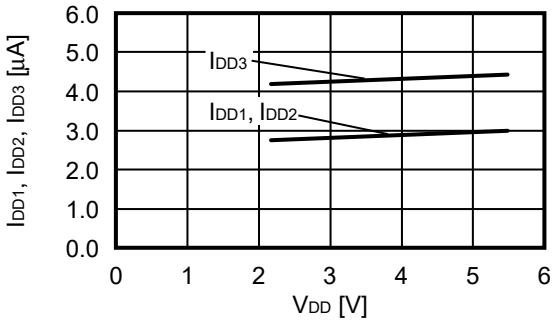
■ Characteristics (Typical Data)

1. Current consumption 1, current consumption 2, current consumption 3

1. 1 Current consumption vs. Power supply voltage

S-77100 Series

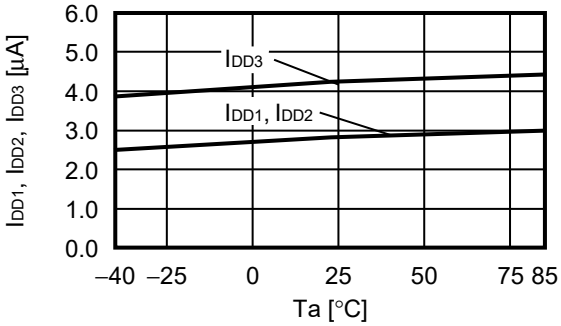
ON pin = V_{SS} or V_{DD}, ENBL_x pin = Open
Schmitt trigger input, Ta = +25°C



1. 2 Current consumption vs. Temperature

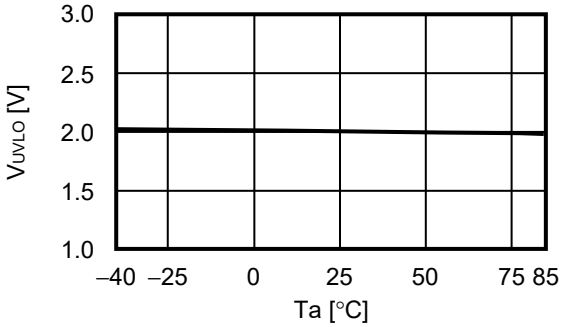
S-77100 Series

ON pin = V_{SS} or V_{DD}, ENBL_x pin = Open
Schmitt trigger input, V_{DD} = 3.3 V



2. Low voltage detection voltage

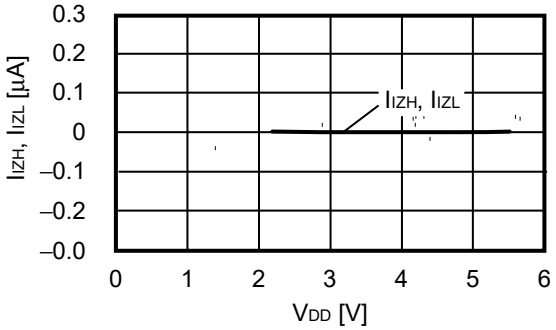
2. 1 Low voltage detection voltage vs. Temperature



3. High level input leakage current, low level input leakage current

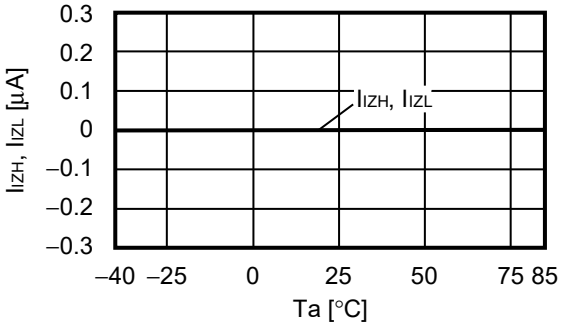
3. 1 Input leakage current vs. Power supply voltage

ON pin, $\overline{OFF}$ pin*1, V_{IN} = V_{DD} (I_{IZH}), V_{IN} = V_{SS} (I_{IZL})
Ta = +25°C



3. 2 Input leakage current vs. Temperature

ON pin, $\overline{OFF}$ pin*1, V_{IN} = V_{DD} (I_{IZH}), V_{IN} = V_{SS} (I_{IZL})
V_{DD} = 3.3 V

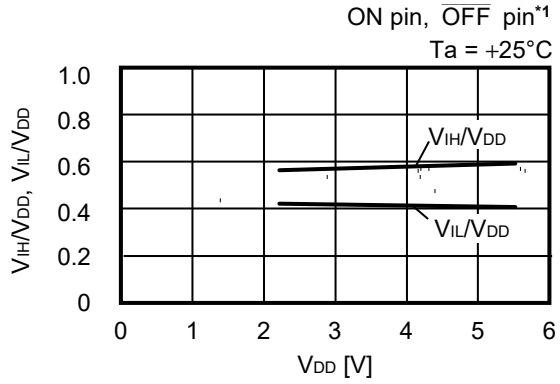


***1.** The S-77101 Series only

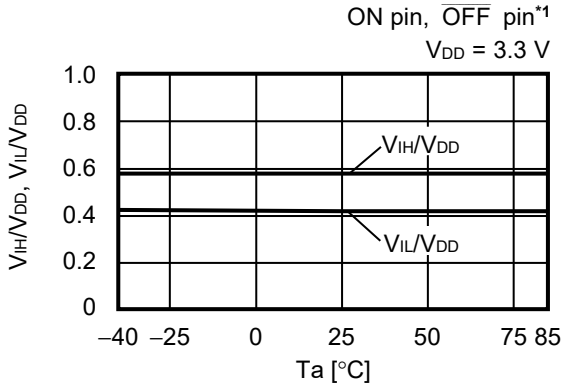
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4. Input voltage (When Schmitt trigger input is selected)

4. 1 Input voltage vs. Power supply voltage

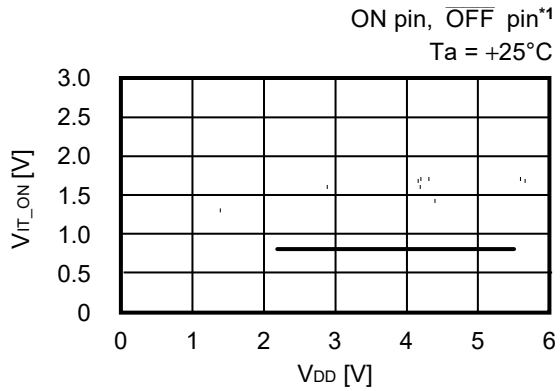


4. 2 Input voltage vs. Temperature

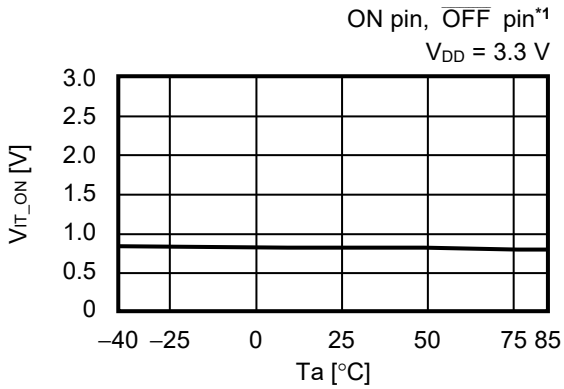


5. Input threshold voltage (When comparator input is selected)

5. 1 Input threshold voltage vs. Power supply voltage

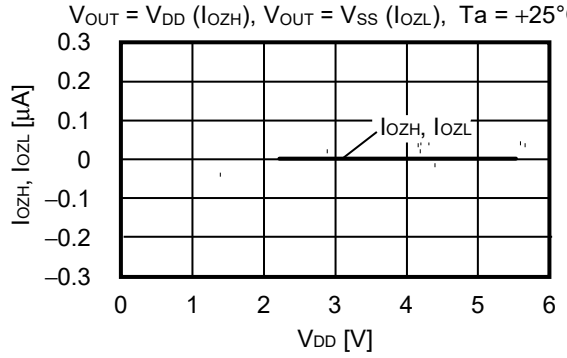


5. 2 Input threshold voltage vs. Temperature

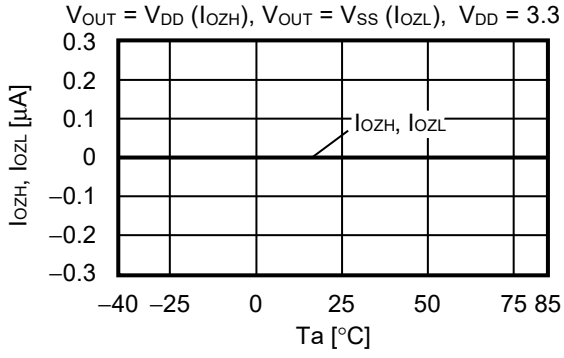


6. High level output leakage current, low level output leakage current

6. 1 Output leakage current vs. Power supply voltage



6. 2 Output leakage current vs. Temperature



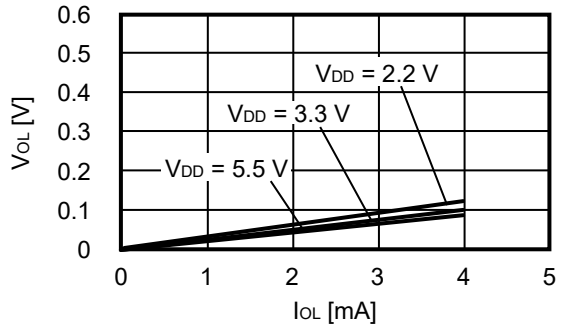
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7. Low level output voltage

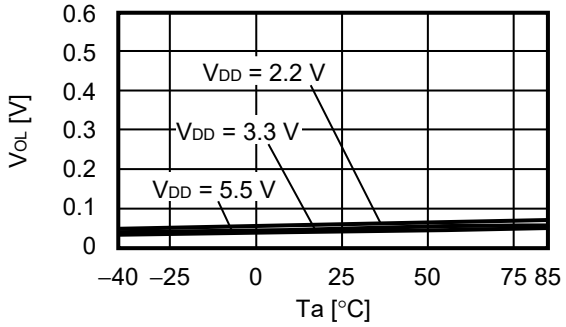
7. 1 Low level output voltage vs. Low level output current

ENBL_A pin, ENBL_B pin, ENBL_C pin, ENBL_D pin*1
Ta = +25°C



7. 2 Low level output voltage vs. Temperature

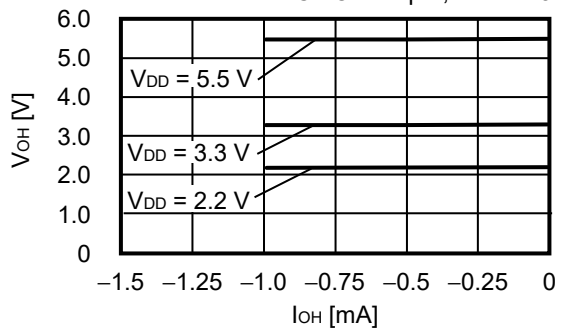
ENBL_A pin, ENBL_B pin, ENBL_C pin, ENBL_D pin*1
IOL = 2.0 mA



8. High level output voltage

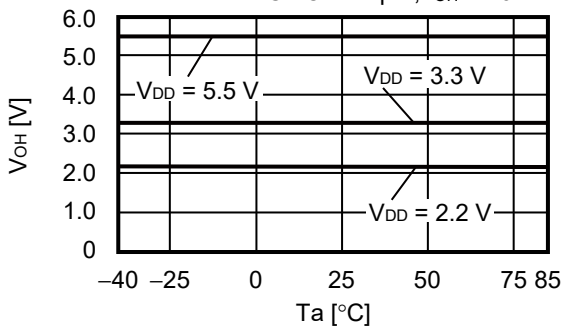
8. 1 High level output voltage vs. High level output current

ENBL_A pin, ENBL_B pin, ENBL_C pin, ENBL_D pin*1
CMOS output, Ta = +25°C



8. 2 High level output voltage vs. Temperature

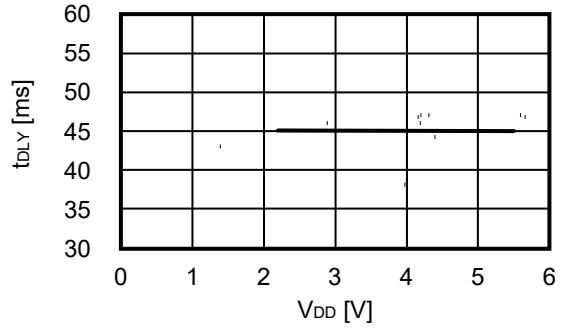
ENBL_A pin, ENBL_B pin, ENBL_C pin, ENBL_D pin*1
CMOS output, IOH = –0.4 mA



9. Delay time

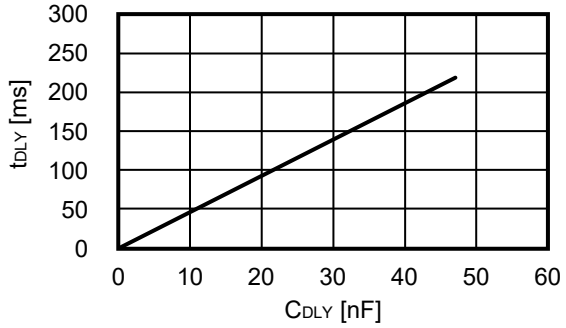
9. 1 Delay time vs. Power supply voltage

The number of times of C_{DLY} charge and discharge = 4 times,
C_{DLY} = 10 nF, Ta = +25°C



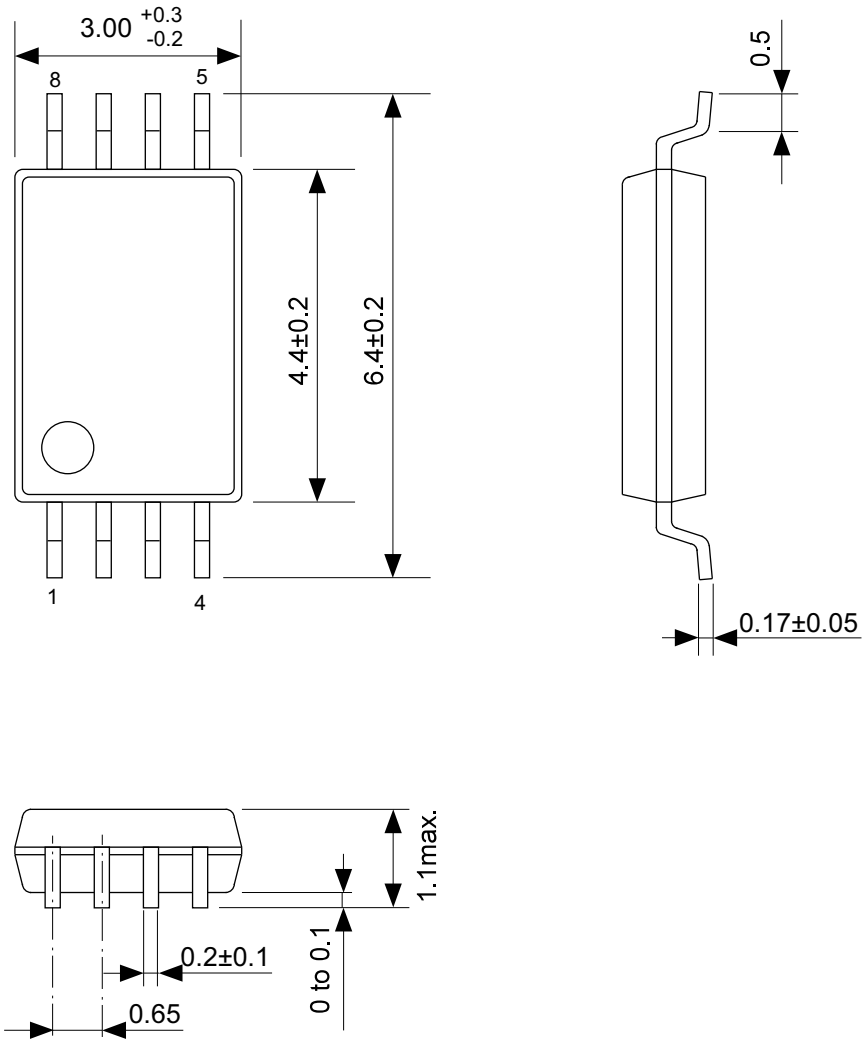
9. 2 Delay time vs. C_{DLY}

The number of times of C_{DLY} charge and discharge = 4 times,
V_{DD} = 3.3 V, Ta = +25°C



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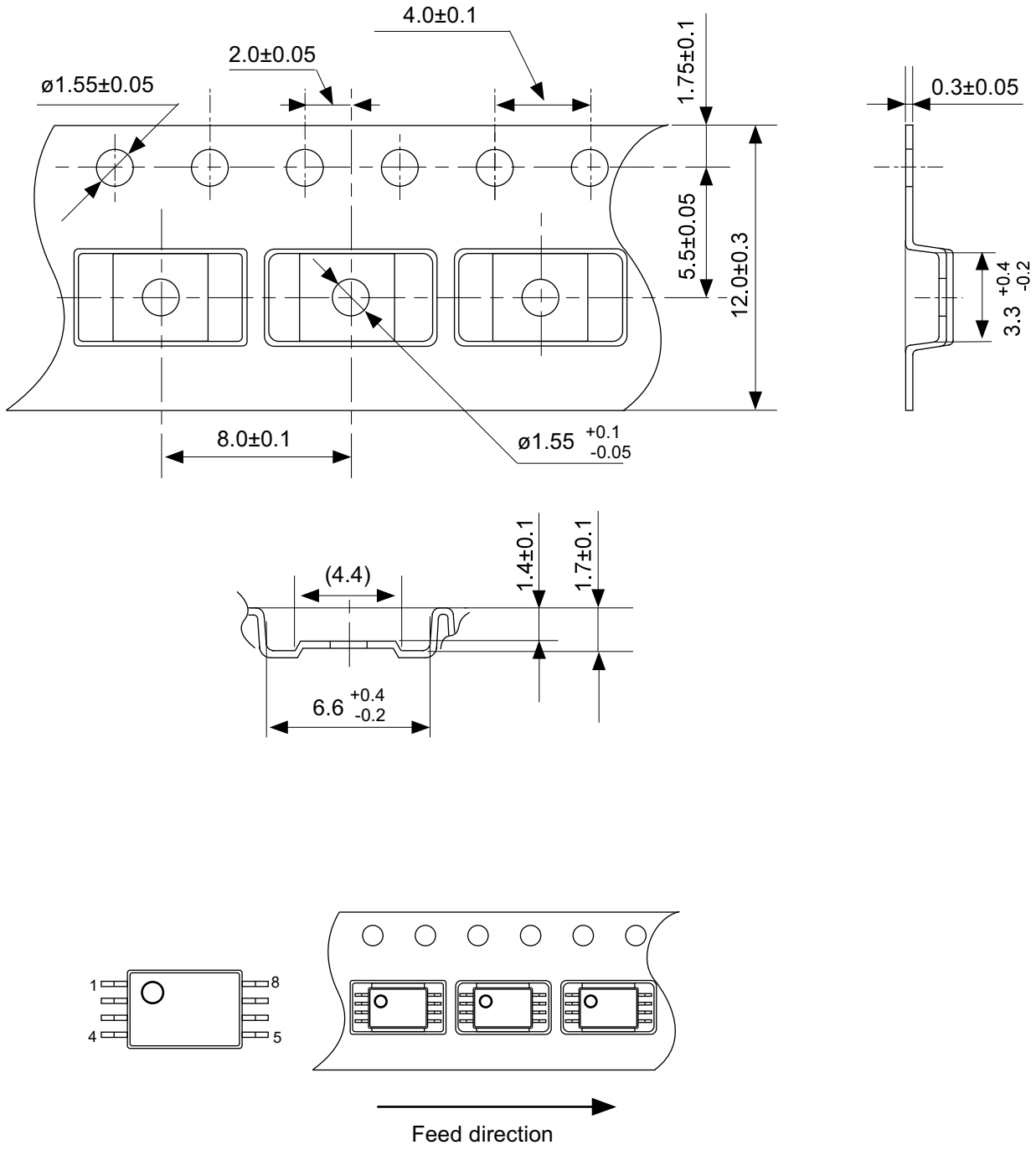


No. FT008-A-P-SD-1.2

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.2
ANGLE	
UNIT	mm

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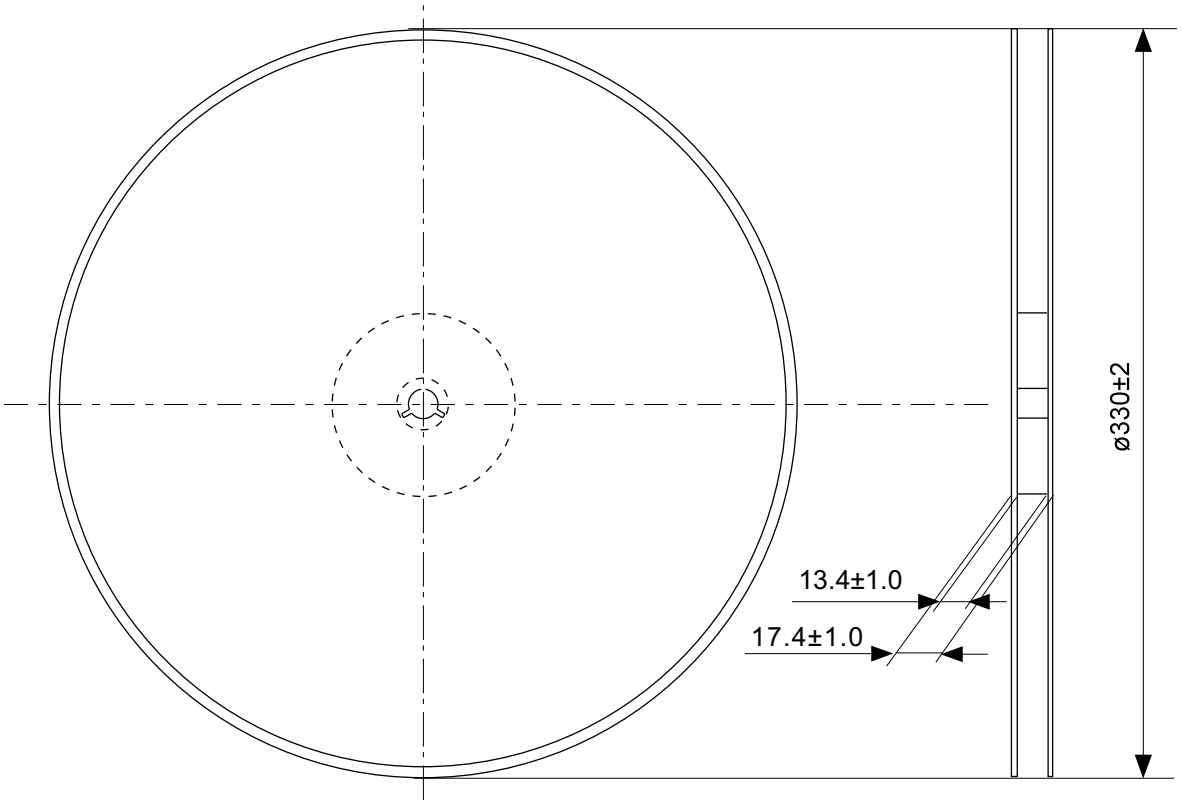
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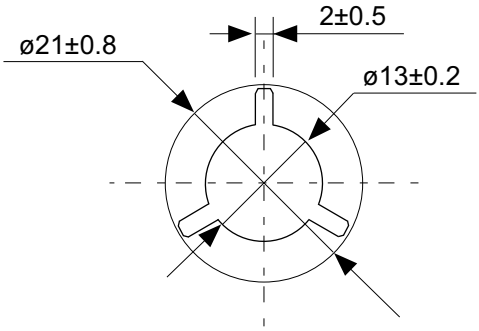
No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
ANGLE	
UNIT	mm
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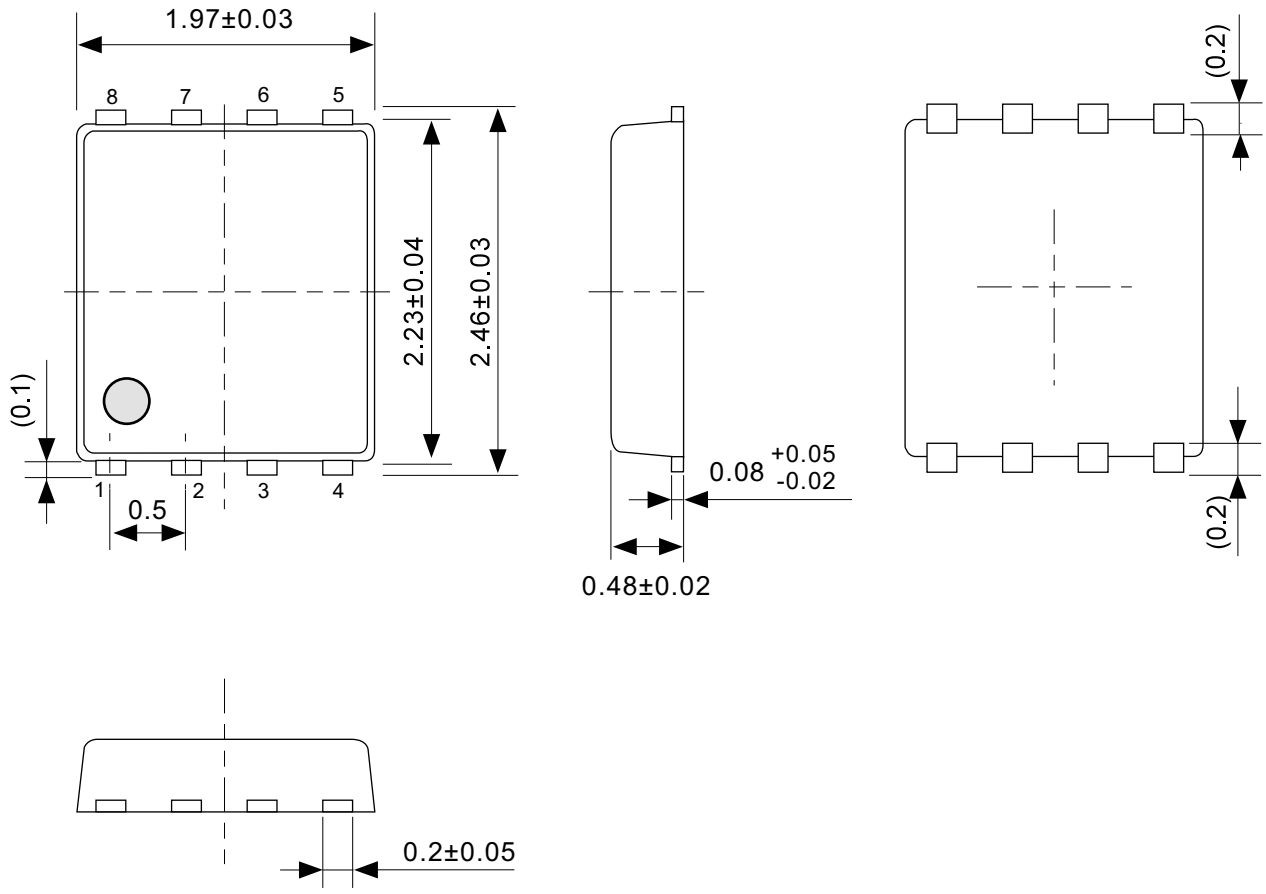
Enlarged drawing in the central part



No. FT008-E-R-S1-2.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-S1-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

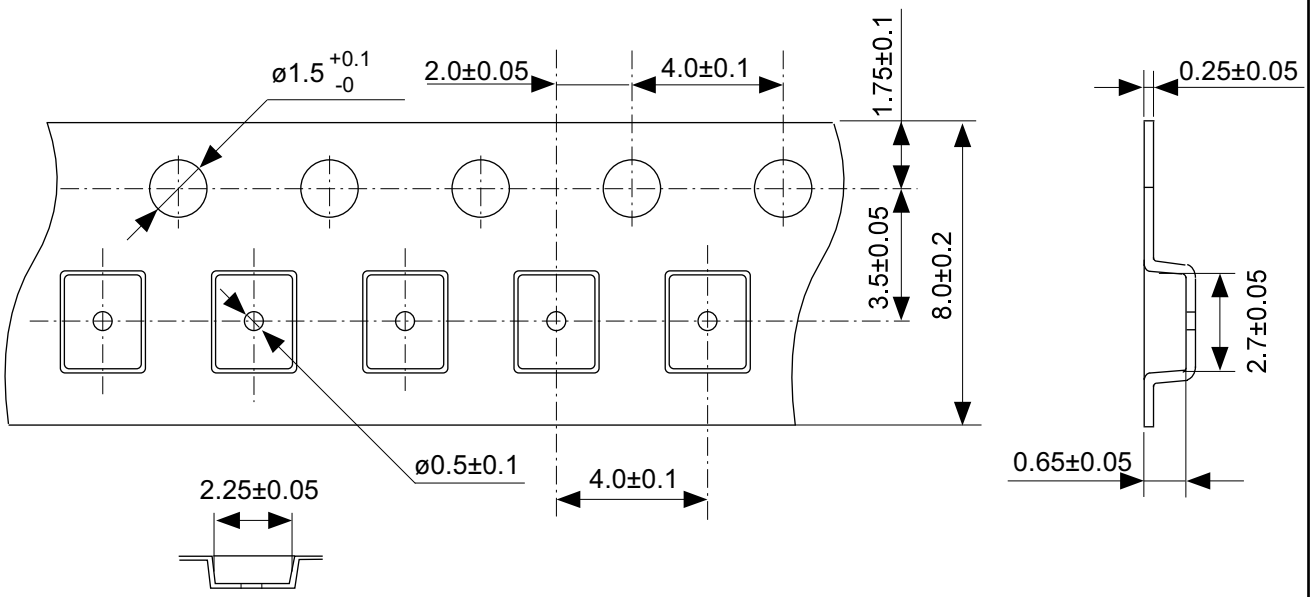
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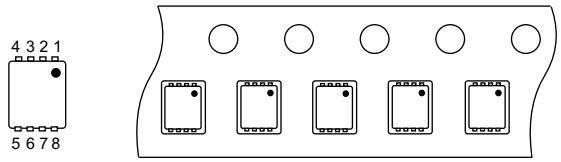


No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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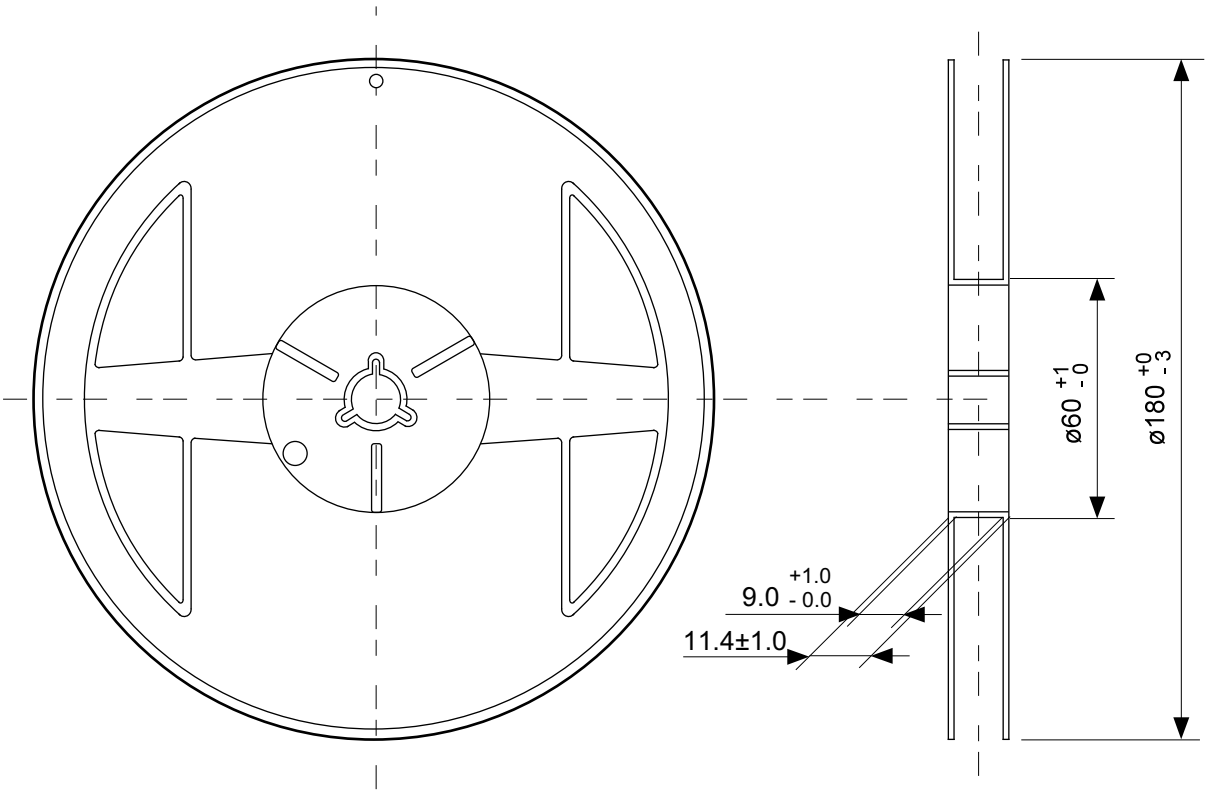


Feed direction

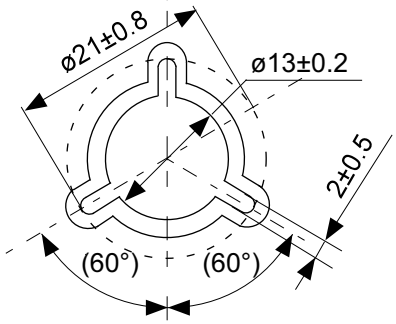
No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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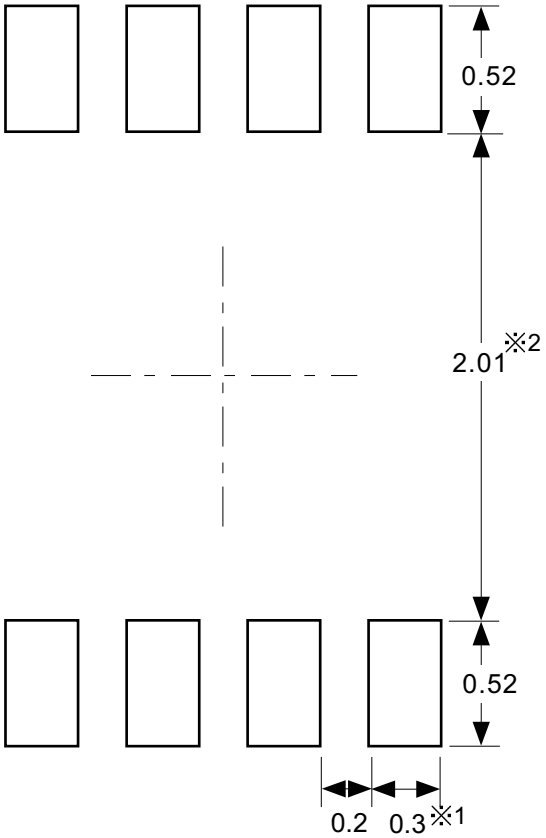
Enlarged drawing in the central part



No. PH008-A-R-SD-2.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

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※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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