CY7C1011CV33

2-Mbit (128 K × 16) Static RAM

Features

- Temperature ranges
  - Industrial: –40 °C to 85 °C
  - Automotive-A: –40 °C to 85 °C
  - Automotive-E: –40 °C to 125 °C
- Pin and function compatible with CY7C1011BV33
- High speed
  - t_{AA} = 10 ns (Industrial and Automotive-A)
  - t_{AA} = 12 ns (Automotive-E)
- Low active power
  - 360 mW (max) (Industrial and Automotive-A)
- 2.0 V data retention
- Automatic power down when deselected
- Independent control of upper and lower bits
- Easy memory expansion with Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) features
- Available in Pb-free 44-pin thin small outline package (TSOP) II, 44-pin thin quad flat package (TQFP), and non Pb-free 48-ball very fine-pitch ball grid array (VFBGA) packages

Functional Description

The CY7C1011CV33 is a high performance complementary metal oxide semiconductor (CMOS) static RAM organized as 131,072 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

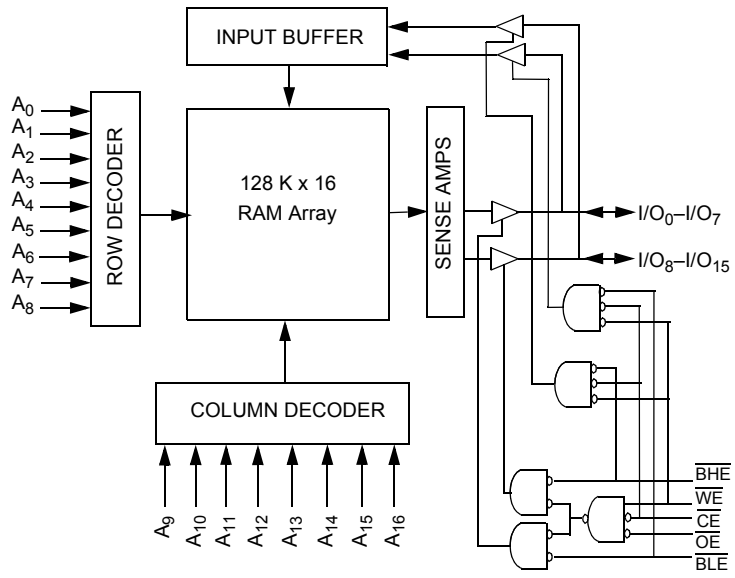
To write to the device, take $\overline{CE}$ and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

To read from the device, take $\overline{CE}$ and $\overline{OE}$ LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If $\overline{BLE}$ is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. For more information, see the Truth Table on page 11 for a complete description of Read and Write modes.

The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

For a complete list of related documentation, click here.

Logic Block Diagram



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Contents

Pin Configuration **3**
Selection Guide **4**
Maximum Ratings **5**
Operating Range **5**
Electrical Characteristics **5**
Capacitance **6**
Thermal Resistance **6**
AC Test Loads and Waveforms **6**
Switching Characteristics **7**
Switching Waveforms **8**
Truth Table **11**
Ordering Information **12**
Ordering Code Definitions 12
Package Diagrams **13**
Acronyms **15**
Document Conventions **15**
Units of Measure 15
Document History Page **16**
Sales, Solutions, and Legal Information **18**
Worldwide Sales and Design Support 18
Products 18
PSoC® Solutions 18
Cypress Developer Community 18
Technical Support 18

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Pin Configuration

Figure 1. 44-pin TSOP II pinout [1]

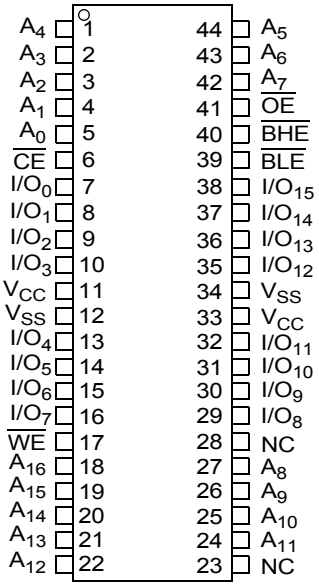
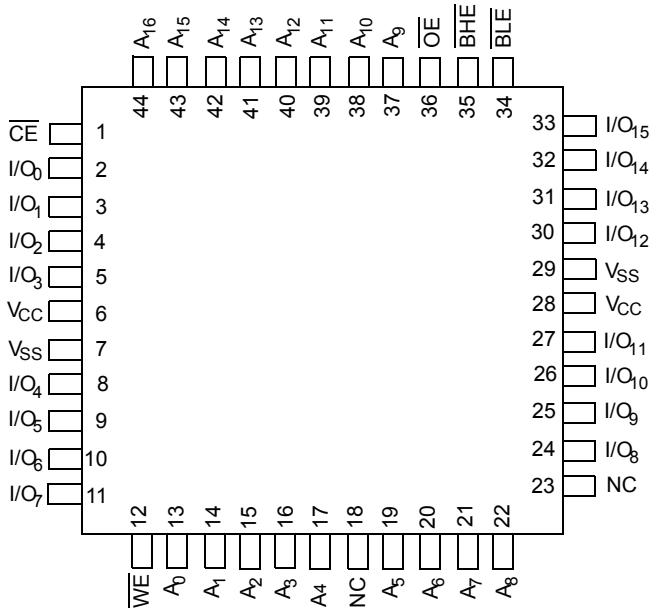


Figure 2. 44-pin TQFP pinout



Note
1. NC pins are not connected on the die.

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Selection Guide

Description		-10	-12	Unit
Maximum access time		10	12	ns
Maximum operating current	Industrial	100	95	mA
	Automotive-A	100	–	mA
	Automotive-E	–	120	mA
Maximum CMOS standby current	Industrial	10	10	mA
	Automotive-A	10	–	mA
	Automotive-E	–	15	mA

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Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND [2] .....–0.5 V to +4.6 V

DC voltage applied to outputs in High Z state [2] .....–0.5 V to V_{CC}+ 0.5 V

DC input voltage [2] .....–0.5 V to V_{CC}+ 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch up current ..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	–40 °C to +85 °C	3.3 V ± 10%
Automotive-A	–40 °C to +85 °C	
Automotive -E	–40 °C to +125 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		Unit
				Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA		–	0.4	–	0.4	V
V_{IH}	Input HIGH voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage[2]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}	Industrial	–1	+1	–1	+1	µA
			Automotive-A	–1	+1	–	–	
			Automotive-E	–	–	–20	+20	
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{CC}, Output disabled	Industrial	–1	+1	–1	+1	µA
			Automotive-A	–1	+1	–	–	
			Automotive-E	–	–	–20	+20	
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Industrial	–	100	–	95	mA
			Automotive-A	–	100	–	–	
			Automotive-E	–	–	–	120	
I_{SB1}	Automatic CE power down current – TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Industrial	–	40	–	40	mA
			Automotive-A	–	40	–	–	
			Automotive-E	–	–	–	45	
I_{SB2}	Automatic CE power down current – CMOS inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	Industrial	–	10	–	10	mA
			Automotive-A	–	10	–	–	
			Automotive-E	–	–	–	15	

Note
2. V_{IL} (min) = –2.0 V for pulse durations of less than 20 ns.

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Capacitance

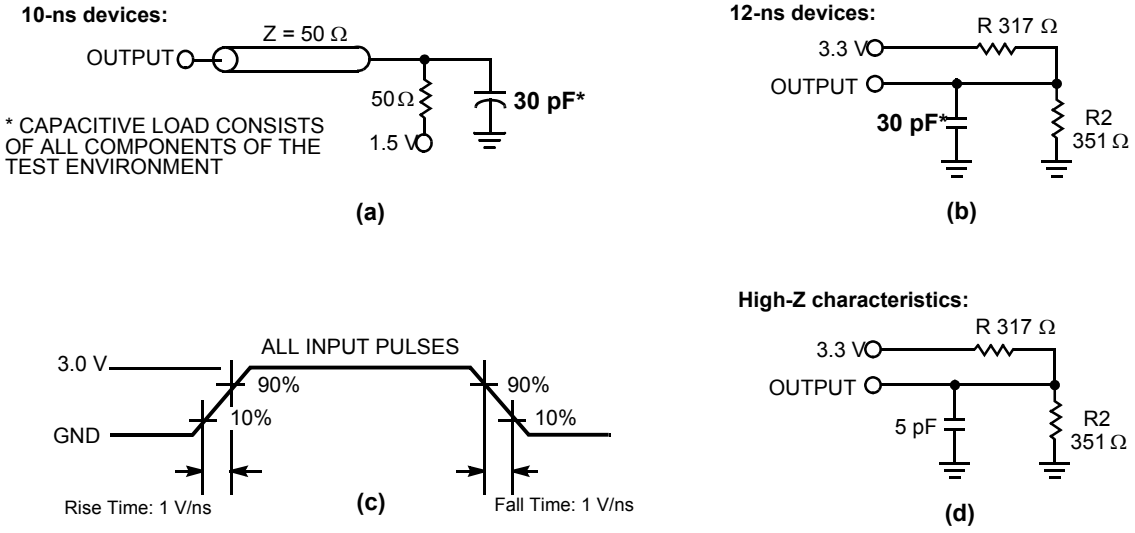
Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter [3]	Description	Test Conditions	44-pin TSOP II	44-pin TQFP	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	44.56	42.66	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		10.75	14.64	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [4]



Notes

3. Tested initially and after any design or process changes that may affect these parameters.
4. AC characteristics (except High Z) for 10-ns parts are tested using the load conditions shown in Figure 3 (a). All other speeds are tested using the Thevenin load shown in Figure 3 (b). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (d).

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Switching Characteristics

Over the Operating Range

Parameter [5]	Description		-10		-12		Unit
			Min	Max	Min	Max	
Read Cycle							
t_{power}[6]	V_{CC} (typical) to the first access		1	–	1	–	µs
t_{RC}	Read cycle time		10	–	12	–	ns
t_{AA}	Address to data valid		–	10	–	12	ns
t_{OHA}	Data hold from address change		3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid		–	10	–	12	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	Industrial/Automotive-A	–	5	–	6	ns
		Automotive-E	–	–	–	8	
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]		0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		–	5	–	6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]		3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		–	5	–	6	ns
t_{PU}	$\overline{CE}$ LOW to power up		0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down		–	10	–	12	ns
t_{DBE}	Byte enable to data valid	Industrial/Automotive-A	–	5	–	6	ns
		Automotive-E	–	–	–	8	
t_{LZBE}	Byte enable to Low Z		0	–	0	–	ns
t_{HZBE}	Byte disable to High Z		–	5	–	6	ns
Write Cycle [9, 10]							
t_{WC}	Write cycle time		10	–	12	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end		7	–	8	–	ns
t_{AW}	Address setup to write end		7	–	8	–	ns
t_{HA}	Address hold from write end		0	–	0	–	ns
t_{SA}	Address setup to write start		0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width		7	–	8	–	ns
t_{SD}	Data setup to write end		5	–	6	–	ns
t_{HD}	Data hold from write end		0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]		3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		–	5	–	6	ns
t_{BW}	Byte enable to end of write		7	–	8	–	ns

Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
6. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
7. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
8. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of Figure 3 on page 6. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW, and $\overline{BHE}$/$\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$, and $\overline{BHE}$/$\overline{BLE}$ must be LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

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Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [11, 12]

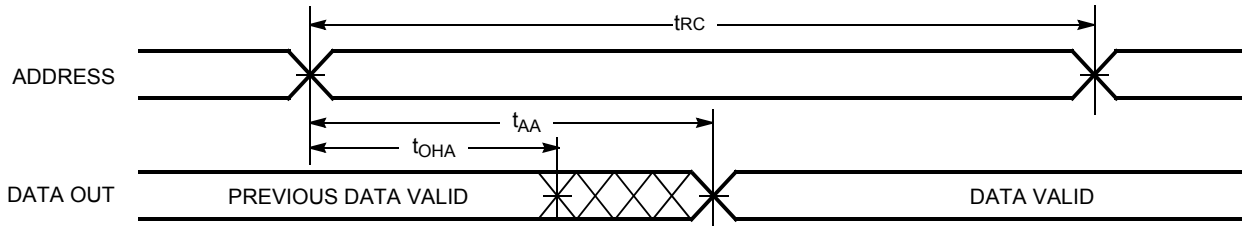
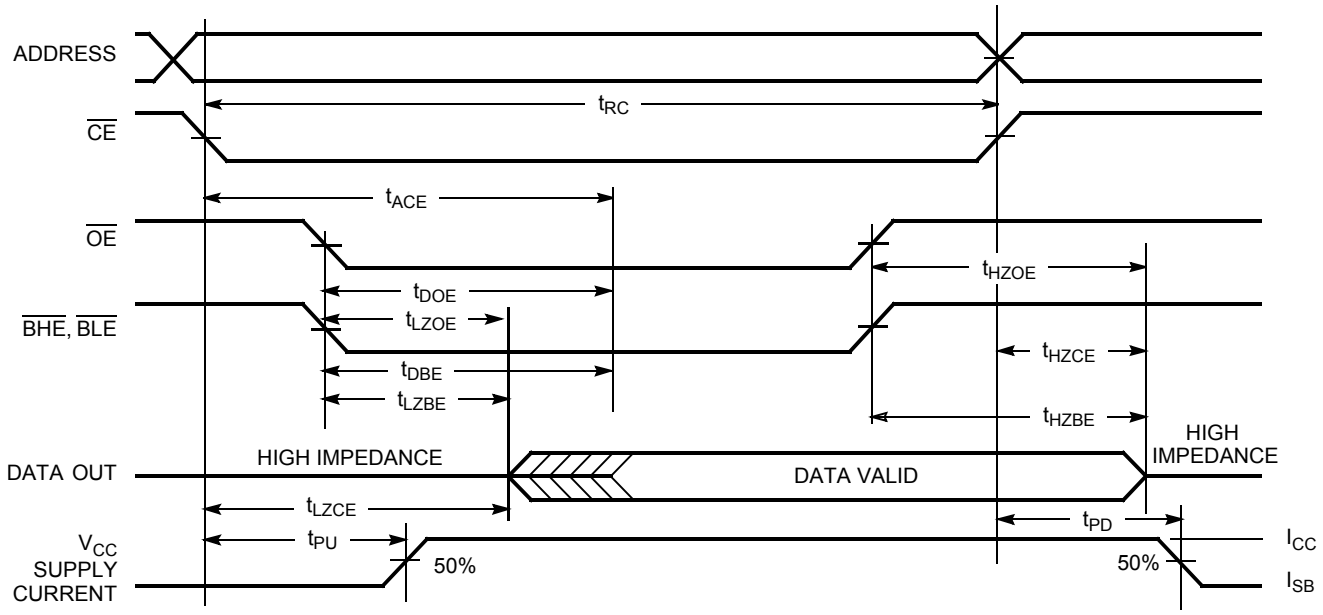


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [12, 13]



Notes
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

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Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [14, 15]

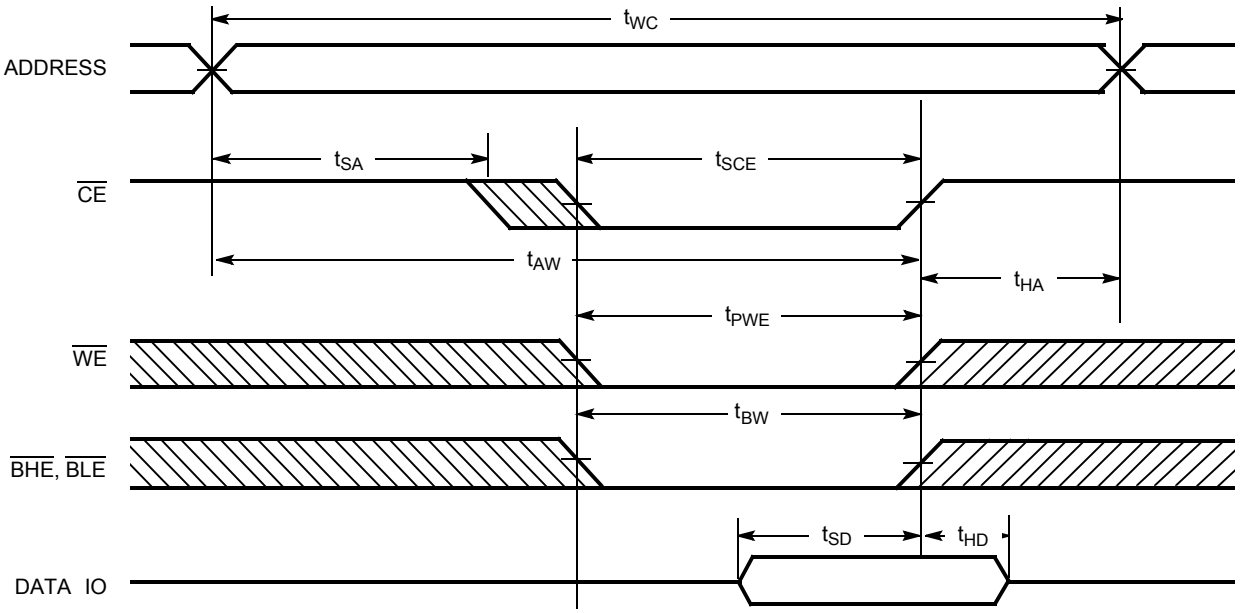
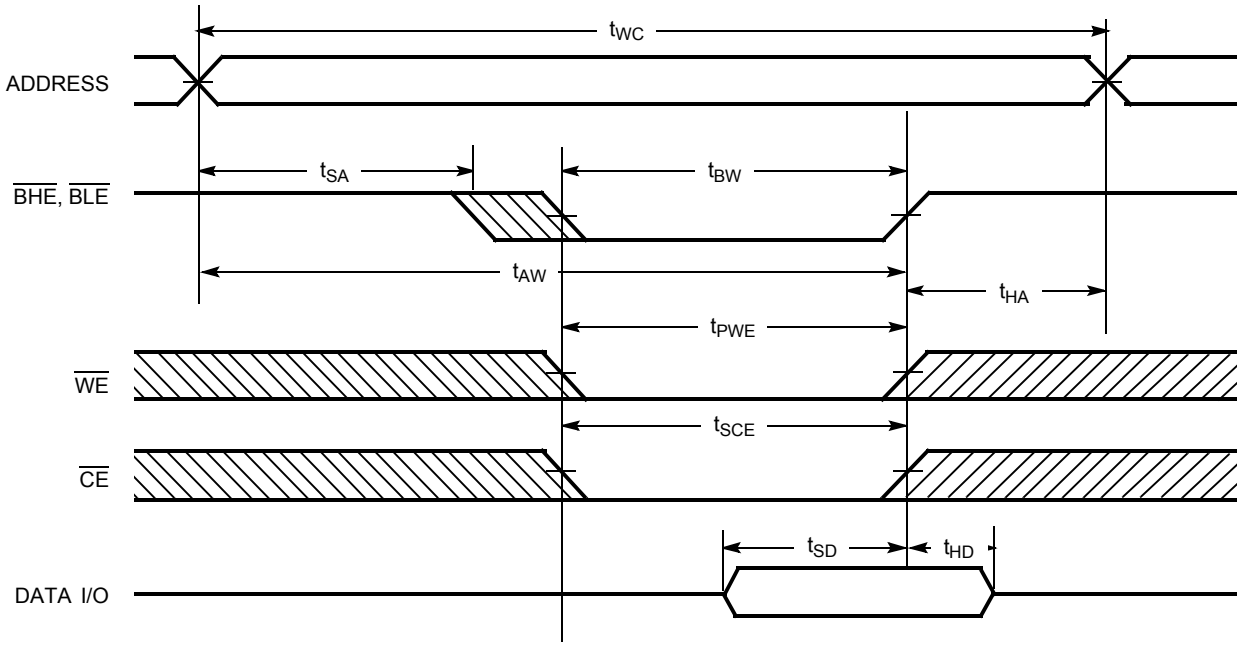


Figure 7. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)

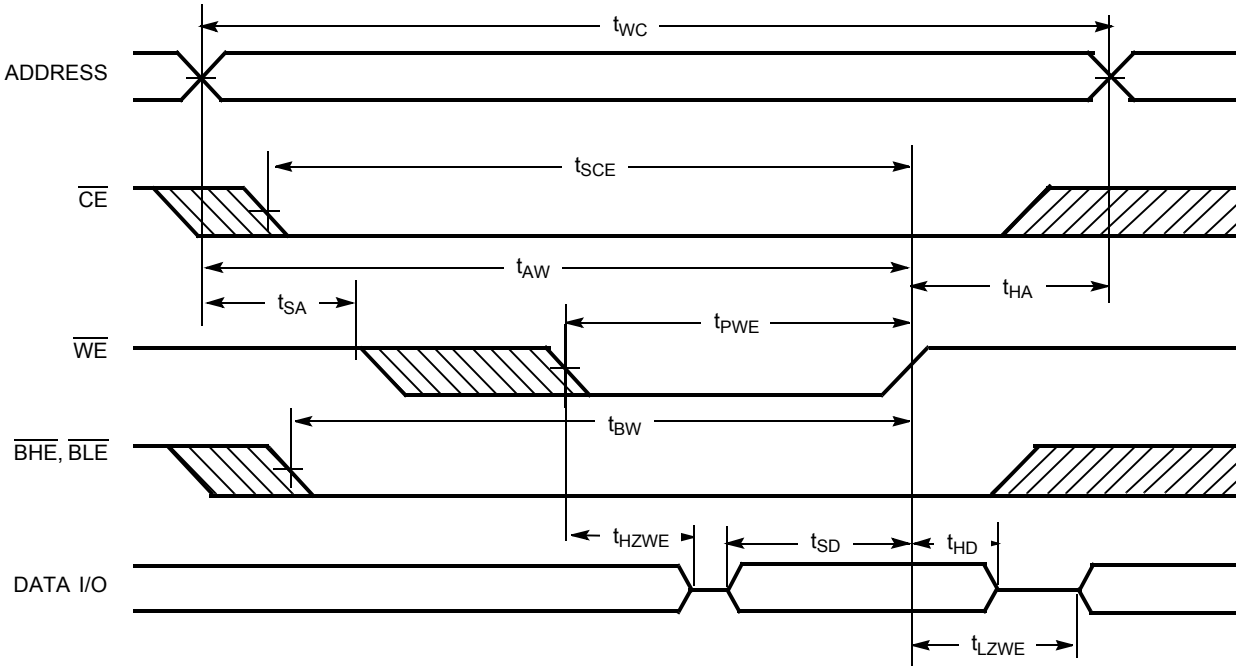


Notes
14. Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

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Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [16]



Notes
16. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

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Truth Table

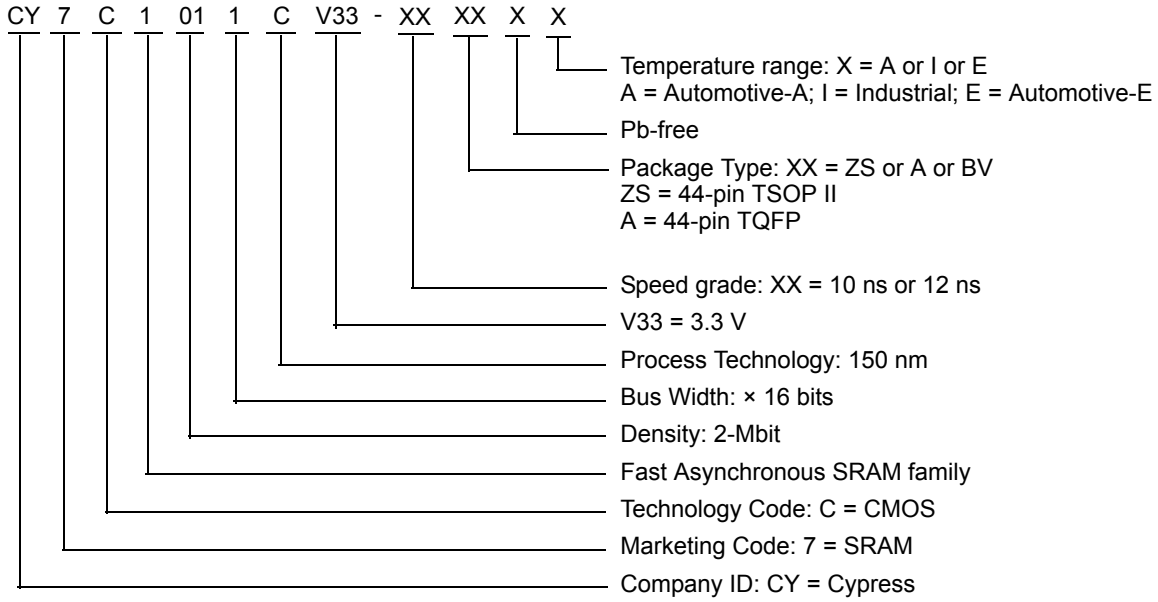
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – all bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read – lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read – upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – all bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write – lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write – upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

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Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1011CV33-10ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A
12	CY7C1011CV33-12ZSXE	51-85087	44-pin TSOP II (Pb-free)	Automotive-E

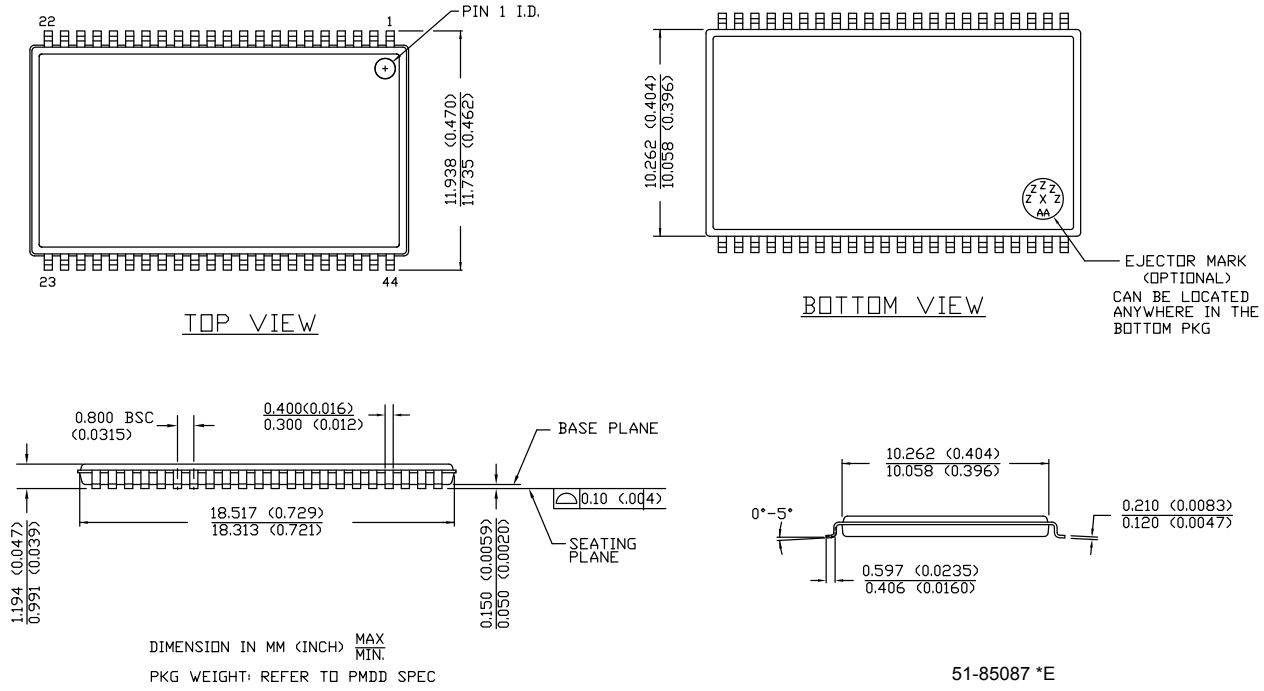
Ordering Code Definitions



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Package Diagrams

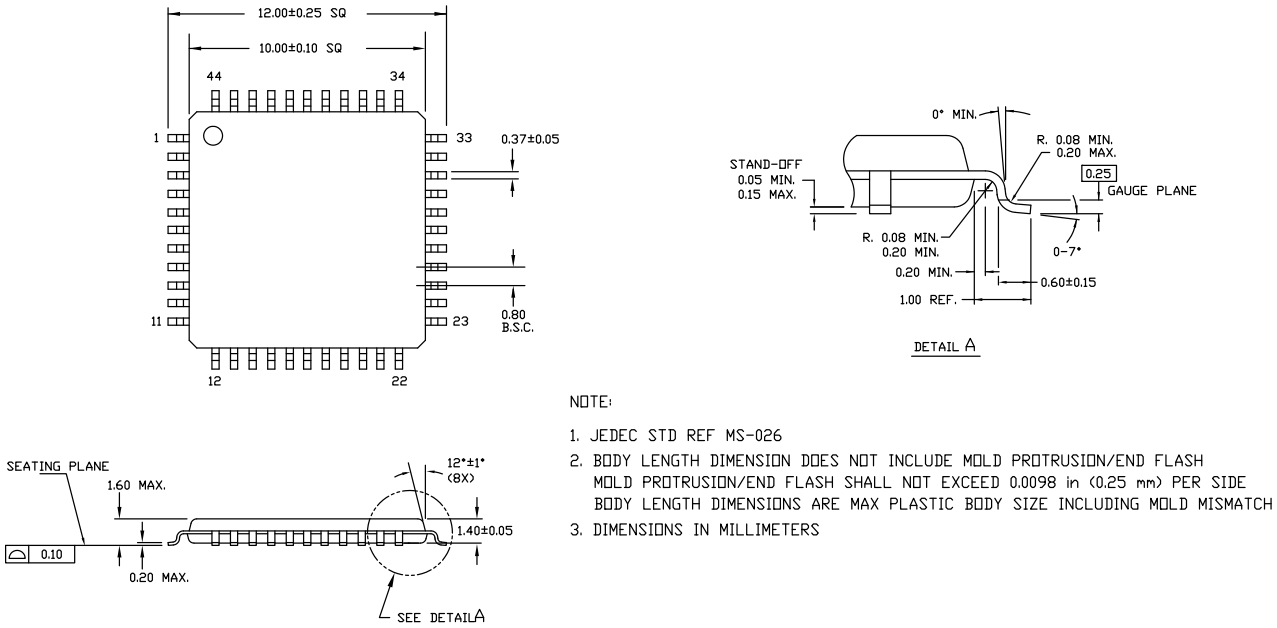
Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



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Package Diagrams (continued)

Figure 10. 44-pin TQFP (10 × 10 × 1.4 mm) A44S Package Outline, 51-85064



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *F

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Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
mW	milliwatt
ns	nanosecond
%	percent
pF	pico farad
V	volt
W	watt

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Document History Page

Document Title: CY7C1011CV33, 2-Mbit (128 K × 16) Static RAM Document Number: 38-05232				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	117132	HGK	07/31/02	New data sheet.
*A	118057	HGK	08/19/02	Updated Pin Configuration: Corrected 48-ball FBGA pinout.
*B	119702	DFP	10/11/02	Replaced FBGA with VFBGA in all instances across the document. Updated Selection Guide: Changed value of CMOS standby current from 8 mA to 10 mA. Updated Pin Configuration: Updated address pinouts to “A0 to A16”. Updated Ordering Information: No change in part numbers. Updated package code to BV48A.
*C	386106	PCI	See ECN	Updated Ordering Information (Added lead-free parts).
*D	498501	NXR	See ECN	Updated Logic Block Diagram: Corrected typo. Updated Maximum Ratings: Included Static Discharge Voltage. Included Latch up Current. Updated Electrical Characteristics: Changed the description of I_{IX} parameter from “Input Load Current” to “Input Leakage Current”. Updated Ordering Information.
*E	522620	VKN	See ECN	Added Thermal Resistance.
*F	1891366	VKN / AESA	See ECN	Updated Ordering Information (Added -10ZSXA part).
*G	2428606	VKN / PYRS	See ECN	Removed 15 ns speed bin related information in all instances across the document. Removed Commercial Temperature Range related information in all instances across the document. Updated Pin Configuration: Corrected typo in the 44-pin TSOP and 48-ball FBGA pinout. Updated Ordering Information (Removed inactive parts).
*H	2664421	VKN / AESA	02/25/09	Added Automotive-E Temperature Range related information (corresponding to 12 ns speed bin) in all instances across the document. Updated Ordering Information.
*I	2898399	KAO / AJU	03/24/2010	Updated Package Diagrams.
*J	2950666	VKN	06/11/2010	Added Contents. Updated Ordering Information: Included MPN “CY7C1011CV33-12BVXE”. Added Ordering Code Definitions. Added Acronyms. Updated Sales, Solutions, and Legal Information.
*K	3089939	PRAS	11/13/2010	Updated Ordering Information (Removed inactive parts).
*L	3276463	KAO	06/07/2011	Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Added Units of Measure. Updated Package Diagrams. Updated to new template.

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Document History Page (continued)

Document Title: CY7C1011CV33, 2-Mbit (128 K × 16) Static RAM Document Number: 38-05232				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*M	3591978	TAVA	04/19/2012	Removed 48-ball VFBGA package related information in all instances across the document. Updated Package Diagrams.
*N	3861271	KAO	01/08/2013	Updated Ordering Information (Updated part numbers). Updated Package Diagrams: spec 51-85087 – Changed revision from *D to *E.
*O	4578508	KAO	11/21/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Switching Waveforms: Added Note 16 and referred the same note in Figure 8. Updated Package Diagrams: spec 51-85064 – Changed revision from *E to *F.
*P	4856402	VINI	07/24/2015	Updated to new template. Completing Sunset Review.

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Wireless/RF	cypress.com/go/wireless

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