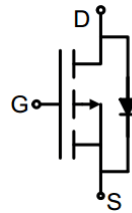
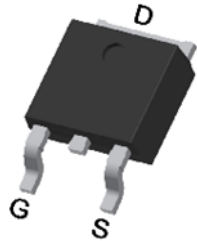


P-Channel Enhancement Mode Power MOSFET

Description The G15P04K uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.		 Schematic diagram	
General Features • V_{DS} -40V • I_D (at $V_{GS} = -10V$) -15A • $R_{DS(ON)}$ (at $V_{GS} = -10V$) < 39mΩ • $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 70mΩ • 100% Avalanche Tested • RoHS Compliant		 TO-252	
Application • Power switch • DC/DC converters			
Device	Package	Marking	Packaging
G15P04K	TO-252	G15P04	2500pcs/Reel

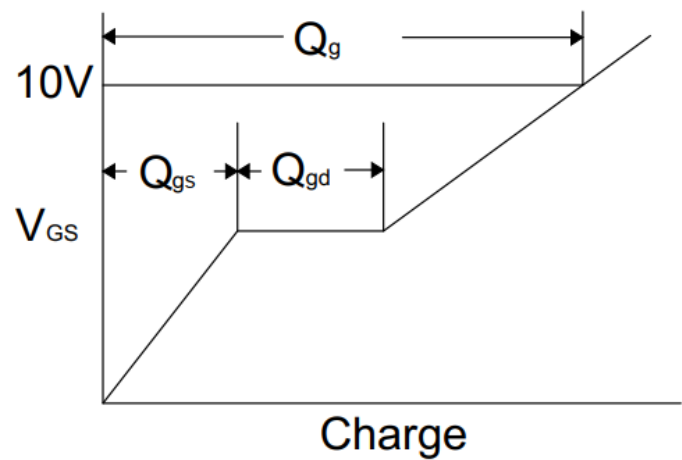
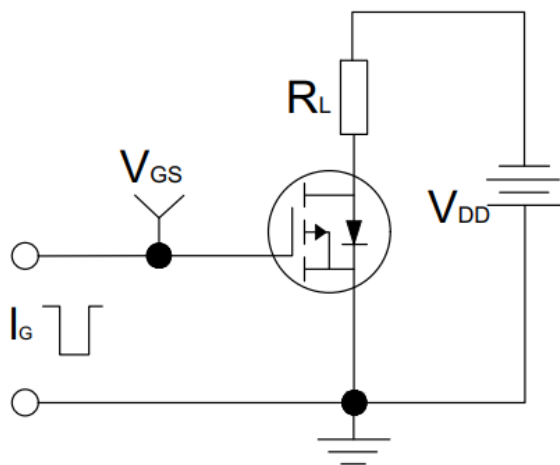
Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted			
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-40	V
Continuous Drain Current	I_D	-15	A
Pulsed Drain Current (note1)	I_{DM}	-60	A
Gate-Source Voltage	V_{GS}	± 20	V
Single Pulse Avalanche Energy (note3)	E_{AS}	36	mJ
Power Dissipation	P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	$^\circ\text{C}$
Thermal Resistance			
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R_{thJC}	3	$^\circ\text{C/W}$

Specifications T _j = 25°C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-40	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -40V, V _{GS} = 0V	--	--	-1	uA
Gate-Source Leakage	I _{GSS}	V _{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-1.5	-3.0	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10V, I _D = - 10A	--	25	39	mΩ
		V _{GS} = -4.5V, I _D = - 8A	--	30	70	
Forward Transconductance	g _{FS}	V _{DS} =10V,I _D =-10A	--	10	--	S
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -20V, f = 1.0MHz	--	930	--	pF
Output Capacitance	C _{oss}		--	85	--	
Reverse Transfer Capacitance	C _{rss}		--	35	--	
Total Gate Charge	Q _g	V _{DD} = -20V, I _D = -6A, V _{GS} = -10V	--	25	--	nC
Gate-Source Charge	Q _{gs}		--	3	--	
Gate-Drain Charge	Q _{gd}		--	7	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} = -20V, I _D = -6A, R _G = 3Ω	--	8	--	ns
Turn-on Rise Time	t _r		--	4	--	
Turn-off Delay Time	t _{d(off)}		--	32	--	
Turn-off Fall Time	t _f		--	7	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I _S	T _C = 25°C	--	--	-15	A
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} = -10A, V _{GS} = 0V	--	--	-1.2	V
Reverse Recovery Time	T _{rr}	I _S = -15A, V _{GS} = 0V di/dt=-100A/us	--	25	--	ns
Reverse Recovery Charge	Q _{rr}		--	31	--	nc

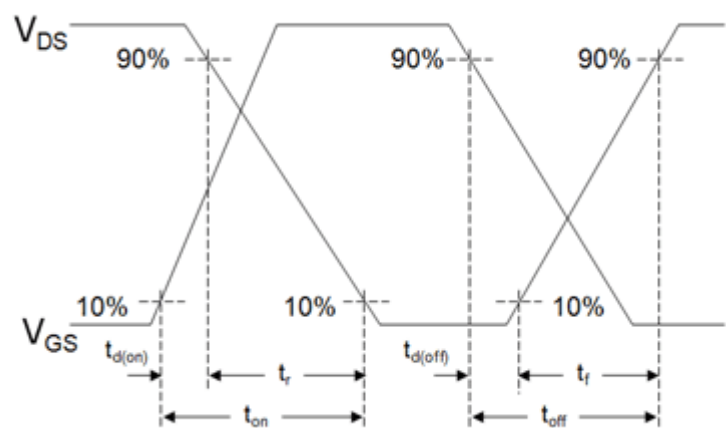
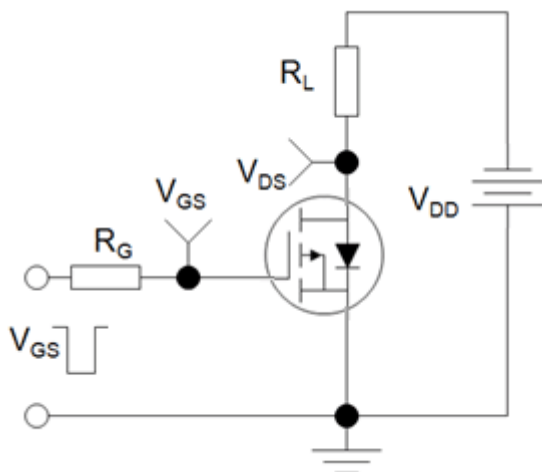
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G
3. $V_{DD} = -40V, R_G = 25\Omega, L = 0.5\text{ mH}$, Starting $T_J = 25^\circ\text{C}$.

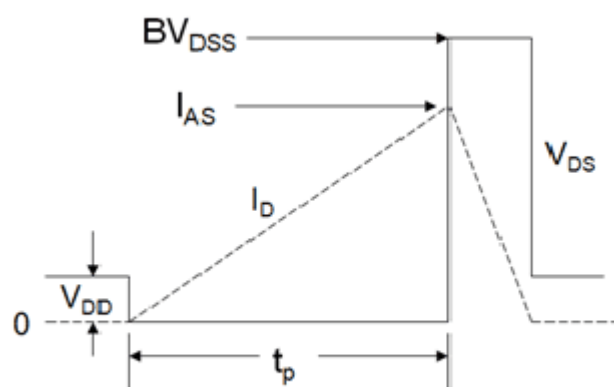
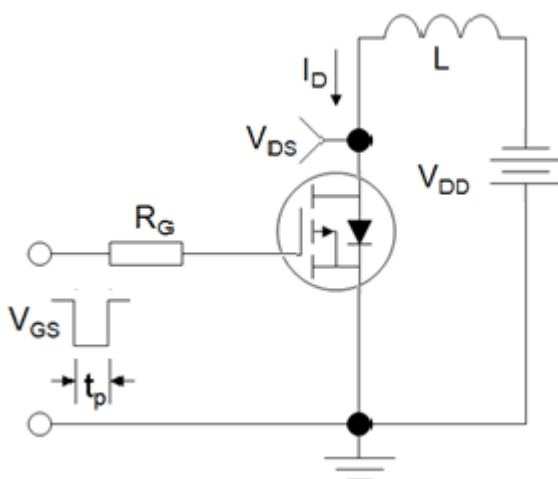
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

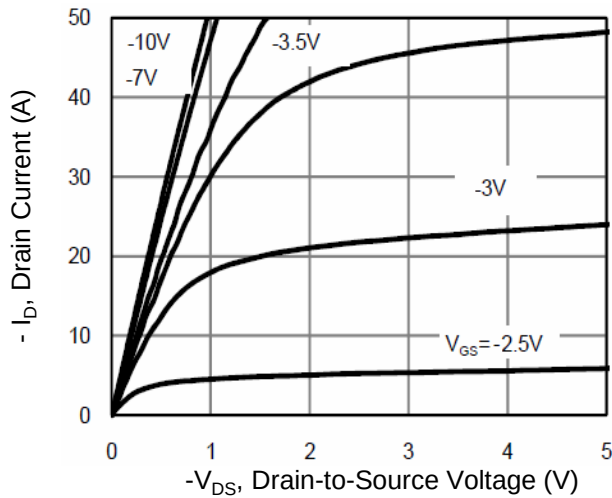


Figure 2. Transfer Characteristics

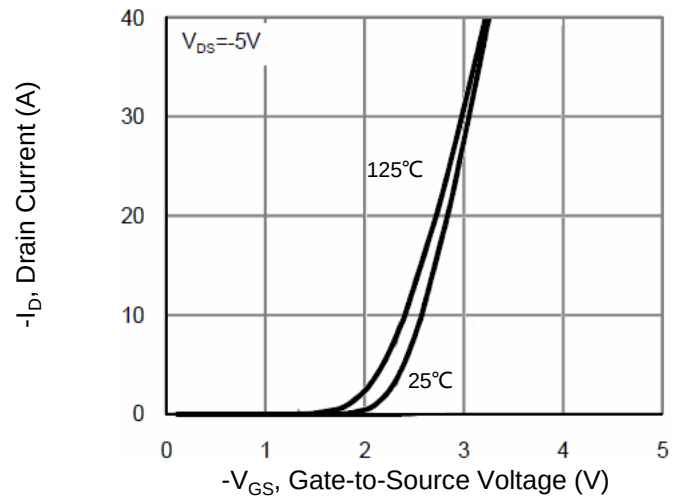


Figure 3. Gate Charge

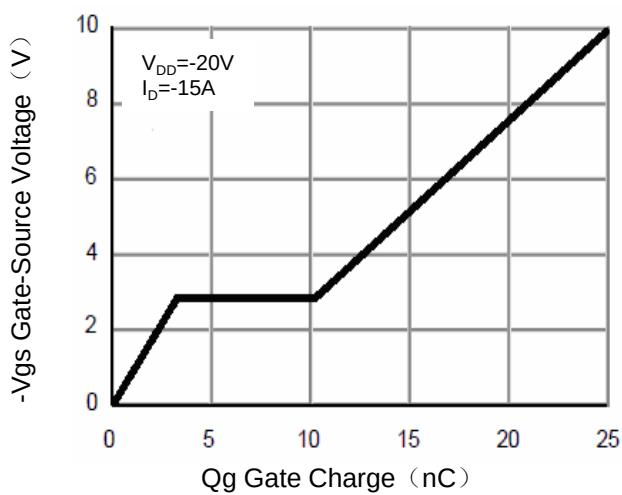


Figure 4. Drain Source On Resistance

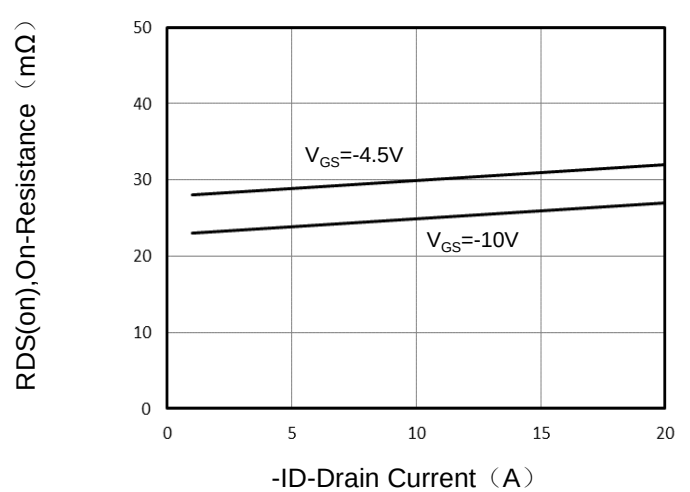


Figure 5. Capacitance

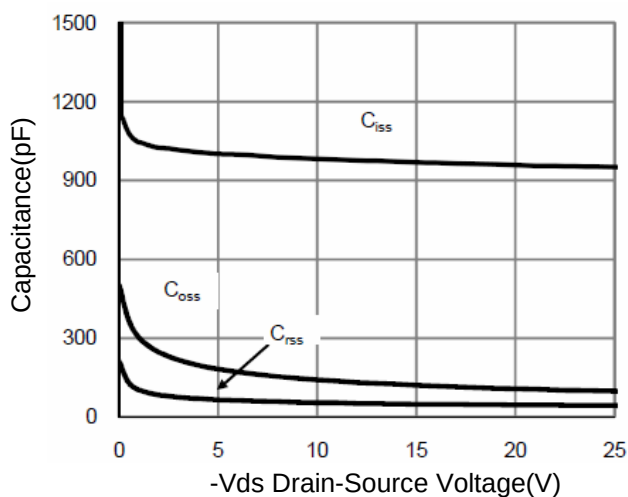
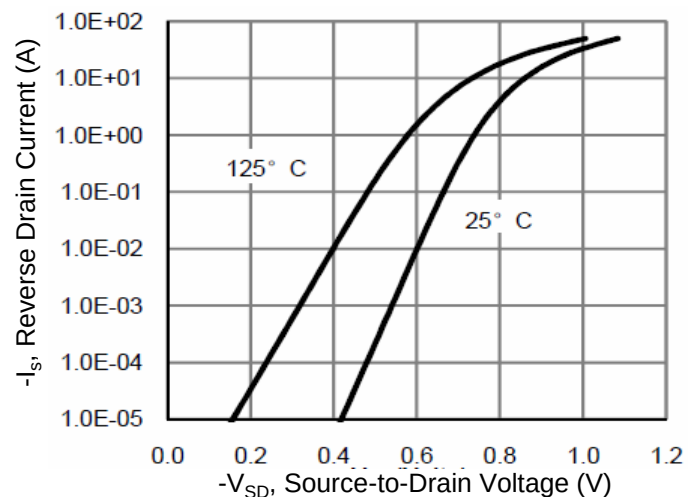


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

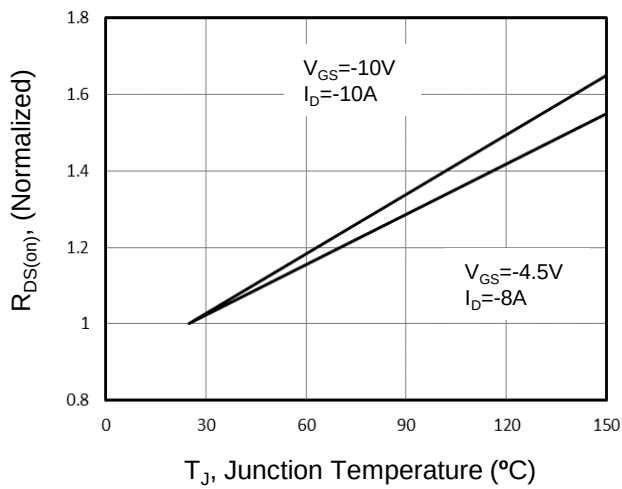


Figure 8. Safe Operation Area

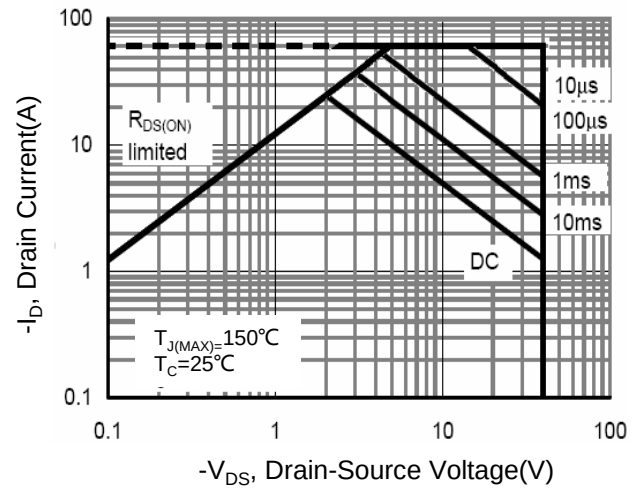
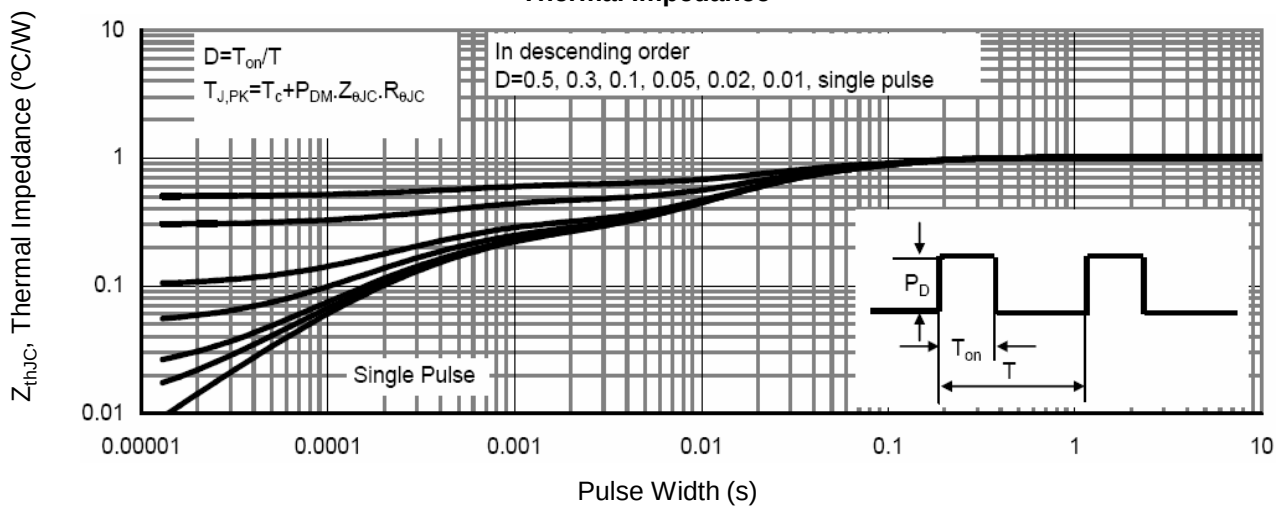
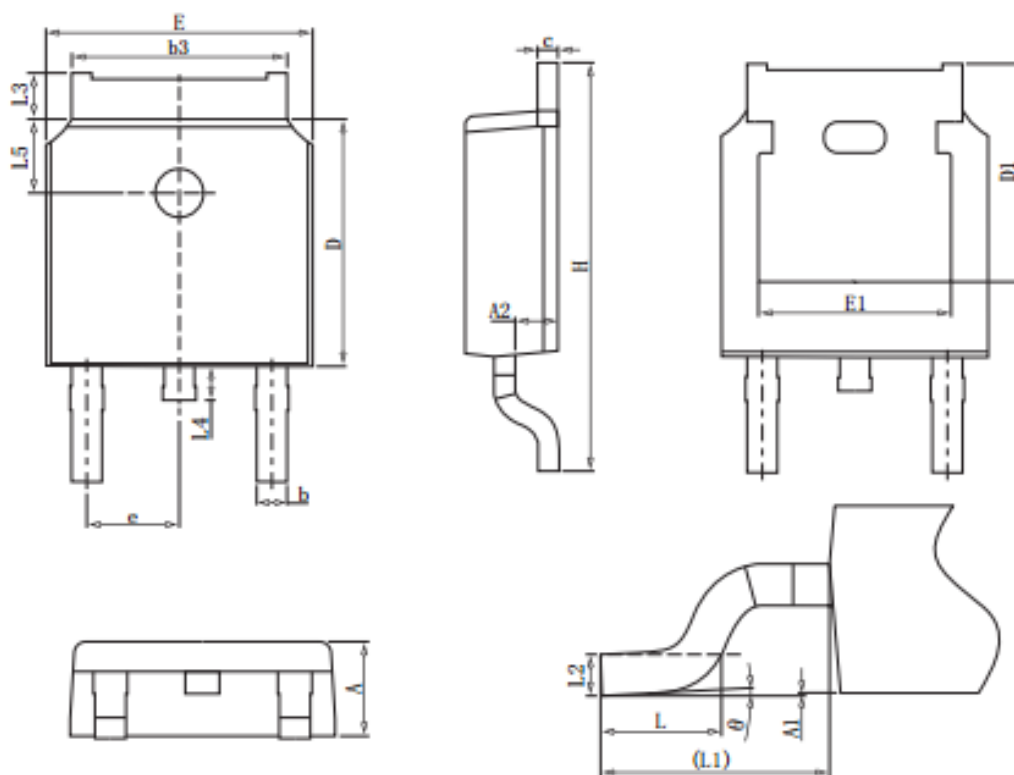


Figure 9. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	2.2	2.3	2.4
A1	0		0.2
A2	0.97	1.07	1.17
b	0.68	0.78	0.9
b3	5.2	5.33	5.5
c	0.43	0.53	0.63
D	5.98	6.1	6.22
D1	5.30REF		
E	6.4	6.6	6.8
E1	4.63		
e	2.286BSC		
H	9.4	10.1	10.5
L	1.38	1.5	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88		1.28
L4	0.5		1
L5	1.65	1.8	1.95
θ	0°		8°