TOSHIBA Field-Effect Transistor Silicon N / P Channel MOS Type

SSM6L14FE

- O Power Management Switch Applications
- High-Speed Switching Applications

N-ch: 1.5-V drive
P-ch: 1.5-V drive
N-ch, P-ch, 2-in-1

Low ON-resistance Q1 N-ch:R_{DS(ON)} = 330 mΩ (max) (@V_{GS} = 2.5 V)

 $R_{DS(ON)} = 240 \text{ m}\Omega \text{ (max) (@V_{GS} = 4.5 V)}$

Q2 P-ch: $R_{DS(ON)}$ = 440 m Ω (max) (@V_{GS} = -2.5 V)

 $R_{DS(ON)} = 300 \text{ m}\Omega \text{ (max) (@V_{GS} = -4.5 V)}$

Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	20	V
Gate-source voltage		V _{GSS}	±10	V
Drain current	DC	I _D	0.8	Α
	Pulse	I _{DP}	1.6	A

Q2 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	-20	V
Gate-source voltage		V _{GSS}	±8	V
Drain current	DC	I _D	-0.72	Α
	Pulse	I _{DP}	-1.44	

Unit: mm 1.6±0.05 1.2±0.05 .0±0.05 $.6\pm0.05$ 2±0. 1.Source1 4.Source2 2.Gate1 5.Gate2 3.Drain2 6.Drain1 ES6 **JEDEC** JEITA **TOSHIBA** 2-2N1D

Weight: 3.0 mg (typ.)

Absolute Maximum Ratings (Ta = 25 °C) (Q1, Q2 Common)

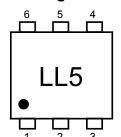
Characteristics	Symbol	Rating	Unit
Power dissipation	P _D (Note 1)	150	mW
Channel temperature	T _{ch}	150	°C
Storage temperature range	T _{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

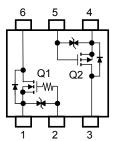
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Mounted on an FR4 board. (total dissipation) (25.4 mm \times 25.4 mm \times 1.6 mm, Cu Pad: 0.135 mm² \times 6)

Marking



Equivalent Circuit (top view)



Start of commercial production 2009-12



Q1 Electrical Characteristics (Ta = 25°C)

Chara	cteristics	Symbol	Test Conditions	Min	Тур.	Max	Unit
Drain-source breakdown voltage		V (BR) DSS	I _D = 1 mA, V _{GS} = 0 V	20	_	_	· V
		V (BR) DSX	I _D = 1 mA, V _{GS} = - 10 V	12	_	_	
Drain cutoff curren	t	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	_	_	1	μА
Gate leakage curre	ent	I _{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μΑ
Gate threshold vol	tage	V _{th}	V _{DS} = 3 V, I _D = 1 mA	0.35	_	1.0	٧
Forward transfer a	dmittance	Y _{fs}	$V_{DS} = 3 \text{ V}, I_D = 500 \text{ mA}$ (Note 2)	1.05	2.1		S
			$I_D = 500 \text{ mA}, V_{GS} = 4.5 \text{ V}$ (Note 2)	_	185	240	
Drain agurag ON r	ooistanaa		$I_D = 400 \text{ mA}, V_{GS} = 2.5 \text{ V}$ (Note 2)	_	245	330	
Drain-source ON-resistance		R _{DS} (ON)	I _D = 250 mA, V _{GS} = 1.8 V (Note 2)	_	310	450	mΩ
			$I_D = 150 \text{ mA}, V_{GS} = 1.5 \text{ V}$ (Note 2)	_	370	600	
Input capacitance		C _{iss}		_	90	_	pF
Output capacitance		Coss	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	_	21	_	
Reverse transfer capacitance		C _{rss}		_	15	_	
Total gate charge		Qg	V _{DS} = 10 V, I _D = 0.8 A V _{GS} = 4.5 V	_	2.00	_	
Gate-source charge		Q _{gs}		_	1.02	_	
Gate-drain charge		Q _{gd}	, vg3 v	_	0.98	_	
Switching time	Turn-on time	t _{on}	V_{DD} = 10 V, I_{D} = 200 mA V_{GS} = 0 to 2.5 V, R_{G} = 4.7 Ω	_	18	_	ns
	Turn-off time	t _{off}		_	50	_	
Drain-source forward voltage		V _{DSF}	$I_D = -0.8 \text{ A}, V_{GS} = 0 \text{ V}$ (Note 2)	_	-0.84	-1.2	V

Q2 Electrical Characteristics (Ta = 25°C)

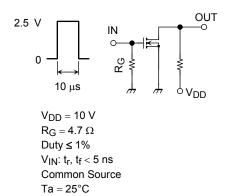
Charac	eteristics	Symbol	Test Conditions	Min	Тур.	Max	Unit
Drain-source breakdown voltage		V (BR) DSS	I _D = -1 mA, V _{GS} = 0 V	-20	_	_	V
		V (BR) DSX	I _D = -1 mA, V _{GS} = 8 V	-12	_	_	V
Drain cutoff current	t	I _{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$	_	_	-10	μА
Gate leakage curre	ent	I _{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$	_		±1	μА
Gate threshold volt	age	V _{th}	V _{DS} = -3 V, I _D = -1 mA	-0.3	_	-1.0	V
Forward transfer ad	dmittance	Y _{fs}	$V_{DS} = -3 \text{ V}, I_D = -400 \text{ mA}$ (Note2)	850		_	mS
			$I_D = -400 \text{ mA}, V_{GS} = -4.5 \text{ V}$ (Note2)	_	0.25	0.30	
Drain aguras ON re	naistanas		$I_D = -200 \text{ mA}, V_{GS} = -2.5 \text{ V}$ (Note2)	_	0.34	0.44	1
Drain-source ON-resistance	R _{DS} (ON)	I _D = -100 mA, V _{GS} = -1.8 V (Note2)	_	0.44	0.67	Ω	
		$I_D = -50 \text{ mA}, V_{GS} = -1.5 \text{ V}$ (Note2)	_	0.55	1.04		
Input capacitance		C _{iss}		_	110	_	
Output capacitance	;	Coss	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	_	28	_	pF
Reverse transfer capacitance		C _{rss}		_	20	_	1
Total gate charge		Qg		_	1.76	_	
Gate-source charge		Q _{gs}	$V_{DS} = -10 \text{ V, } I_{DS} = -720 \text{ mA}$	_	1.22	_	nC
Gate–drain charge		Q _{gd}	- V _{GS} = -4.5 V	_	0.54	_	
Switching time	Turn-on time	t _{on}	$V_{DD} = -10 \text{ V}, I_{D} = -100 \text{ mA}$ $V_{GS} = 0 \text{ to } -2.5 \text{ V}, R_{G} = 50 \Omega$	_	11	_	
	Turn-off time	t _{off}		_	38	_	ns
Drain-source forward voltage		V _{DSF}	$I_D = 720 \text{ mA}, V_{GS} = 0 \text{ V}$ (Note2)	_	0.85	1.2	V

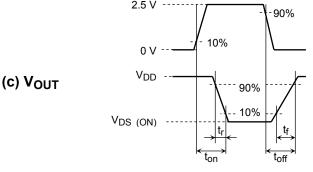
Note 2: Pulse test

Q1 Switching Time Test Circuit

(a) Test Circuit



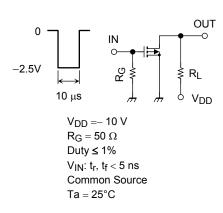




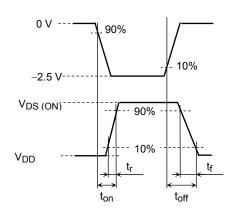
Q2 Switching Time Test Circuit

(a) Test Circuit









Q1 Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (1 mA for the Q1 of the SSM6L14FE). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

Q2 Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (–1 mA for the Q2 of the SSM6L14FE). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

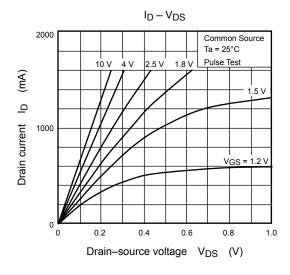
Take this into consideration when using the device.

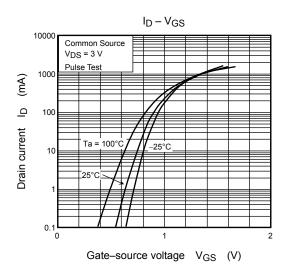
Handling Precaution

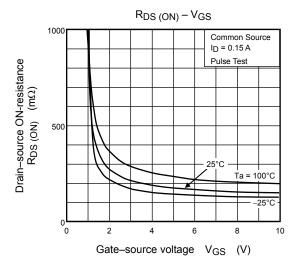
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

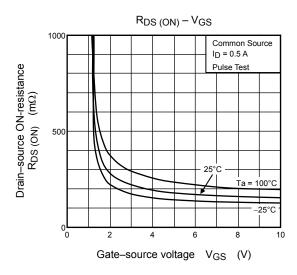
Thermal resistance $R_{th\ (ch-a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

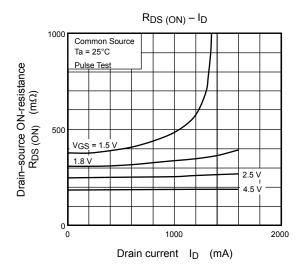
Q1 (N-ch MOSFET)

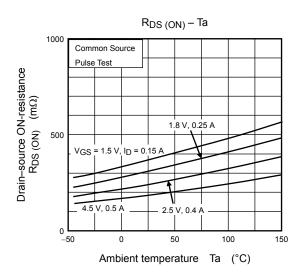




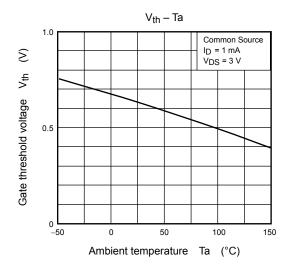


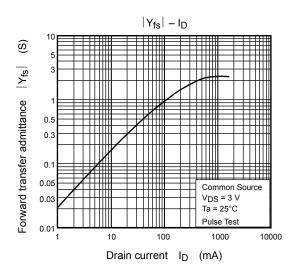


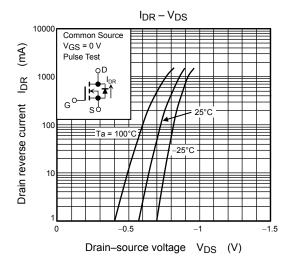


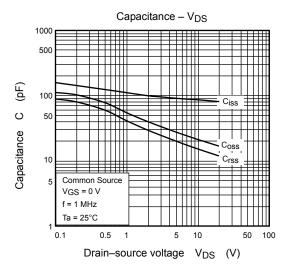


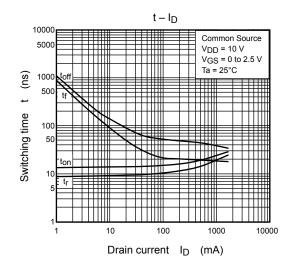
Q1 (N-ch MOSFET)

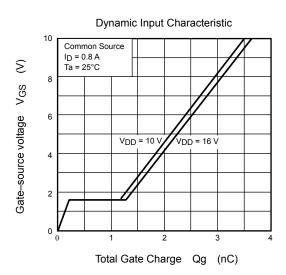










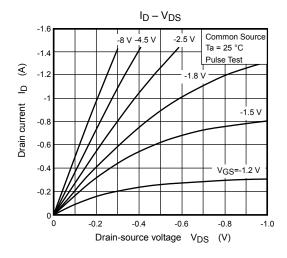


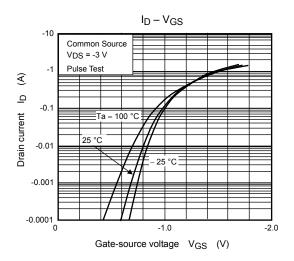


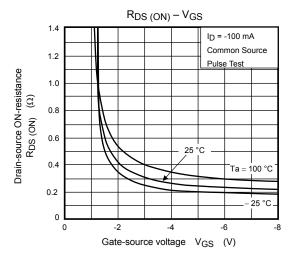
SSM6L14FE

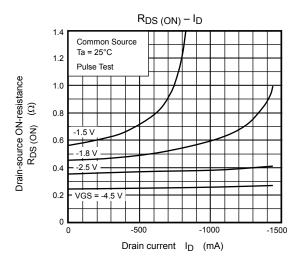


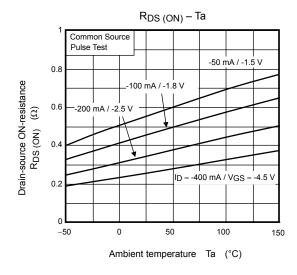
Q2 (P-ch MOSFET)

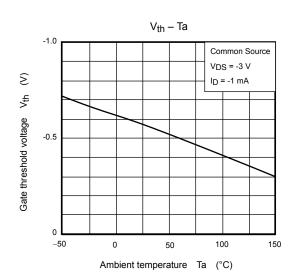






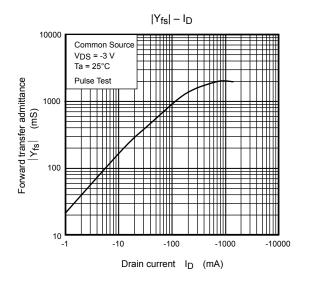


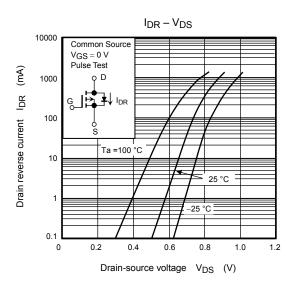


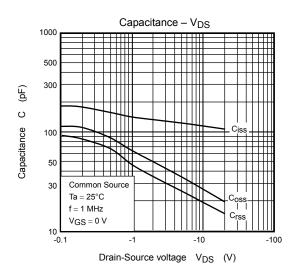


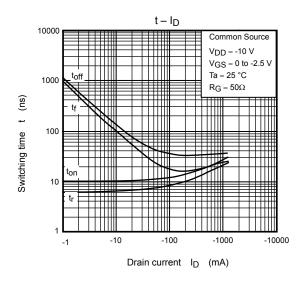


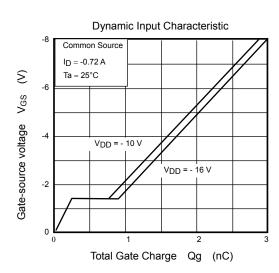
Q2 (P-ch MOSFET)





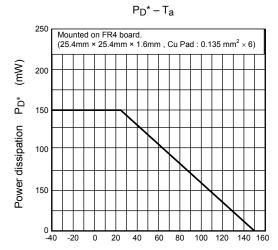








Q1, Q2 Common



*:Total Rating Ambient temperature Ta (°C)

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