MOSFET – Power, Single P-Channel, WDFN8 -30 V

NVTFS012P03P8Z, NVTFWS012P03P8Z

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
−30 V	11.3 mΩ @ −10 V	−49 A
	20 mΩ @ −4.5 V	

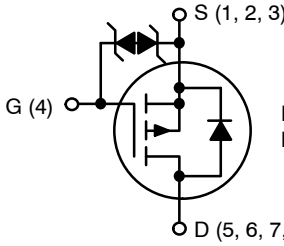
Features

- Small Footprint for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- AEC−Q101 Qualified
- These Devices are Pb−Free, Halogen−Free/BFR−Free and are RoHS Compliant

Applications

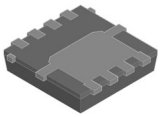
- Battery Management
- Protection
- Power Load Switch

ELECTRICAL CONNECTION



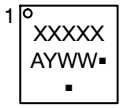


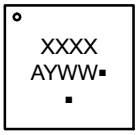
WDFN8
(μ8FL)
CASE 511AB



WDFNW8
(μ8FL WF)
CASE 515AN

MARKING DIAGRAMS





XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−30	V
Gate−to−Source Voltage			V_{GS}	±25	V
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	T_A = 25°C	I_D	−11.7	A
		T_A = 85°C		−8.4	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		T_A = 25°C	P_D	2.40	W
Continuous Drain Current $R_{\theta JC}$	Steady State	T_C = 25°C	I_D	−49	A
		T_C = 85°C		−38	
Power Dissipation $R_{\theta JC}$		T_C = 25°C	P_D	44	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	47	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	52	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	145	
Junction−to−Case	$R_{\theta JC}$	3.3	

1. Surface−mounted on FR4 board using 1 in^2 pad size, 2 oz. Cu pad.
2. Surface−mounted on FR4 board using minimum pad size, 2 oz. Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro−mechanical application board design. $R_{\theta CA}$ is determined by the user's board design.

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5 .

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA	−30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, ref to 25°C		−9.9		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −30 V, T_J = 25°C			−10	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±25 V			±10	μA
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA	−1.0		−3.0	V
Threshold Temperature Coefficient	V_{GS}/T_J	I_D = −250 μA, ref to 25°C		−4.7		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −10 V, I_D = −10 A		8.3	11.3	mΩ
		V_{GS} = −4.5 V, I_D = −10 A		13.3	20	
Forward Transconductance	g_{FS}	V_{DS} = −5 V, I_D = −10 A		41		S
CHARGES AND CAPACITANCES						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −15 V, f = 1.0 MHz		1535		pF
Output Capacitance	C_{oss}			526		
Reverse Transfer Capacitance	C_{rss}			506		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −10 A		21		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.4		nC
Gate−to−Source Charge	Q_{GS}			2.8		
Gate−to−Drain Charge	Q_{GD}			14.8		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −10 A		36		nC
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 5)						
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −4.5 V, V_{DD} = −15 V, I_D = −10 A, R_G = 6 Ω		15		ns
Rise Time	t_r			66		
Turn−Off Delay Time	$t_{d(off)}$			48		
Fall Time	t_f			77		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 5)						
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −10 V, V_{DD} = −15 V, I_D = −10 A, R_G = 6 Ω		7		ns
Rise Time	t_r			17		
Turn−Off Delay Time	$t_{d(off)}$			89		
Fall Time	t_f			75		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −10 A, T_J = 25°C		0.82	1.3	V
		T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = −100 A/μs, I_S = −10 A		19		ns
Reverse Recovery Charge	Q_{RR}			10		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

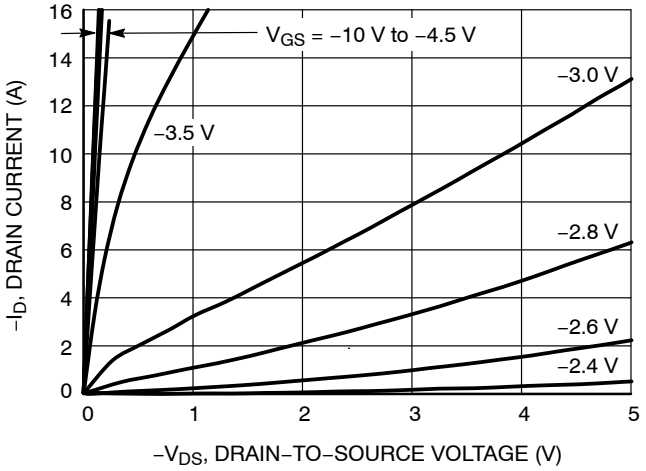


Figure 1. On−Region Characteristics

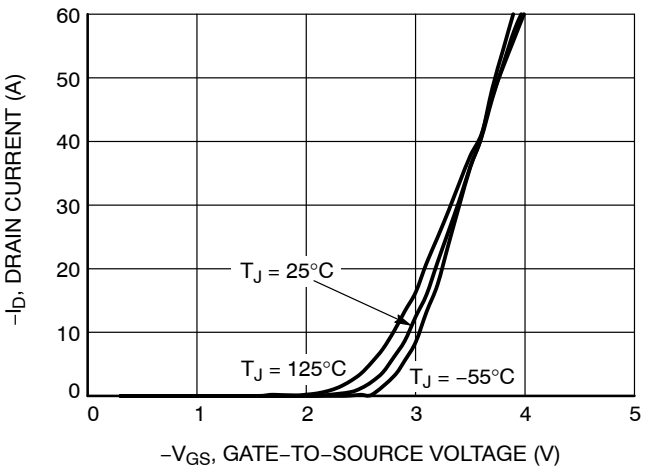


Figure 2. Transfer Characteristics

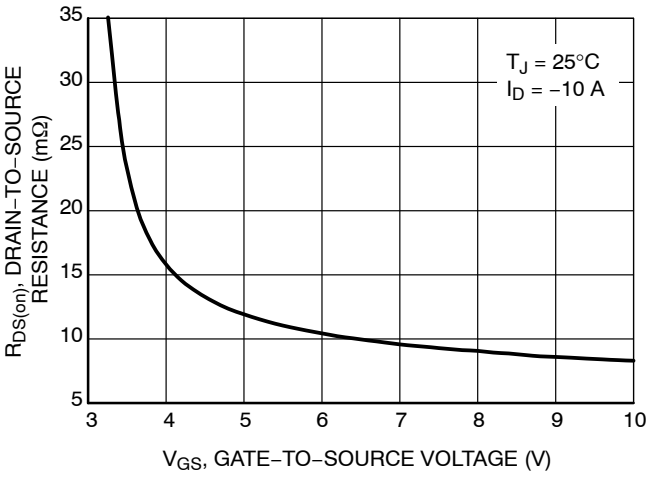


Figure 3. On−Resistance vs. Gate−to−Source Voltage (V)

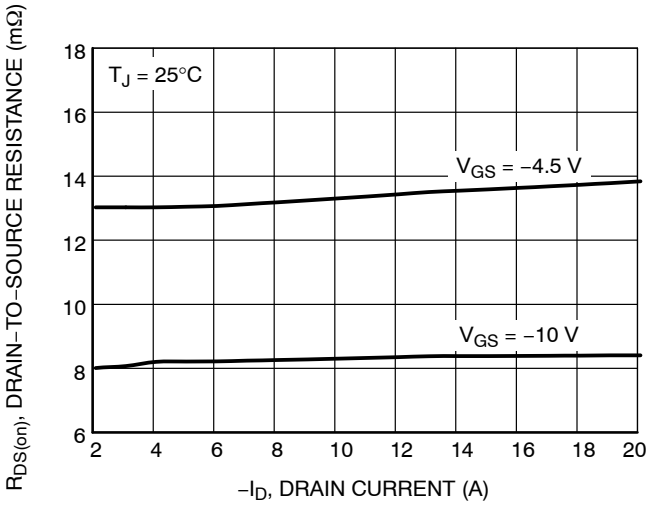


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

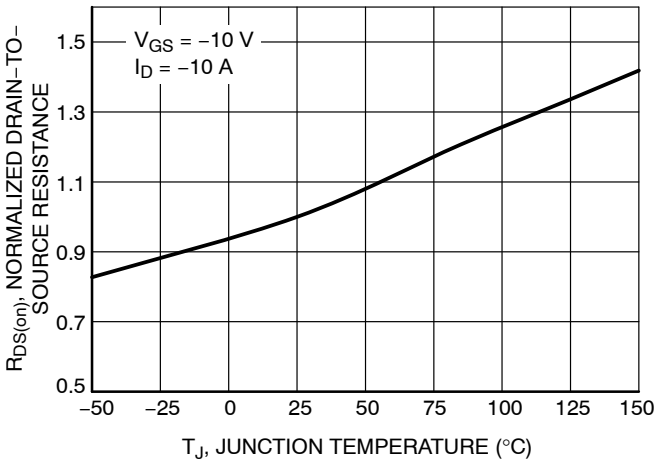


Figure 5. On−Resistance Variation with Temperature

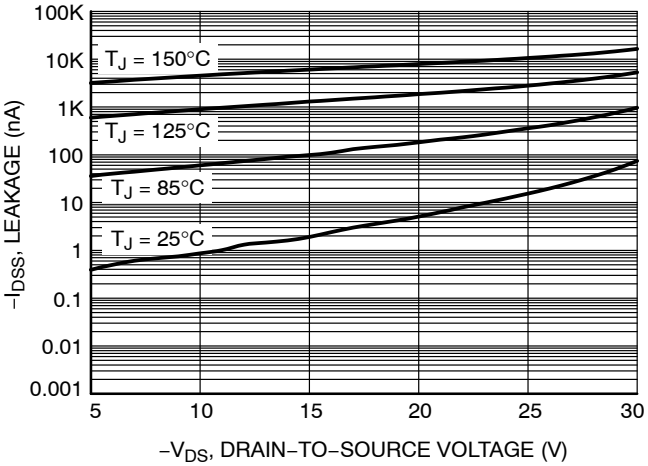


Figure 6. Drain−to−Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

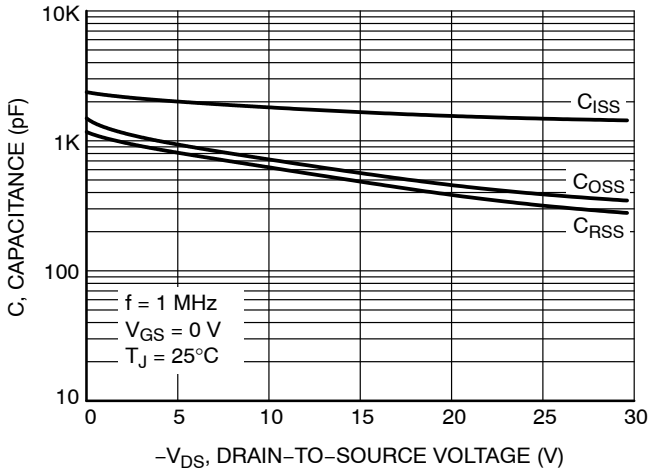


Figure 7. Capacitance Variation

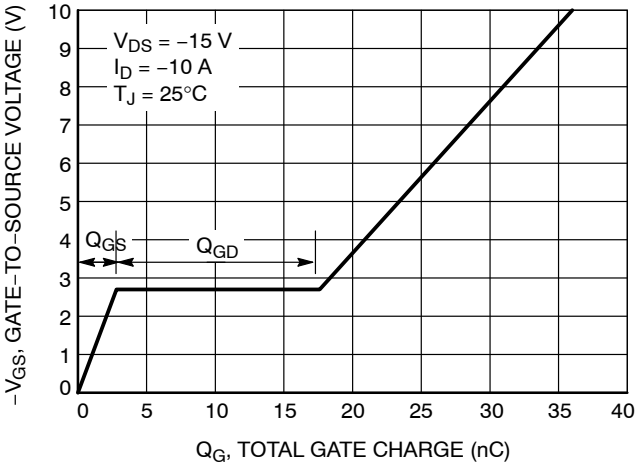


Figure 8. Gate−to−Source vs. Total Charge

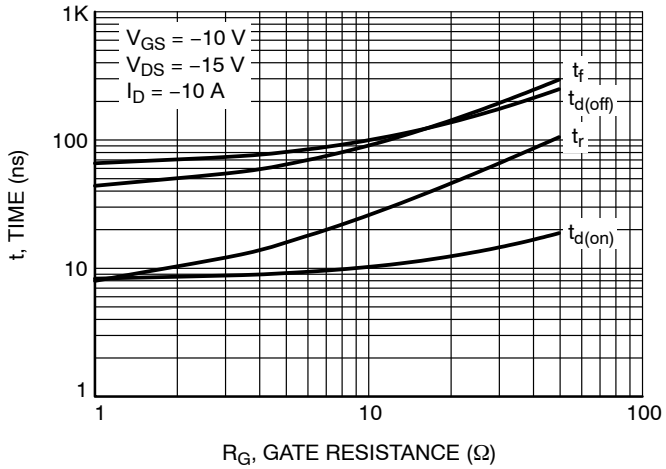


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

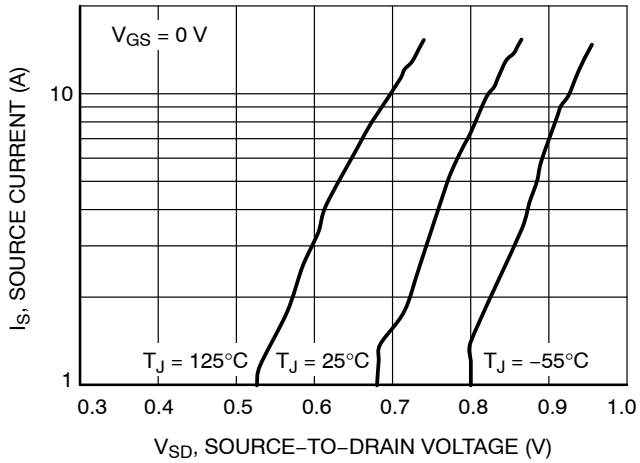


Figure 10. Diode Forward Voltage vs. Current

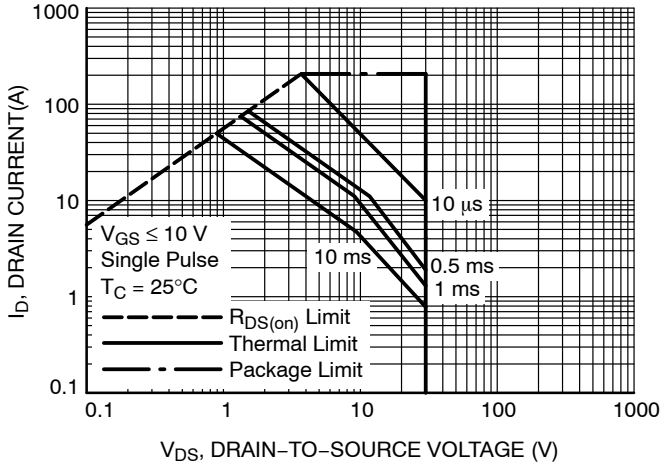


Figure 11. Maximum Rated Forward Biased Safe Operating Area

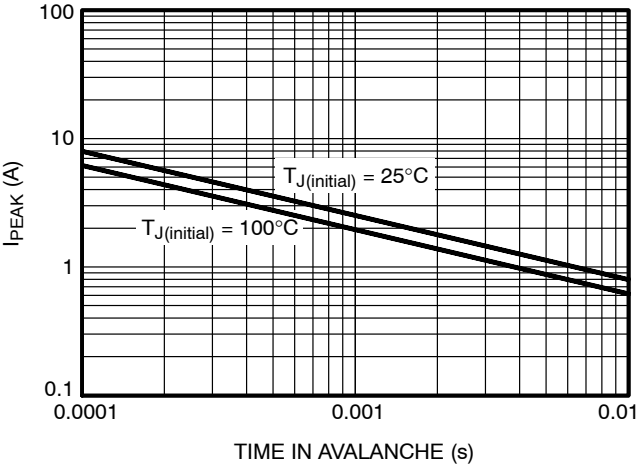


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

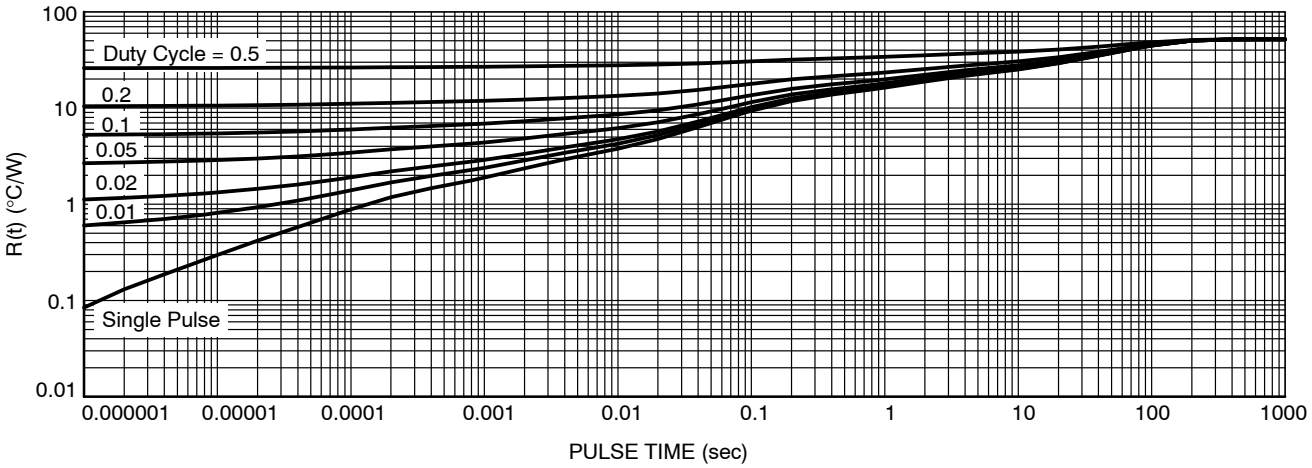


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
NVTFWS012P03P8ZTAG	12PW	WDFN8 (Pb−Free, Wettable Flank)	1500 / Tape & Reel

DISCONTINUED (Note 6)

NVTFS012P03P8ZTAG	12P3	WDFN8 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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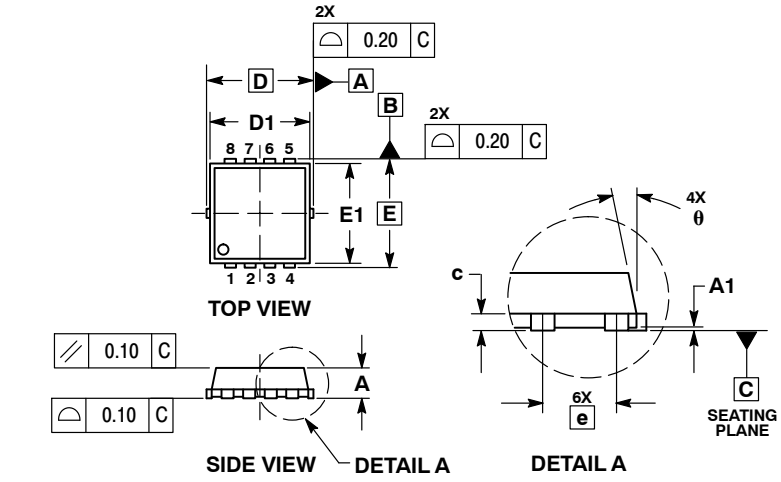
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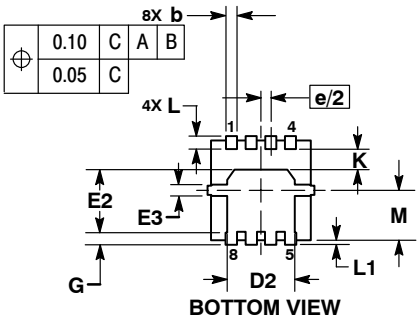
WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

DATE 23 APR 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D		3.30 BSC			0.130 BSC	
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E		3.30 BSC			0.130 BSC	
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e		0.65 BSC			0.026 BSC	
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °



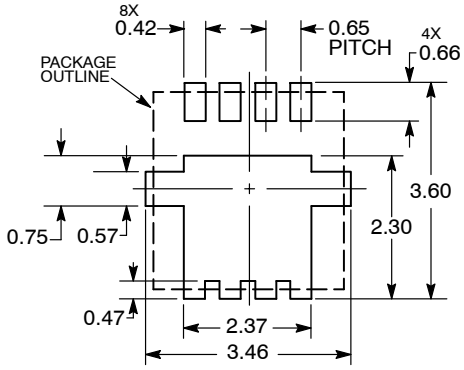
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



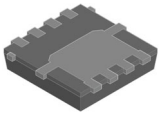
DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**	**PAGE 1 OF 1**

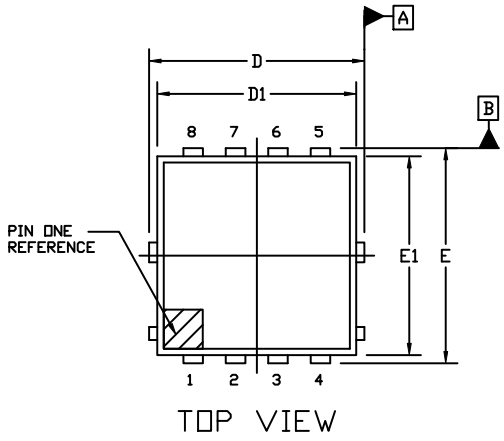
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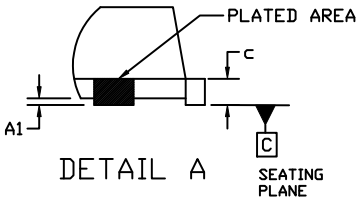


WDFNW8 3.3x3.3, 0.65P (Full−Cut µ8FL WF)
CASE 515AN
ISSUE O

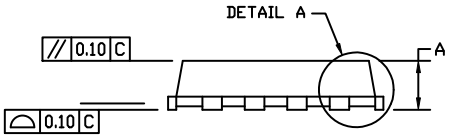
DATE 25 AUG 2020



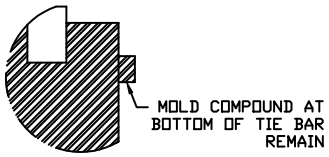
TOP VIEW



DETAIL A



SIDE VIEW

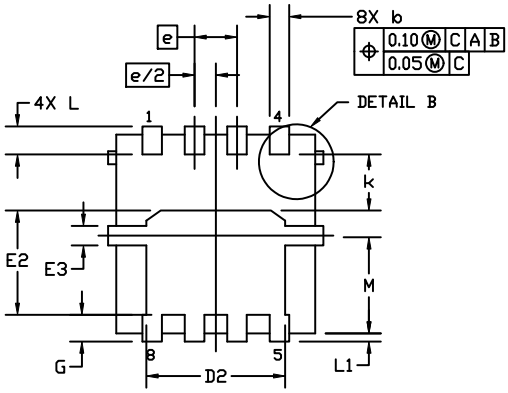


DETAIL B

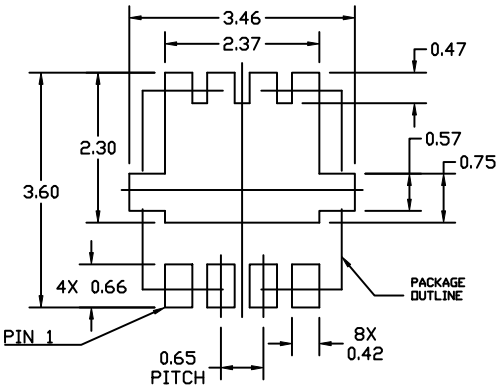
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



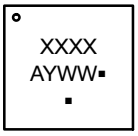
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFNW8 3.3x3.3, 0.65P (Full−Cut µ8FL WF)**	**PAGE 1 OF 1**

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