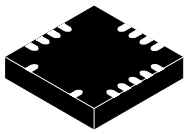
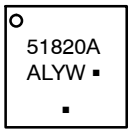
High Speed Half-Bridge Driver for GaN Power Switches

NCP51820



QFN15 4x4, 0.5P
CASE 485FN

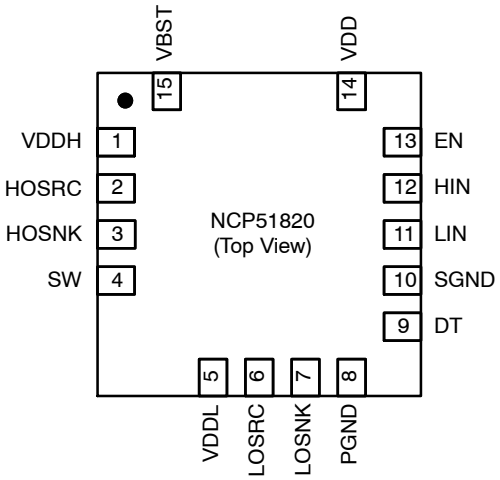
MARKING DIAGRAM



51820A	= Specific Device Code
A	= Assembly Site
L	= Wafer Lot Number
YW	= Assembly Start Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NCP51820AMNTWG	QFN15 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

The NCP51820 high−speed, gate driver is designed to meet the stringent requirements of driving enhancement mode (e−mode), high electron mobility transistor (HEMT) and gate injection transistor (GIT), gallium nitrade (GaN) power switches in off−line, half−bridge power topologies. The NCP51820 offers short and matched propagation delays with advanced level shift technology providing −3.5 V to +650 V (typical) common mode voltage range for the high−side drive and −3.5 V to +3.5 V common mode voltage range for the low−side drive. In addition, the device provides stable dV/dt operation rated up to 200 V/ns for both driver output stages in high speed switching applications.

To fully protect the gate of the GaN power transistor against excessive voltage stress, both drive stages employ a dedicated voltage regulator to accurately maintain the gate−source drive signal amplitude. The circuit actively regulates the driver's bias rails and thus protects against potential gate−source over−voltage under various operating conditions.

The NCP51820 offers important protection functions such as independent under−voltage lockout (UVLO), monitoring VDD bias voltage and VDDH and VDDL driver bias and thermal shutdown based on die junction temperature of the device. Programmable dead−time control can be configured to prevent cross−conduction.

Features

- 650 V, Integrated High−Side and Low−Side Gate Drivers
- Recommended for Soft Switching Applications
- UVLO Protections for VDD High and Low−Side Drivers
- Dual TTL Compatible Schmitt Trigger Inputs
- Split Output Allows Independent Turn−ON/Turn−OFF Adjustment
- Source Capability: 1 A; Sink Capability: 2 A
- Separated HO and LO Driver Output Stages
- 1 ns Rise and Fall Times Optimized for GaN Devices
- SW and PGND: Negative Voltage Transient up to 3.5 V
- 200 V/ns dV/dt Rating for all SW and PGND Referenced Circuitry
- Maximum Propagation Delay of Less Than 50 ns
- Matched Propagation Delays to Less Than 5 ns
- User Programmable Dead−Time Control
- Thermal Shutdown (TSD)

Typical Applications

- Driving GaN Power Transistors used in Soft Switching Full or Half−Bridge, LLC, Active Clamp Flyback or Forward, Totem Pole PFC and Synchronous Rectifier Topologies
- Industrial Inverters and Motor Drives
- AC to DC Converters

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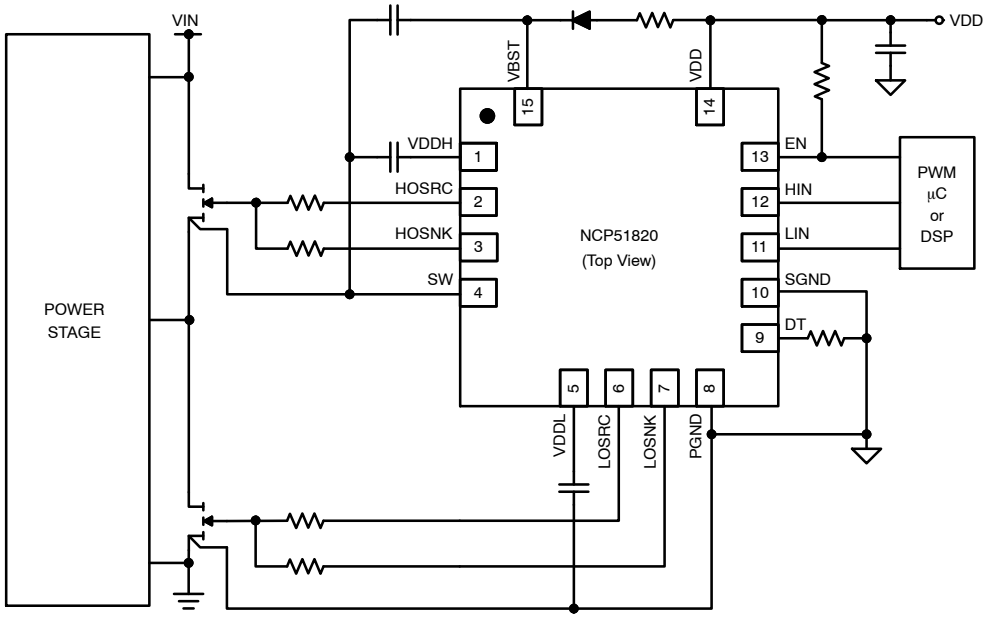

Figure 1. Typical Application Schematic

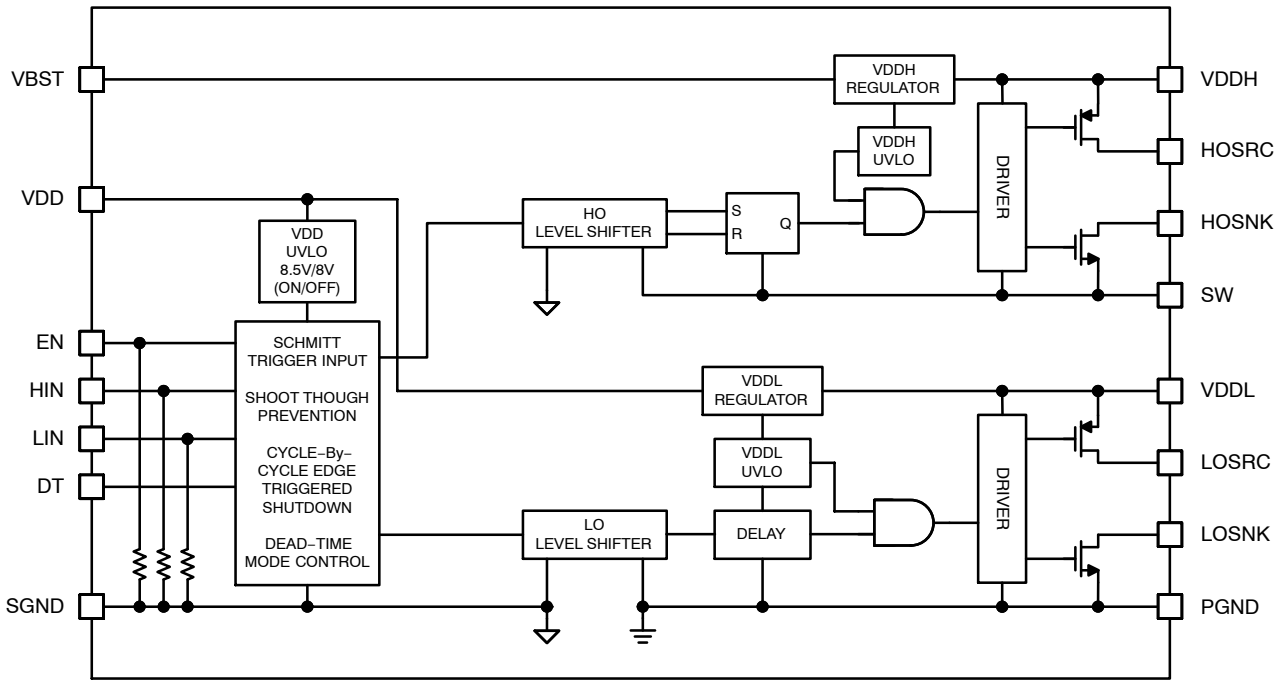

Figure 2. Internal Block Diagram

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PIN CONNECTIONS

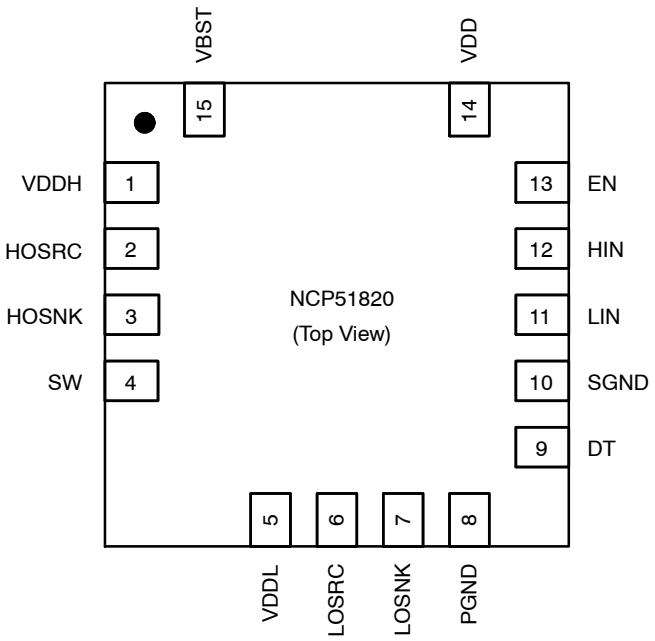

Figure 3. Pin Assignments – 15 Lead QFN (Top View)

PIN DESCRIPTION

Pin No.	Name	Description
1	VDDH	High−side driver positive bias voltage output
2	HOSRC	High−side driver sourcing output
3	HOSNK	High−side driver sinking output
4	SW	Switch−node / high−side driver return
5	VDDL	Low−side driver positive bias voltage output
6	LOSRC	Low−side driver sourcing output
7	LOSNK	Low−side driver sinking output
8	PGND	Power ground / low−side driver return
9	DT	Dead time adjustment / mode select
10	SGND	Logic / signal ground
11	LIN	Logic input for low−side gate driver output
12	HIN	Logic input for high−side gate driver output
13	EN	Logic input for disabling the driver (low power mode)
14	VDD	Bias voltage for high current driver
15	VBST	Bootstrap positive bias voltage

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ABSOLUTE MAXIMUM RATINGS (All voltages are referenced to SGND pin unless otherwise noted)

Symbol	Rating		Min	Max	Unit
V_{DD}	Low−side and logic−fixed supply voltage (PGND = SGND)		−0.3	20	V
V_{DDL}	Low−side supply voltage V_{DDL} (internally regulated; output only, do not connect to external voltage source, referenced to PGND)		−0.3	5.5	V
V_{SW}	High−side common mode voltage range (SW)		−3.5	650	V
V_{DDH}	High−side floating supply voltage V_{DDH} (internally regulated; output only, do not connect to external voltage source; referenced to SW)		−0.3	5.5	V
V_{BST_SGND}	High−side floating supply voltage V_{BST}		−0.3	670	V
V_{BST_SW}	High−side floating supply voltage V_{BST} (referenced to SW)		−0.3	20	V
V_{HOSRC}, V_{HOSNK}	High−side floating driver sourcing/sinking output voltage (referenced to SW)		−0.3	V_{DDH}+0.3	V
V_{PGND}	PGND voltage		−3.5	3.5	V
V_{LOSRC}, V_{LOSNK}	Low−side driver sourcing/sinking output voltage (referenced to PGND)		−0.3	V_{DDL}+0.3	V
V_{IN}	Logic input voltage (HIN, LIN, and EN)		−0.3	V_{DD}+0.3	V
V_{DT}	Dead−time control voltage (DT)		−0.3	V_{DD}+0.3	V
dV_{SW}/dt	Allowable offset voltage slew rate		–	200	V/ns
T_J	Operating Junction Temperature		–	150	°C
T_{STG}	Storage Temperature Range		−55	150	°C
	Electrostatic Discharge Capability	Human Body Model (Note 3)	–	1	kV
		Charged Device Model (Note 3)	–	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. V_{DD} − PGND voltage must not exceed 20 V
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001−2012
   ESD Charged Device Model tested per JESD22−C101.
4. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78 Class I.

THERMAL CHARACTERISTICS

Symbol	Rating		Value	Unit
θ_{JA}	Thermal Characteristics, QFN15 4x4 (Note 5) Thermal Resistance Junction−Ambient (Note 6)	IS0P	245	°C/W
		IS2P	188	
P_D	Power Dissipation (Note 6) QFN15 4x4 (Note 5)	IS0P	0.51	W
		IS2P	0.665	

5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
6. JEDEC standard: JESD51−2, JESD51−3. Mounted on 76.2×114.3×1.6 mm PCB (FR−4 glass epoxy material).
   IS0P: one single layer with zero power planes
   IS2P: one single layer with two power planes

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RECOMMENDED OPERATING CONDITIONS (All voltages are referenced to SGND pin unless otherwise noted)

Symbol	Rating	Min	Max	Unit
V_{DD}	Low−side and logic−fixed supply voltage	9	17	V
V_{SW}−SGND	SW−SGND maximum dc offset voltage (High−Side driver)	−	580	V
V_{BST}	High−side floating supply voltage V_{BST}	−	V_{SW}+17	V
V_{HOSRC}, V_{HOSNK}	High−side floating driver sourcing/sinking output voltage	−	V_{DDH}	V
V_{LOSRC}, V_{LOSNK}	Low−side driver sourcing/sinking output voltage	−	V_{DDL}	V
V_{IN}	Logic input voltage (HIN, LIN, and EN)	−	17	V
PGND−SGND	PGND−SGND maximum dc offset voltage (Low−Side driver)	−3.0	3.0	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{DD}, V_{BST}) = 15 V, DT = SGND = PGND and C_{LOAD} = 330 pF for typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, unless otherwise specified.) The V_{IN} and I_{IN} parameters are referenced to SGND. The V_O and I_O parameters are referenced to V_{SW} and PGND and are applicable to the respective outputs HOSRC, HOSNK, LOSRC, and LOSNK.

Symbol	Parameter	Test Conditions and Description	Min	Typ	Max	Unit
POWER SUPPLY SECTION (VDD)						
I_{QDD}	Quiescent V_{DD} supply current	V_{LIN} = V_{HIN} = 0 V, EN = 0 V	−	100	150	μA
I_{PDD}	Operating V_{DD} supply current	f_{LIN} = 500 kHz, average value	−	1.5	2.5	mA
V_{DDUV+}	V_{DD} UVLO positive going threshold	V_{DD} = Sweep	8.0	8.5	9.0	V
$V_{DDUV−}$	V_{DD} UVLO negative going threshold	V_{DD} = Sweep	7.5	8.0	8.5	V
V_{DDHYS}	V_{DD} UVLO Hysteresis	V_{DD} = Sweep	−	0.5	−	V
$t_{UVDDFLT}$	V_{DD} UVLO Filter Delay Time (Note 7)		−	5.3	−	μs
BOOTSTRAPPED POWER SUPPLY SECTION						
I_{LK}	Offset supply leakage current	V_{BST} = V_{SW} = 600 V	−	−	10	μA
I_{QBST}	Quiescent V_{BST} supply current	V_{LIN} = V_{HIN} = 0 V, EN = 5 V	−	35	100	μA
I_{PBST}	Operating V_{BST} supply current	f_{HIN} = 500 kHz, average value	−	1.5	2.5	mA
V_{BSTUV+}	V_{BST} UVLO positive going threshold	V_{DD} = 12 V	6.0	6.5	7.0	V
$V_{BSTUV−}$	V_{BST} UVLO negative going threshold	V_{DD} = 12 V	5.5	6.0	6.5	V
V_{HYST}	V_{BST} UVLO Hysteresis	V_{DD} = 12 V	−	0.5	−	V
GATE DRIVER POWER SUPPLY SECTION						
V_{DDH}	V_{DDH}−V_{SW} regulated voltage	0 mA < I_O < 10 mA	4.94	5.20	5.46	V
V_{DDL}	V_{DDL}−PGND regulated voltage		4.94	5.20	5.46	V
INPUT LOGIC SECTION (HIN, LIN and EN)						
V_{INH}	High Level Input Voltage Threshold		−	−	2.5	V
V_{INL}	Low Level Input Voltage Threshold		1.2	−	−	V
V_{IN_HYS}	Input Logic Voltage Hysteresis		−	0.5	−	V
I_{IN+}	High Level Logic Input Bias Current	V_{HIN} = V_{LIN} = 5 V	9	15	21	μA
$I_{IN−}$	Low Level Logic Input Bias Current	V_{HIN} = V_{LIN} = 0 V	−	−	2.2	μA
R_{IN}	Input Pull−down Resistance	V_{HIN} = V_{LIN} = 5 V	−	333	−	kΩ
DEAD−TIME SECTION						
$V_{DT,MIN}$	Minimum Dead−Time Control Voltage	R_{DT} = 30 kΩ	0.45	0.60	0.75	V
$t_{DT,MIN}$			22	30	38	ns

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ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{DD}, V_{BST}) = 15 V, DT = SGND = PGND and C_{LOAD} = 330 pF for typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, unless otherwise specified.) The V_{IN} and I_{IN} parameters are referenced to SGND. The V_O and I_O parameters are referenced to V_{SW} and PGND and are applicable to the respective outputs HOSRC, HOSNK, LOSRC, and LOSNK. (continued)

Symbol	Parameter	Test Conditions and Description	Min	Typ	Max	Unit
DEAD−TIME SECTION						
$V_{DT,MAX}$	Maximum Dead−Time Control Voltage	R_{DT} = 200 kΩ	3.1	4.0	4.8	V
$t_{DT,MAX}$			160	200	240	ns
Δt_{DT}	Dead−Time mismatch between LO → HO and HO → LO	R_{DT} = 30 kΩ	−	−	5	ns
		R_{DT} = 200 kΩ	−	−	10	ns
$V_{DT,0}$	Dead−Time Disable Threshold	Cross conduction prevention active	0.35	0.40	0.45	V
$V_{DT,OLE}$	High− & Low−Side Overlap Enable Threshold	Cross conduction prevention disabled	5.5	6.0	6.5	V
PROTECTION SECTION						
V_{UVTH_VDDX+}	UVLO Threshold on VDDH and VDDL positive going threshold		4.15	4.40	4.70	V
$V_{UVTH_VDDX−}$	UVLO Threshold on VDDH and VDDL negative going threshold		4.0	4.2	4.5	V
TSD	Thermal Shutdown (Note 7)		150	−	−	°C
hys	Hysteresis of Thermal Shutdown (Note 7)		−	50	−	°C
GATE DRIVE OUTPUT SECTION						
V_{OH}	High−level output voltage, V_{VDDH}−V_{HOSRC} or V_{VDDL}−V_{LOSRC}	I_{OSRC} = 10 mA	−	10	40	mV
V_{OL}	Low−level output voltage, V_{HOSNK}−V_{SW} or V_{LOSNK} −PGND	I_{OSNK} = 10 mA	−	5	20	mV
I_{OSRC}	Peak source current (Note 7)	C_{LOAD} = 200 pF, R_{gate} = 1 Ω	0.9	1.0	−	A
I_{OSNK}	Peak sink current (Note 7)	C_{LOAD} = 200 pF, R_{gate} = 1 Ω	1.8	2.0	−	A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design, is not tested in production.

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{DD}, V_{BST})=15 V, DT=SGND=PGND and C_{LOAD}=330 pF, for typical values T_A=25°C, for min/max values T_A=−40°C to +125°C, unless otherwise specified.) (Notes 9)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{QDD}	Quiescent V_{DD} supply current	V_{LIN} = V_{HIN} = 0 V, EN = 0 V	−	100	150	μA
t_{PDLON}	LOSRC turn−on propagation delay time	LIN rising to LOSRC rising (50% to 10%)	−	25	50	ns
t_{PDLOFF}	LOSNK turn−off propagation delay time	LIN falling to LOSNK falling (50% to 90%)	−	25	50	ns
t_{PDHON}	HOSRC turn−on propagation delay time	HIN rising to HOSRC rising (50% to 10%) SW = PGND	−	25	50	ns
t_{PDHOFF}	HOSNK turn−off propagation delay time	HIN falling to HOSNK falling (50% to 90%) SW = PGND	−	25	50	ns
t_{RL}	LOSRC turn−on rising time	SW = PGND	−	2	4	ns
t_{FL}	LOSNK turn−off falling time		−	1.5	3.0	ns
t_{RH}	HOSRC turn−on rising time		−	2	4	ns
t_{FH}	HOSNK turn−off falling time		−	1.5	3.0	ns

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DYNAMIC ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{DD}, V_{BST})=15 V, DT=SGND=PGND and C_{LOAD}=330 pF, for typical values T_A=25°C, for min/max values T_A=−40°C to +125°C, unless otherwise specified.) (Notes 9) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Δt_{DEL}	Propagation Delay match	HIN to HO and LIN to LO, SW = PGND	–	–	5	ns
t_{PW}	Minimum input pulse width		–	–	10	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. This parameter, although guaranteed by design, is not tested in production.
9. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C.

TIMING DIAGRAM

Shown in Figure 4 are the timing waveform definitions matching the specified dynamic electrical characteristics specified in the gate drive output section.

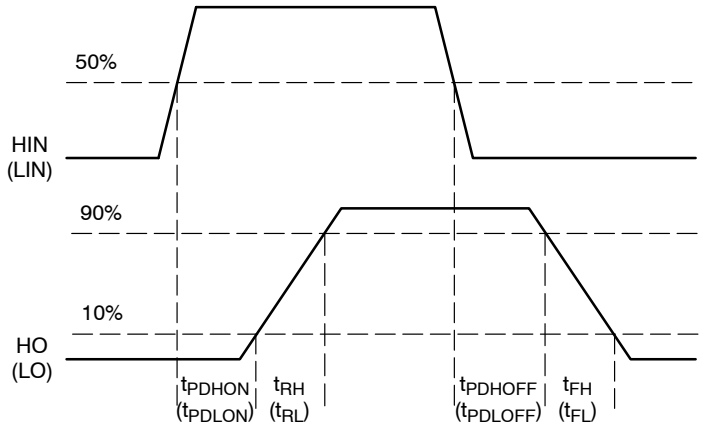

Figure 4. Input to Output Timing Diagram

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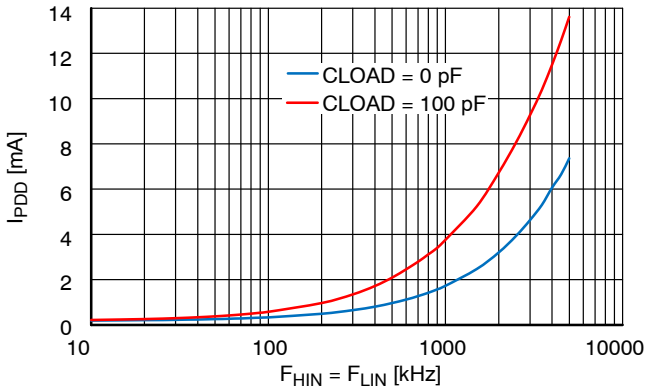

Figure 5. Operating VDD Supply Current (I_{PDD}) vs. Frequency (VDD = 12 V, SW = PGND, EN = VDD, Both Outputs Switching)

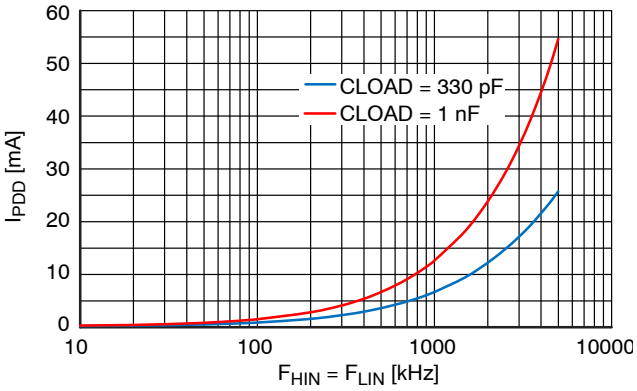

Figure 6. Operating VDD Supply Current (I_{PDD}) vs. Frequency (VDD = 12 V, SW = PGND, EN = VDD, Both Outputs Switching)

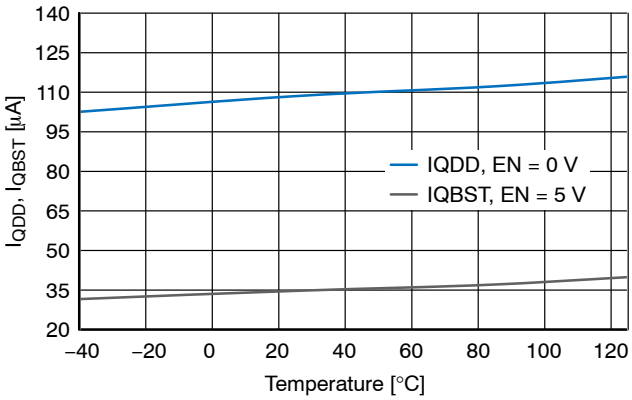

Figure 7. Quiescent Current (I_{QDD}, I_{QBST}) vs. Temperature

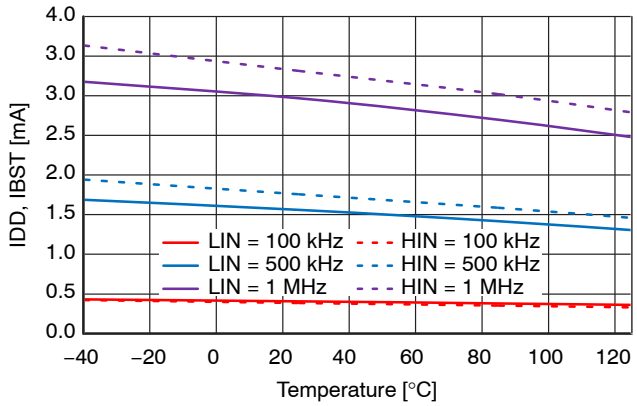

Figure 8. Operating Current (I_{PDD}, I_{PBST}) vs. Temperature

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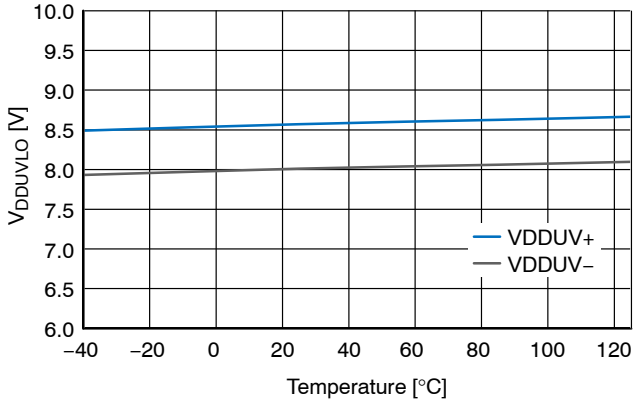

Figure 9. VDD UVLO ($V_{DDUVLO+}$, $V_{DDUVLO-}$) vs. Temperature

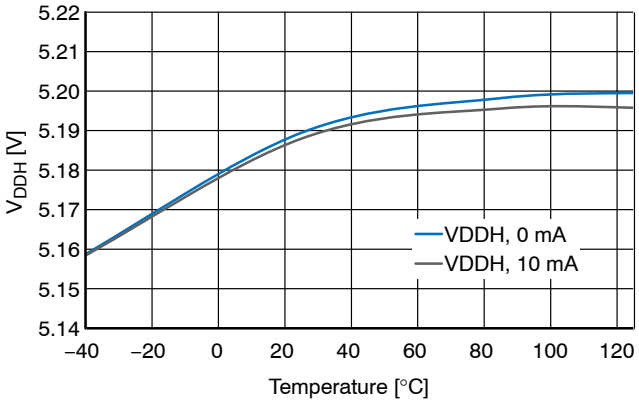

Figure 10. VDDH (V_{DDH}) Regulated Output Voltage vs. Temperature

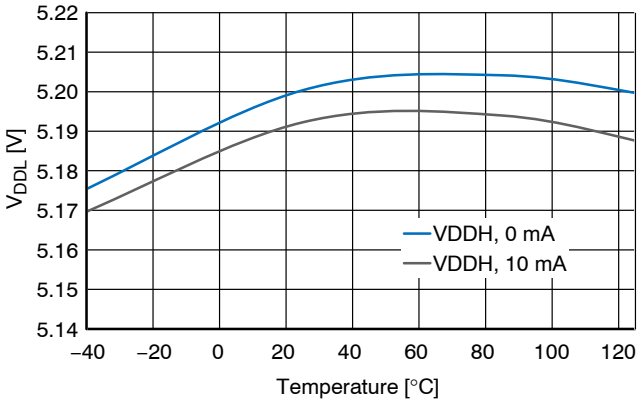

Figure 11. VDDL (V_{DDL}) Regulated Output Voltage vs. Temperature

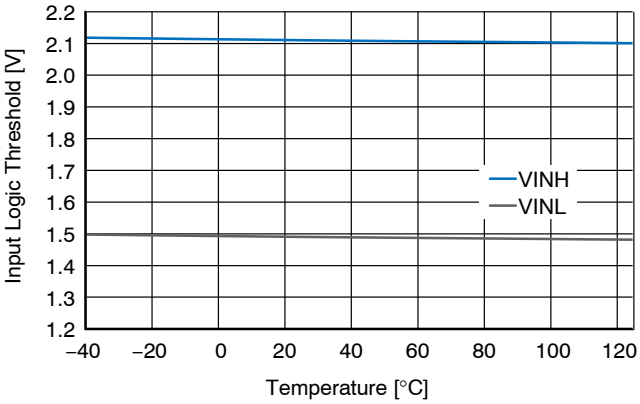

Figure 12. Input Logic (HIN, LIN, EN) Threshold vs. Temperature

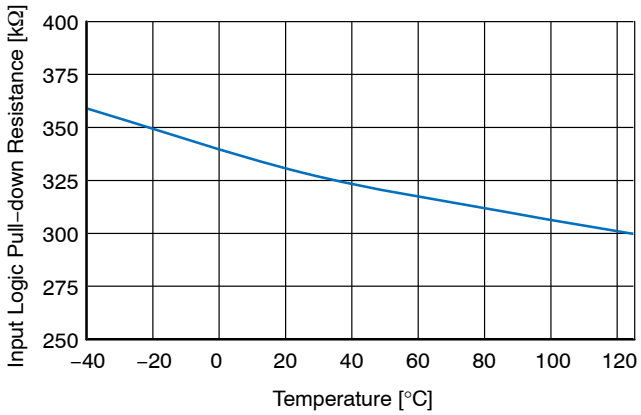

Figure 13. Input Logic (HIN, LIN, EN) Pull−down Resistance vs. Temperature

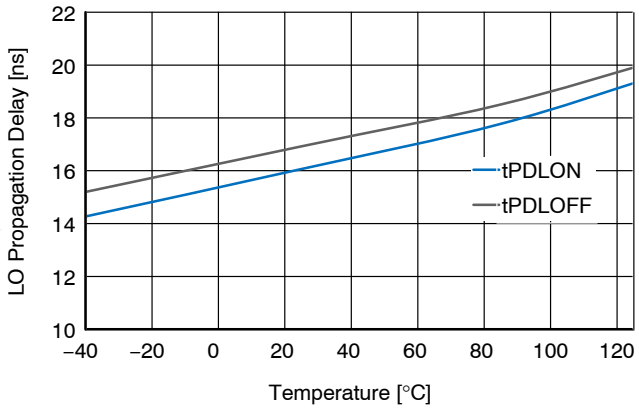

Figure 14. LIN to LOSRC Propagation Delay vs. Temperature

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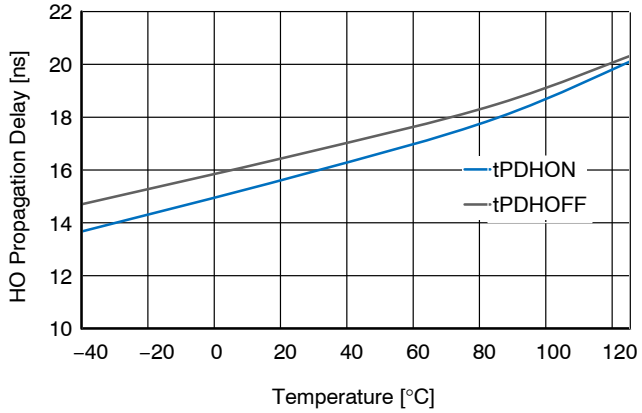

Figure 15. HIN to HOSRC Propagation Delay vs. Temperature

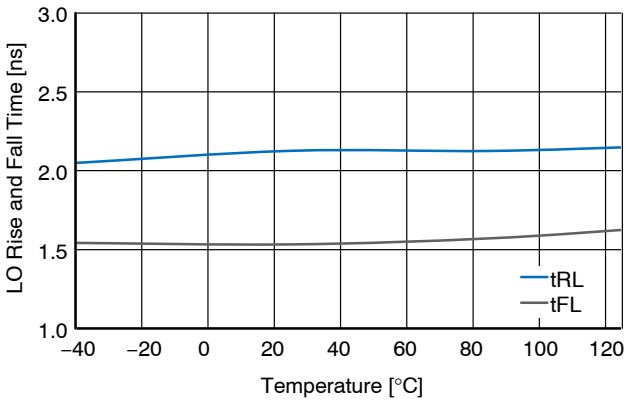

Figure 16. LOSRC Rise Time and LOSNK Fall Time vs. Temperature

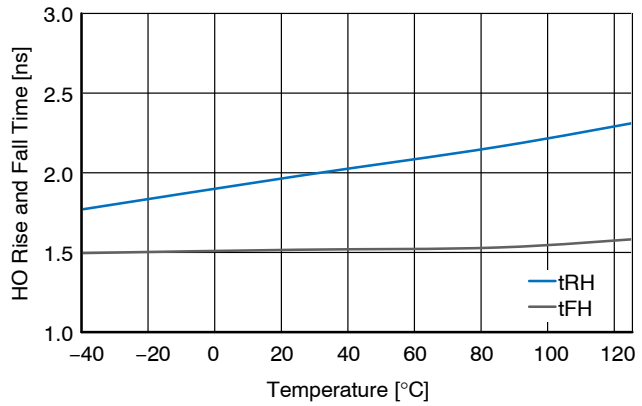

Figure 17. HOSRC Rise Time and HOSNK Fall Time vs. Temperature

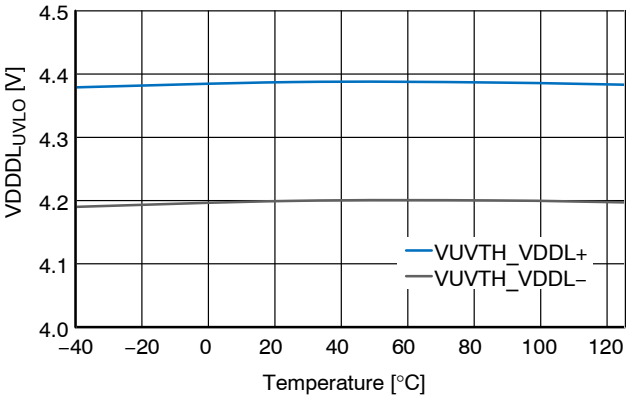

Figure 18. VDDL UVLO vs. Temperature

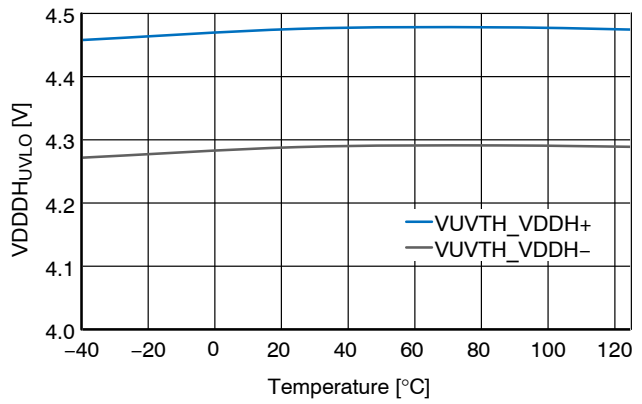

Figure 19. VDDH UVLO vs. Temperature

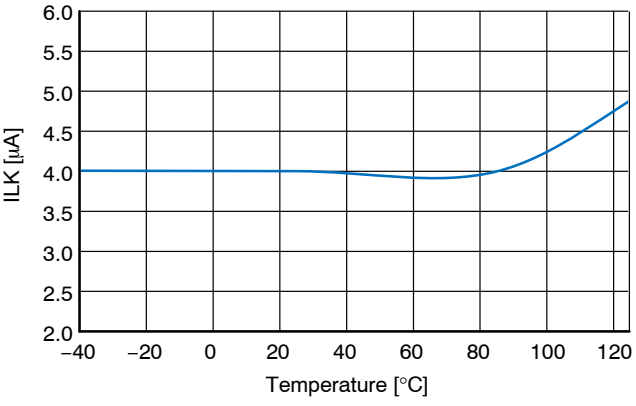

Figure 20. VBST Leakage Current (I_{LK}) vs. Temperature

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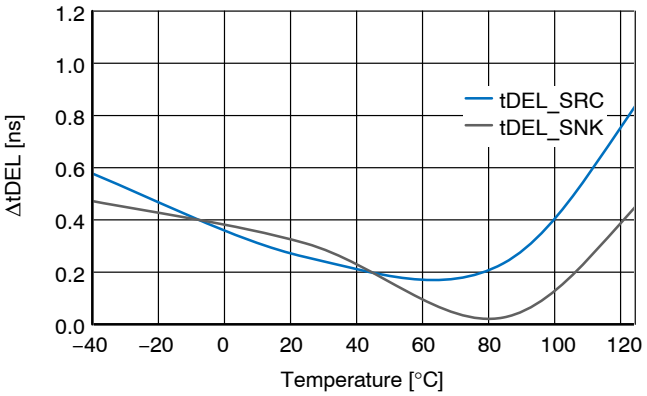

Figure 21. Propagation Delay Matching (HIN to HO, LIN to LO) vs. Temperature

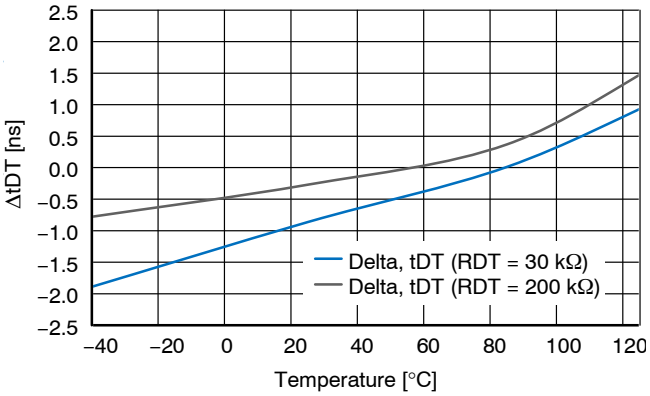

Figure 22. Dead−time Mismatch vs. Temperature

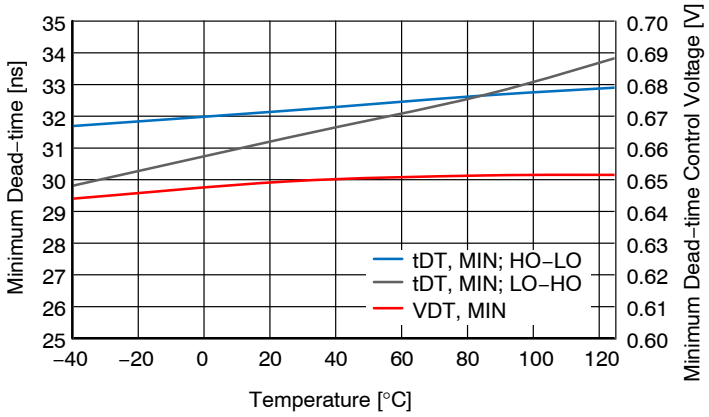

Figure 23. Minimum Dead−time (R_{DT} = 30 kΩ) vs. Temperature

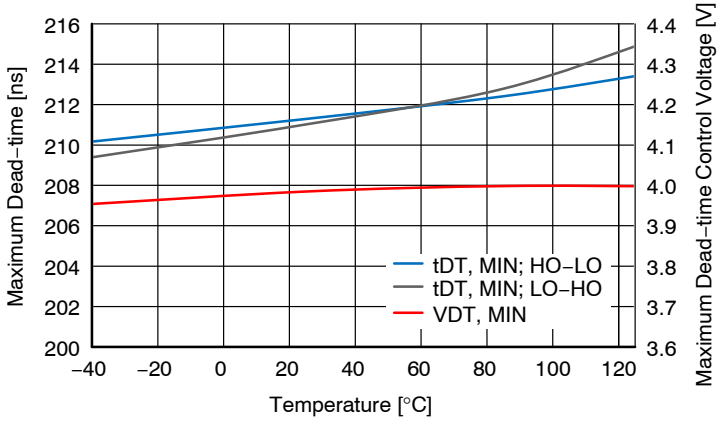

Figure 24. Maximum Dead−time (R_{DT} = 200 kΩ) vs. Temperature

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APPLICATIONS INFORMATION

The NCP51820 can be quickly configured by following the steps outlined in this section. The component references made throughout this section refer to the schematic diagram and reference designations shown in Figure 25.

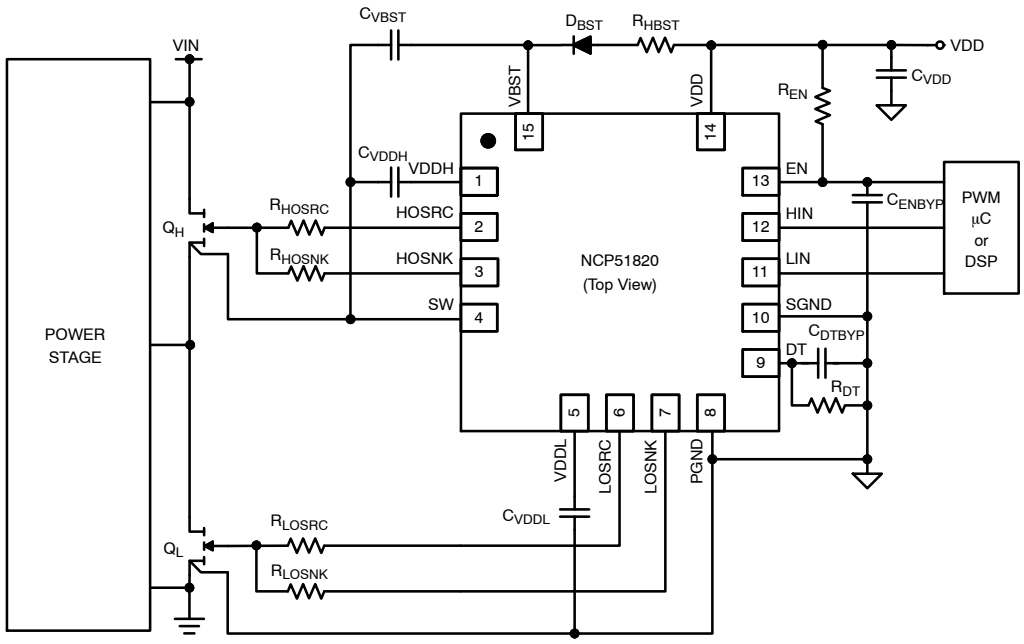

Figure 25. Application Schematic, Half−Bridge Example (Kelvin Gate Return Connections Shown)

DETAILED PIN FUNCTIONALITY

Bias Supply Voltage (VDD)

A dc voltage applied to VDD provides bias for the digital inputs, internal logic functions, high−side floating bootstrap (VBST) bias supplying the internal high−side regulator (VDDH) as well as providing bias directly to the internal low−side regulator (VDDL). Because the GaN FETs receive source current locally through the dedicated internal regulators, a single VDD bypass capacitor, C_{VDD}, is all that's required, connected directly between the VDD and SGND pins. The C_{VDD} capacitor should be a ceramic bypass capacitor > 100 nF, located as close as possible to the VDD and SGND pins to properly filter out all glitches while switching. Under voltage lockout (UVLO) is important for protecting the GaN FETs and power stage. The NCP51820 includes UVLO thresholds of V_{DDUV+} > 8.5 V, ON and V_{DDUV-} < 8 V, OFF, making it well suited for +12 V bias rails.

High−Side Bootstrap Voltage (VBST)

Three components make up the high side bootstrap voltage bias serving as the input to the VDDH regulator. The bootstrap current limiting resistor and diode, R_{BST} and D_{BST}, series connected between the VDD and VBST pins and the bootstrap capacitor, C_{VBST}, connected directly Switch node between VBST and (SW) pins. The VBST voltage is input to an internal LDO which produces the VDDH voltage. A large value for C_{VBST} means the bootstrap capacitor will take longer to fully charge as also determined by the on−time of the low−side GaN. Typically a higher value of C_{VBST} helps with better noise immunity and internal regulator stability. Neglecting the effects of parasitic inductance, the minimum value bootstrap capacitor can be approximated as:

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}} \quad \text{(eq. 1)}$$

Where:

Q_G = total gate charge required by GaN
ΔV_{BST} = VDD − V_{PP} − N$x V_F$ > 6 V
N = number of series diodes connected
V_{PP} = allowable V_{BST} droop voltage (typically less than 10% of VDD)
V_F = D_{BST} forward voltage drop

Choose a low ESR and ESL ceramic capacitor with a voltage rating of twice the applied voltage (2 x ΔV_{BST}). Once the bootstrap capacitor is selected, the peak charging current can be determined by knowing the frequency and duty cycle of the low−side gate drive.

$$I_{PK} = C_{BST} \times \frac{dV}{dt} = C_{BST} \times \frac{\Delta V_{BST} \times F_{SW}}{D_{MAX}} \quad \text{(eq. 2)}$$

Where:

D_{MAX} = Max duty cycle of low−side gate drive
F_{SW} = Switching frequency

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The bootstrap diode, D_{BST}, needs to have a voltage rating greater than VIN, should be high−speed (low reverse recovery), should be low current and should have very low junction capacitance. Diode junction capacitance, C_J, can become more problematic due to the high dV/dt that can appear across the GaN V_{DS}. Symptoms of high dV/dt switching can be mitigated by using a Kelvin source return to SW, as shown in Figure 25. Another method to reduce C_J is to use 2 or more diodes in series such that the sum of the total voltage ratings from each diode is greater than VIN. Each of the individual C_J's add reciprocally to reduce the total junction capacitance. The additional number of diode forward voltage drops must also be accounted for when calculating C_{BST}.

The purpose of the bootstrap resistor, R_{BST}, is to limit peak C_{BST} charging current, I_{PK}, especially during startup. A small resistor may not limit the peak current enough, resulting in excessive ringing which can cause jitter in the high−side gate drive and/or EMI problems. A large resistor will dissipate more power and create a longer RC time constant causing a longer start−up time. A bootstrap resistor in the range of 1 Ω < R_{BST} < 10 Ω is usually sufficient.

High−Side Linear Regulator (VDDH)

The NCP51820 includes an internal linear regulator dedicated to providing a tightly regulated, 5.2 V gate drive amplitude signal to the high−side GaN FET. The VDDH regulator appears after the bootstrap, providing the most direct interface to the high−side GaN FET. This assures the lowest possible parasitic capacitance, required for meeting high−speed switching requirements of GaN. The VDDH regulator is referenced between VDDH and the SW pins and can float between a common mode voltage range of −3.5 V up to 650 V. Source current for the high−side GaN FET is provided from the charge stored in C_{VDDH} connected between VDDH and SW. The value of the C_{VDDH} capacitor is a function of the gate charge requirement of the GaN FET. C_{VDDH} should be chosen such that C_{VBST} > 10*C_{VDDH}, ie If C_{VBST} is 1 μF, C_{VDDH} should be less than 100 nF. The VDDH regulator also includes dedicated UVLO thresholds of V_{UVTH_VDDH+} > 4.5 V, ON and $V_{UVTH_VDDH−}$ < 4.3 V, OFF.

Switch Node (SW)

The SW pin serves as the high−side, gate drive, return reference. As shown in Figure 2, the high−side level shifter, drive logic, PMOS sink and VDDH regulator are referenced to SW. For GaN FETs that include a source Kelvin return, a direct connection should be made from SW to the GaN FET Kelvin return. C_{VDDH} and C_{BST} should then be referenced to the SW pin but separate from the power stage switch node as shown in Figure 25. For GaN FETs that do not include a dedicated source Kelvin pin, best practice PCB layout techniques should be used to isolate the gate drive return current from the power stage, switch node current. Please refer to document AND9932, for NCP51820 and high−speed GaN, PCB layout tips.

Low−Side Linear Regulator (VDDL)

The NCP51820 includes an internal linear regulator dedicated to providing a tightly regulated, 5.2 V gate drive amplitude signal to the low−side GaN FET. The VDDL regulator is fed directly from VDD, providing the most direct interface to the low−side GaN FET. This assures the lowest possible parasitic capacitance, required for meeting high−speed switching requirements of GaN. The VDDL regulator is referenced between VDDL and the power ground (PGND) pins and is capable of operating from common mode voltage range between −3.5 V to +3.5 V. Source current for the low−side GaN FET is provided from the charge stored in the C_{VDDL} connected between VDDL and PGND. The value of the C_{VDDL} capacitor is a function of the gate charge requirement of the low−side GaN FET. C_{VDDL} should be chosen such that CVDD > 10*C_{VDDL}, ie if C_{VDD} cap 1 μF, C_{VDDL} should be less than 100 nF. The VDDL regulator also includes dedicated UVLO thresholds of V_{UVTH_VDDL+} > 4.5 V, ON and $V_{UVTH_VDDL−}$ < 4.3 V, OFF.

Signal Ground (SGND) and Power Ground (PGND)

SGND is the GND for all internal control logic and digital inputs. Internally, the SGND and PGND pins are isolated from each other.

PGND serves as the low−side, gate drive, return reference. As shown in Figure 2, the low−side level shifter, drive logic, PMOS sink and VDDL regulator are referenced to PGND. For GaN FETs that include a source Kelvin return, a direct connection should be made from PGND to the GaN FET Kelvin return. C_{VDDL} should then be referenced to the PGND but separate from the power stage ground as shown in Figure 25. For GaN FETs that do not include a dedicated source Kelvin pin, best practice PCB layout techniques should be used to isolate the gate drive return current from the power stage, ground return current. Please refer to document AND9932, for NCP51820 and high−speed GaN, PCB layout tips.

For half−bridge power topologies or any applications using a current sense transformer, SGND and PGND must be connected together on the PCB. In such applications, it is recommended to connect the SGND and PGND pins together with a short, low−impedance trace on the PCB as close to the NCP51820 as possible. Directly beneath the NCP51820 is an ideal way to make the SGND to PGND connection.

For low−power applications, such as the active−clamp flyback or forward shown in Figure 26, a current sensing resistor, R_{CS}, located in the low−side GaN FET source leg is commonly used. In such applications, the NCP51820 PGND and SGND pins must not be connected on the PCB because R_{CS} would essentially be shorted through this connection. The NCP51820 low−side drive circuit is able to withstand −3.5 V to +3.5 V of common mode voltage. Since most current sense voltage signals are less than 1 V, the low−side drive stage can easily "float" above the voltage,

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V_{RCS}, generated by the current sense. For the active clamp example in Figure 26, the entire low−side gate drive, shown in the shaded box, is floating above V_{RCS}. This is important because it ensures no loss of gate drive amplitude so the full 5.2 V, VDDL voltage appears at the low−side GaN FET gate−source terminals. A low impedance current sense resistor is recommended. Please refer to document AND9932, for NCP51820 and high−speed GaN, PCB layout tips.

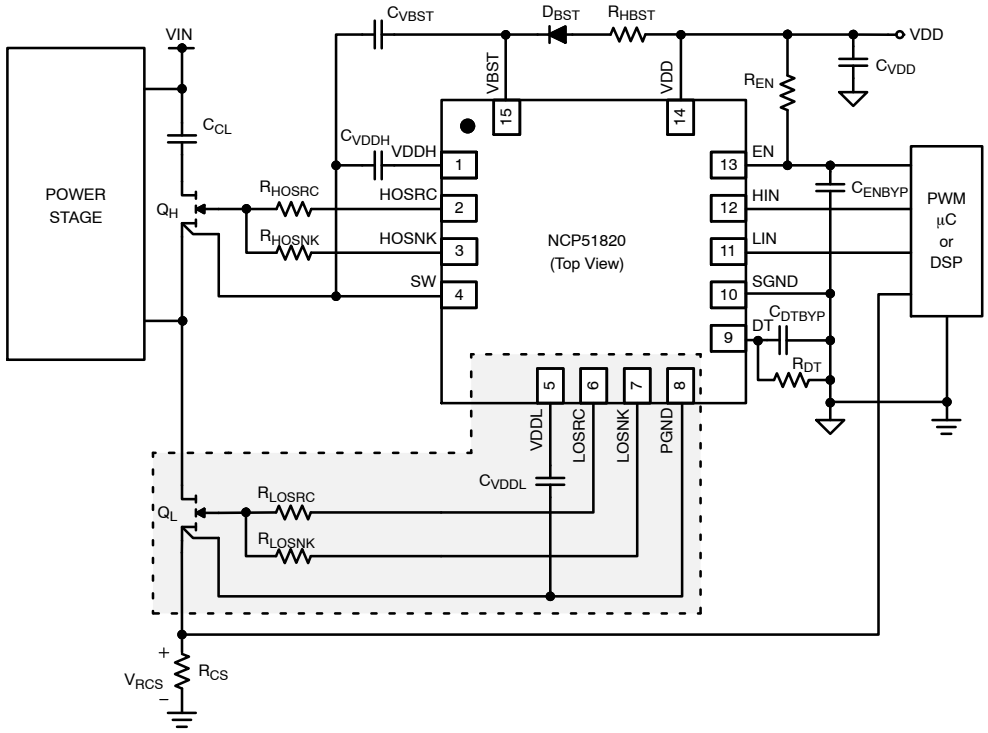

Figure 26. Application Schematic, Active Clamp, Low−Side, Floating Gate Drive Example

Input (HIN, LIN)

Both independent PWM inputs are Schmitt trigger, Transistor−Transistor Logic (TTL) compatible and are internally pulled low to SGND such that each corresponding driver input is defaulted to the inactive (disabled) state. The TTL input thresholds provide buffer and logic level translation functions capable of operating from a variety of PWM signals up to VDD of the NCP51820. TTL levels permit the inputs to be driven from a range of input logic signal levels for which a voltage greater than 2.5 V maximum is considered logic high. Both input thresholds meet industry−standard, TTL−logic defined thresholds and are therefore independent of V_{DD} voltage. A typical hysteresis voltage of 0.5 V is specified for each driver input. For optimal high−speed switching performance, the driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/µs or faster, so a rise time from 0 to 3.3 V should be 550 ns or less.

Enable (EN)

Enable (EN) is internally pulled low to SGND so the driver is always defaulted to a disabled output status. Similar to HIN and LIN, EN is a Schmitt trigger TTL compatible input. Pulling the EN pin above 2.5 V maximum, enables the outputs, placing the NCP51820 into an active ready state. Due to the nature of high−speed switching associated with GaN power stages, and for improved noise immunity, it is recommended to connect the EN pin to VDD through a 1 kΩ (or less) pull−up resistor. For applications where the EN pin is actively controlled, the EN pin can be driven direct but should be bypassed with a 10 nF decoupling capacitor. As shown in Figure 27, if EN is pulled low during normal operation, the driver outputs are immediately disabled, even terminating an active HIN or LIN pulse mid –cycle during the on−time. When EN is toggled high, during normal operation, a cycle−by−cycle, edge−triggered logic function is employed to prevent shortened, erroneous control pulses from being processed by the output. This behavior is highlighted in Figure 27, where EN transitions high at the same time the HIN (or LIN) input pulse is high. In this way, the NCP51820 is intelligent by waiting until the next rising edge to process the full input signal to the output driver stage.

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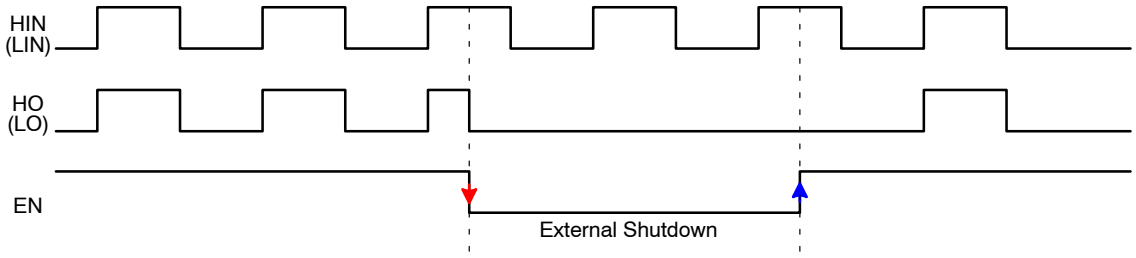

Figure 27. Timing Chart of Enable Function

Dead−Time Control (DT)

Accurately ensuring some minimal amount of dead−time between the high−side and low−side gate drive output signals is critical for safe, reliable optimized operation of any high−speed, half−bridge power stage. The DT should be bypassed with a 100 nF (C_{DTBYP}) ceramic capacitor placed closest to the pin and directly between DT and SGND. If used, the R_{DT} resistor should then be placed directly in parallel with C_{DTBYP}. The NCP51820 offers four unique mode settings to utilize dead−time in such a way to be fully compatible with any control algorithm.

MODE A:

Connect DT to SGND; When the DT pin voltage, V_{DT}, is less than 0.5 V typical (R_{DT} = 0 Ω), the DT programmability is disabled and fixed dead−time, anti−cross−conduction protection is enabled. If HIN and LIN are overlapping by X ns, then X ns of dead−time is automatically inserted. Conversely, if HIN and LIN have greater than 0 ns of dead−time, then the dead−time is not modified by the NCP51820 and is passed through to the output stage as defined by the controller. This type of dead−time control is preferred when the controller will be making the necessary dead−time adjustments but needs to rely on the NCP51820 dead−time control function for anti−cross−conduction protection.

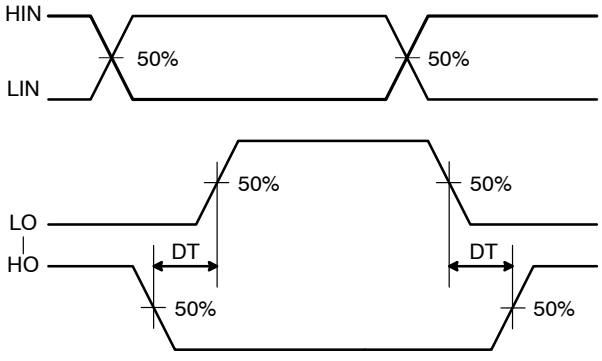

Figure 28. Internal Dead−Time Definitions

MODE B:

Connect a 25 kΩ < R_{DT} < 200 kΩ Resistor from DT to SGND; Dead−time is programmable by a single resistor connected between the DT and SGND pins. The amount of desired dead−time can be programmed via the dead−time resistor, R_{DT}, between the range of 25 kΩ < R_{DT} < 200 kΩ to obtain an equivalent dead−time, proportional to R_{DT}, in the range of 25 ns < t_{DT} < 200 ns. If either edge between HIN and LIN result in a dead−time less than the amount set by R_{DT}, the set DT value shall be dominant. If either edge between HIN and LIN result in a dead−time greater than the amount set by R_{DT}, the controller dead−time shall be dominant. The control voltage range, V_{DT}, for R_{DT} is 0.5 V < V_{DT} < 4 V. DT programmability is summarized and shown graphically in Figure 29.

MODE C:

Connect a 249 kΩ Resistor from DT to SGND; Connect a 249 kΩ resistor between DT and SGND to program the maximum dead−time value of 200 ns. The control voltage range, V_{DT}, for assuring t_{DT} = 200 ns is 4 V < V_{DT} < 5 V. DT programmability is summarized and shown graphically in Figure 29.

MODE D:

Connect DT to VDD; When the DT pin voltage, V_{DT}, is greater than 6 V (pulled up to VDD through 10 kΩ resistor), anti−cross−conduction protection is disabled, allowing the output signals to overlap. This operating mode is suitable for applications where it is desired to have both driver output stages switching simultaneously. If choosing this operating mode while driving a half−bridge power stage, extreme caution should be taken, as cross conduction can potentially damage power components if not accounted for. This type of dead−time control is preferred when the controller will be making extremely accurate dead−time adjustments and can respond to the potential of over−current faults on a cycle−by−cycle basis. DT programmability is summarized and shown graphically in Figure 29.

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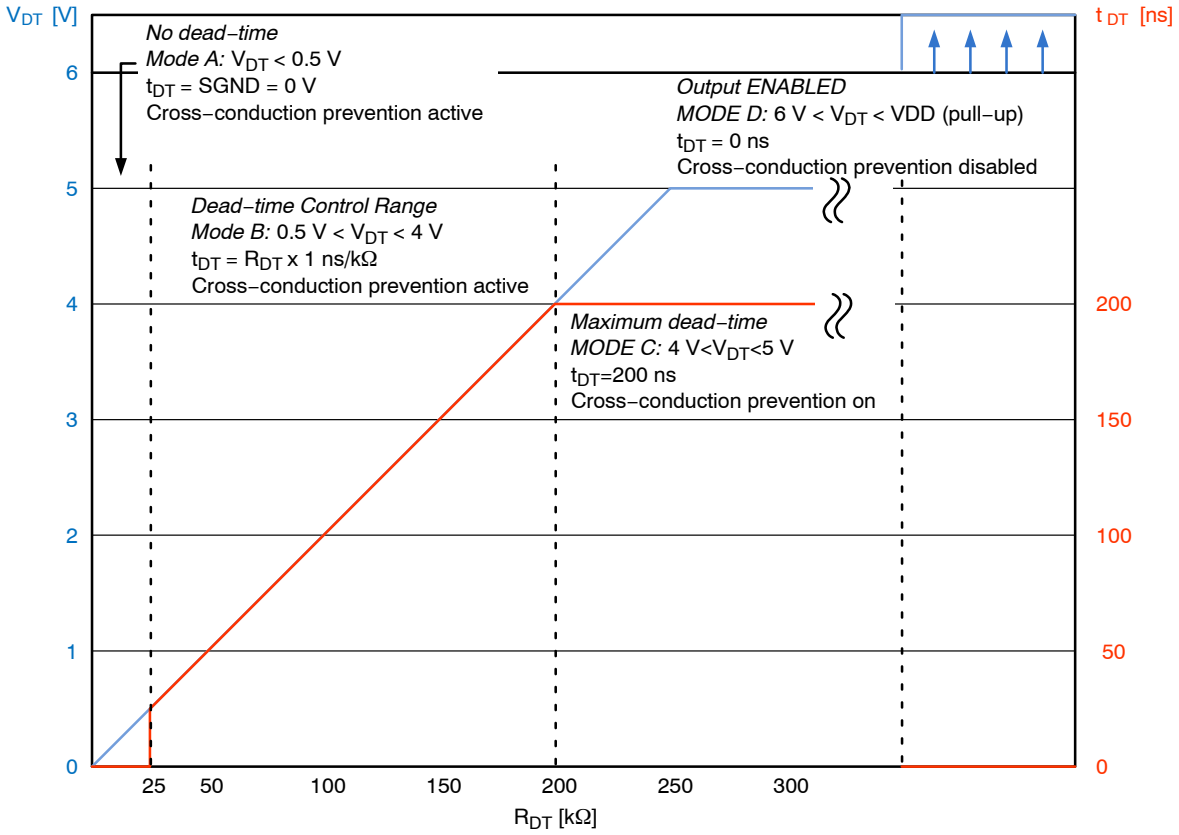

Figure 29. Dead−Time Control, t_{DT}, V_{DT} vs R_{DT}

High−Side Output (HOSRC and HOSNK)

The NCP51820 high−side drive stage is level shifted from HIN and SGND and referenced to SW and can withstand a common mode voltage range from −3.5 V to +650 V. HOSRC and HOSNK outputs are driven by a pure MOS, low−impedance totem pole output stage to ensure tightly regulated, low stray capacitance, full VDDH switching. The output slew rate is determined primarily by VDDH and the Q_G of the high−side GaN FET. The turn−on (HOSRC) and turn−off (HOSNK) functions each have dedicated pins. This allows a single resistor between each pin and the high−side GaN FET gate to independently control gate ringing as well as fine tuning dV_{DS}/dt turn−on and turn−off transitions present on the GaN drain−source voltage. The driver provides the high peak currents necessary for high−speed switching, even at the Miller plateau voltage. The outputs of the NCP51820 are rated to 1 A peak current source (HOSRC) and 2 A sink (HOSNK).

Low−Side Output (LOSRC and LOSNK)

The NCP51820 low−side drive stage is level shifted from LIN and SGND and referenced to PGND and can withstand a common mode voltage range from −3.5 V to +3.5 V. LOSRC and LOSNK outputs are driven by a pure MOS, low−impedance totem pole output stage to ensure tightly regulated, low stray capacitance, full VDDL switching. The output slew rate is determined primarily by VDDL and the Q_G of the low−side GaN FET. The turn−on (LOSRC) and turn−off (LOSNK) functions each have dedicated pins. This allows a single resistor between each pin and the low−side GaN FET gate to independently control gate ringing as well as fine tuning dV_{DS}/dt turn−on and turn−off transitions present on the GaN drain−source voltage. The driver provides the high peak currents necessary for high−speed switching, even at the Miller plateau voltage. The outputs of the NCP51820 are rated to 1 A peak current source (LOSRC) and 2 A sink (LOSNK). The high−side and low−side drive stage can be thought of as two independent floating driver channels. Both driver output channels are perfectly suited for driving the latest generation HEMT GIT GaN FETs which require constant current into the internal gate clamp or HEMT GaN FETs which are strictly unclamped, voltage controlled devices requiring tightly regulated gate drive signals.

INPUT TO OUTPUT PROTECTION FUNCTIONS

Figure 30 graphically summarizes the input to output protection functions for the following three cases:

Case A:

External shutdown due to EN pulled low. Outputs are immediately terminated when EN is pulled low. The second rising edge of either HIN or LIN is processed to the output when EN is pulled high.

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Case B:

UVLO protection event during shutdown and start−up. Crossing the UVLO ON and OFF thresholds has the same effect as EN, where outputs are immediately terminated when UVLO OFF is reached. The second rising edge of either HIN or LIN is processed to the output when UVLO ON is reached.

Case C:

Anti−cross−conduction, shoot−through protection. As described in the DT section MODE A, when the DT pin is connected SGND, any amount of HIN to LIN overlap is translated to HO to LO dead−time.

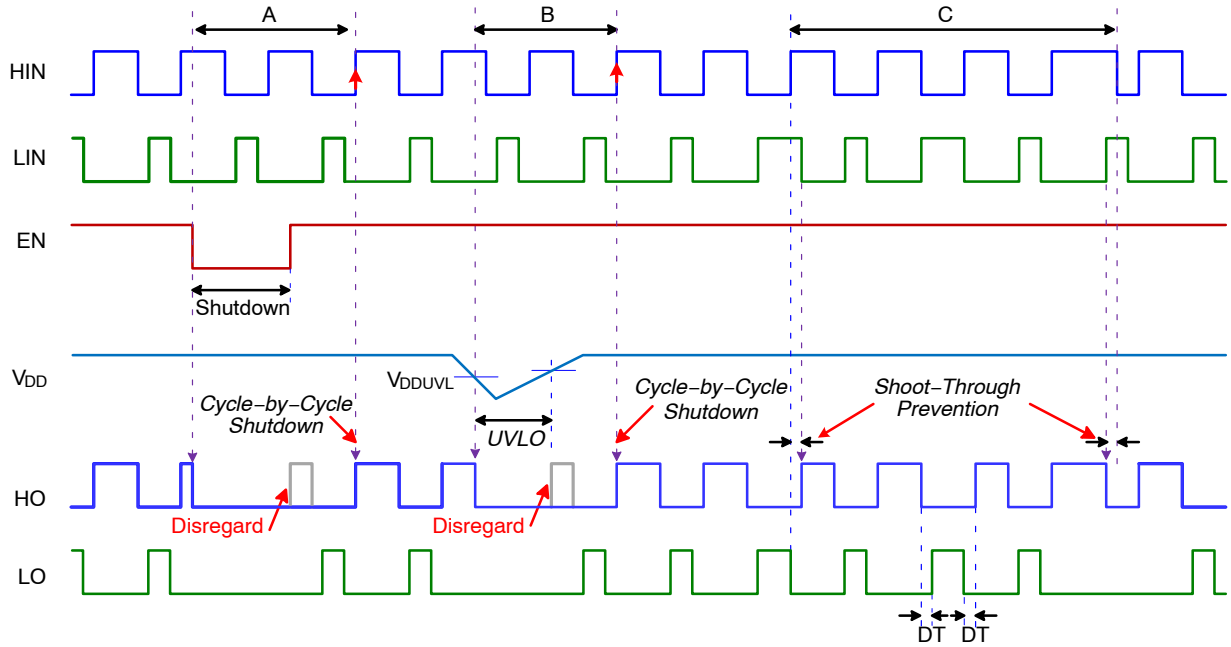

Figure 30. Protection Functions, Timing Diagram

PCB LAYOUT

When beginning a PCB design using GaN FETs, the best layout procedure is one that is priority−driven as listed below. Each of these "summary" comments are highlighted in more detail with clarifying diagrams in document AND9932, NCP51820 and high−speed GaN, PCB layout tips.

1. Multi−layer PCB designs with proper use of ground/return planes as described in this document are a must. High frequency, high voltage, high dV/dt and high di/dt all warrant the need for a multi−layer, PCB design approach. Inexpensive, single−layer, PCB designs do not allow for proper routing or design of ground planes necessary to realize the full benefits of a GaN based power stage.
2. Begin by placing the most noise sensitive components near the NCP51820 first. VDD, VDDH, VDDL, EN and DT bypass capacitors as well as the VBST capacitor, resistor and diode should be placed as close to their respective pins as possible.
3. Place the DT resistor directly next to C_{DTBYP} and the DT and SGND pins.
4. Place the HO and LO, source and sink gate drive resistors as close to the GaN FETs as possible.
5. Move the NCP51820 and associated components close to the GaN FET source and sink resistors.
6. If possible, arrange the GaN FETs in a "staggered" pattern with the goal of maintaining the HO and LO gate drive lengths as closely matched as possible. To avoid high current and high dV/dt through vias, it is preferred that both GaN FETs be located on the same side of the PCB as the NCP51820.
7. The HO and LO gate drives should be considered as two independent gate drive circuits that are electrically isolated from each other. HO and LO will therefore each require dedicated copper land return planes on layer 2 directly beneath layer 1 gate drive routing.

Proper routing of the power loop, switch−node, gate drive loops and use of planes are critical for a successful GaN PCB design. For the gate drives, proper routing and noise isolation will help reduce additional parasitic loop inductance, noise injection, ringing, gate oscillations and inadvertent turn−on. The goal is to design a high frequency, power PCB that is thoughtful with regard to proper grounding while maintaining controlled current flow through direct pathway connections with minimal loop distances.

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COMPONENT PLACEMENT AND ROUTING

The diagram shown in Figure 31 highlights the critical component placement around the NCP51820 and the interface to the HS and LS GaN FETs. The strategic placement of critical components around the NCP51820, use of dedicated ground and return planes, Kelvin source connections and direct gate drive routing are discussed in detail in document AND9932, NCP51820 and high−speed GaN, PCB layout tips.

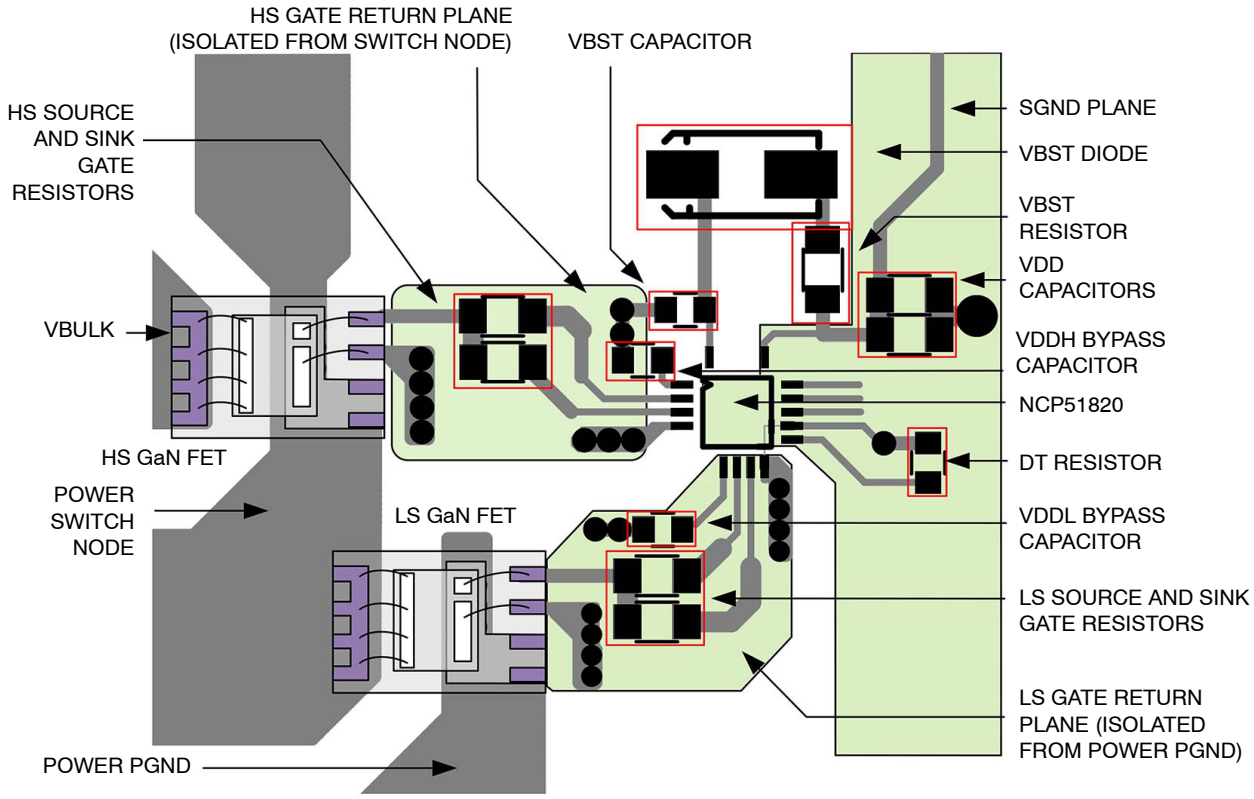

Figure 31. NCP51820 Component Placement

THERMAL GUIDELINES

High−speed, gate drivers used to switch GaN FETs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure the IC is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components, P_{GATE} and $P_{DYNAMIC}$:

$$P_{TOTAL} = 2 \times P_{GATE} + P_{DYNAMIC} \quad \text{(eq. 3)}$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the GaN FETs on and off at the switching frequency. The power dissipation that results from driving a GaN FET with a specified gate−source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, F_{SW}, is determined by:

$$P_{GATE} = Q_G \times V_{GS} \times F_{SW} \quad \text{(eq. 4)}$$

This needs to be calculated for the high−side and low−side GaN FETs where the Q_G can possibly be different if the devices are not the same

Dynamic Predrive / Shoot−through Current: Power loss resulting from internal current consumption under dynamic operating conditions can be obtained using the "I_{PDD} vs. Frequency" graphs in Figure 5 and Figure 6 to determine the current, I_{PDD} flowing from V_{DD} under actual operating conditions.

$$P_{DYNAMIC} = I_{PDD} \times V_{DD} \quad \text{(eq. 5)}$$

Once the power dissipated in the driver is determined, the driver junction temperature rise with respect to the PCB can be evaluated using the thermal equation, given below:

$$T_J = (P_{TOTAL} \times \theta_{JA}) + T_B \quad \text{(eq. 6)}$$

Where:

T_J = driver junction temperature
θ_{JA} = thermal characterization parameter relating temperature rise to total power dissipation
T_B = board temperature in location defined

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As an example, consider an application driving two GaN FETs with a gate charge of 5 nC each with V_{DD} = 12 V (V_{DDH} = V_{DDL} = 5.2 V). At a switching frequency of 500 kHz, the total power dissipation is:

$$P_{GATE} = 5\ nC \times 5.2\ V \times 500\ kHz \times 2 = 26\ mW \quad \text{(eq. 7)}$$

$$P_{DYNAMIC} = 4\ mA \times 12\ V = 48\ mW \quad \text{(eq. 8)}$$

$$P_{TOTAL} = 74\ mW \quad \text{(eq. 9)}$$

The QFN15 4x4 package has a junction−to−ambient thermal characterization parameter of θ_{JA} = 245°C/W. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must not exceed the absolute maximum rating of 150°C; with 80% derating, T_J would be limited to 120°C. Rearranging Equation 6 determines the board temperature required to maintain the junction temperature below 120°C:

$$T_B = T_J - (P_{TOTAL} \times \theta_{JA}) \quad \text{(eq. 10)}$$

$$T_B \leq 120°C - (74\ mW \times 245°C/W) = 102°C \quad \text{(eq. 11)}$$

Similarly, eq. 6 can be used to calculate the junction temperature (operating near room temperature) as:

$$T_J = (74\ mW \times 245°C/W) + 25°C \quad \text{(eq. 12)}$$

$$T_J = 43.13°C \quad \text{(eq. 13)}$$

IMPACT IONIZATION CURRENT

NCP51820 tends to exhibit an Impact Ionization current that flows from the boot pin (VB) to ground (GND) under certain conditions. This happens when voltage on the bridge pin (HB) is less than 40 V for a time greater than 100 μs and that is immediately followed by switching event that pulls−up the HB pin above 150 V. This current can potentially last multiple switching cycle before it diminishes. Furthermore, Impact Ionization current is not seen in systems where the bulk voltage is always below 150 V i.e., HB node is never pulled above 150 V, for instance, a 48 V to 12 V full−bridge power converter.

Figure 1 below shows an example of Impact Ionization current. This example shows a half−bridge converter running at 100 kHz frequency with 3 μs on−time. It shows Impact Ionization current flowing in first three pulses during startup and subsiding thereafter.

Depending on the duration and magnitude of the Impact Ionization current it can lead to thermal stress on the device which can potentially, in corner cases, cause a thermal failure of NCP51820.

Following are the safe conditions under which the Impact Ionization current doesn't occur:

1. Systems where VHB < 150 V and VBOOT < 170 V.
   OR
2. Systems where VHB > 40 V before the start of switching
   OR
3. Further, if the dv/dt of the VHB is kept under 0.1 V/ns, then the Impact Ionization current substantially reduces.

Mitigating Impact Ionization Current in Various Topologies

- Flyback Converters and derivatives: Any topologies based on flyback or derivatives (DCM/CCM Flyback, Active Clamp Flyback, and AHB Flyback) do not show any Impact Ionization current. This is because that transformer in the flyback topology is connected to input directly hence the VHB at t = 0 is at input voltage (> 40 V) satisfying the second conditioned mentioned above.
- Synchronous Boost Converter: Similar to flyback the VHB at t=0 is at input voltage (> 40 V) so no Impact Ionization current flows.
- Phase Shifted Full−bridge: The HB pin can be potentially at less than 40 V when switching starts. This can cause Impact Ionization current to flow during startup and in burst mode. This can be mitigated by adding parallel resistors (>1Meg) across the FETs. Parallel resistors ensure that the switch node voltage is at a voltage greater than 40 V before the switching starts.
- High Voltage Synchronous Buck Converter: Synchronous buck presents the worst case for the Impact Ionization current. The HB is at a voltage equal to output voltage always at t= 0. Hence at the startup or in the cases of burst mode we see Impact Ionization current when the Vout < 40 V. One potential solution can be pre−charging the output with VCC through a diode and running the system in soft−switching from first pulse itself. However if the regulated Vout is less than 40 V then there is a chance of Impact Ionization current every burst cycle.
  But as explained earlier this occurs only in case of HV systems. When the bulk voltage is less than 150 V no Impact Ionization current is seen.

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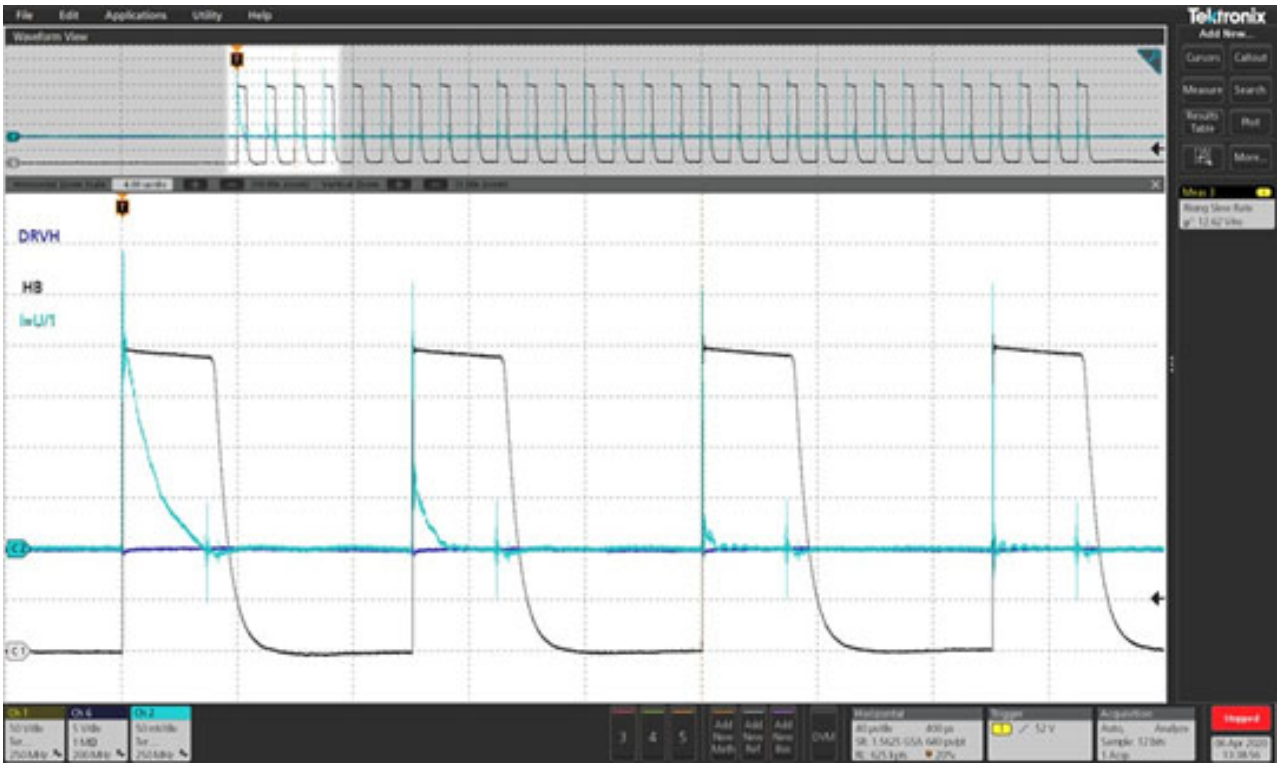

Figure 32. 1 Impact Ionization Current in NCP51820. C1 is HB Node at 50 V/div and C2 is Impact Ionization Current at 50 mA/div

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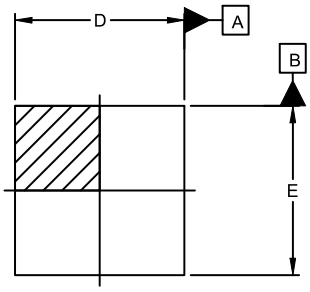
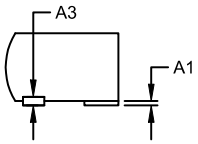
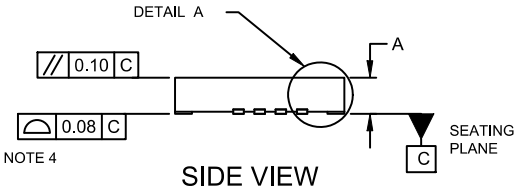


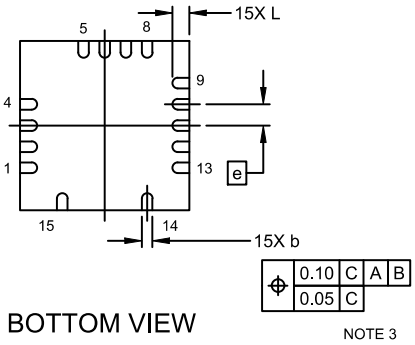
TOP VIEW



DETAIL A



SIDE VIEW

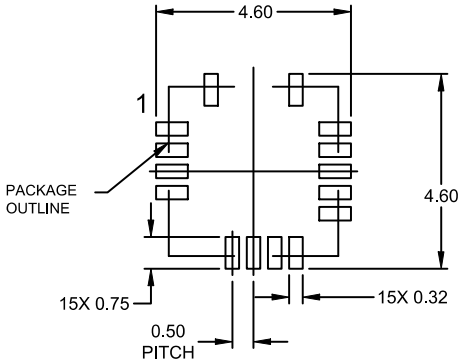


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

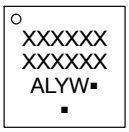
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	---	0.05
A3		0.10 REF	
b	0.20	0.25	0.30
D	3.95	4.00	4.05
E	3.95	4.00	4.05
e		0.50 BSC	
L	0.30	0.40	0.50



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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