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AP0100AT2L00XUGAH3-GEVB

AP0100AT Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of ON Semiconductor's image sensors products. This headboard is intended to plug directly into the Demo 3 system. Test points and jumpers on the board provide access to the clock, I/Os, and other miscellaneous signals.

Features

- Clock Input
  - Default – 27 MHz Crystal Oscillator
  - Optional Demo 3 Controlled MClk
- Two Wire Serial Interface
- Parallel Interface
- HiSPi (High Speed Serial Pixel) Interface
- ROHS Compliant

Block Diagram

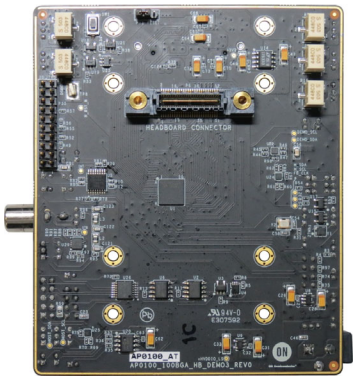

Figure 1. AP0100AT Evaluation Board

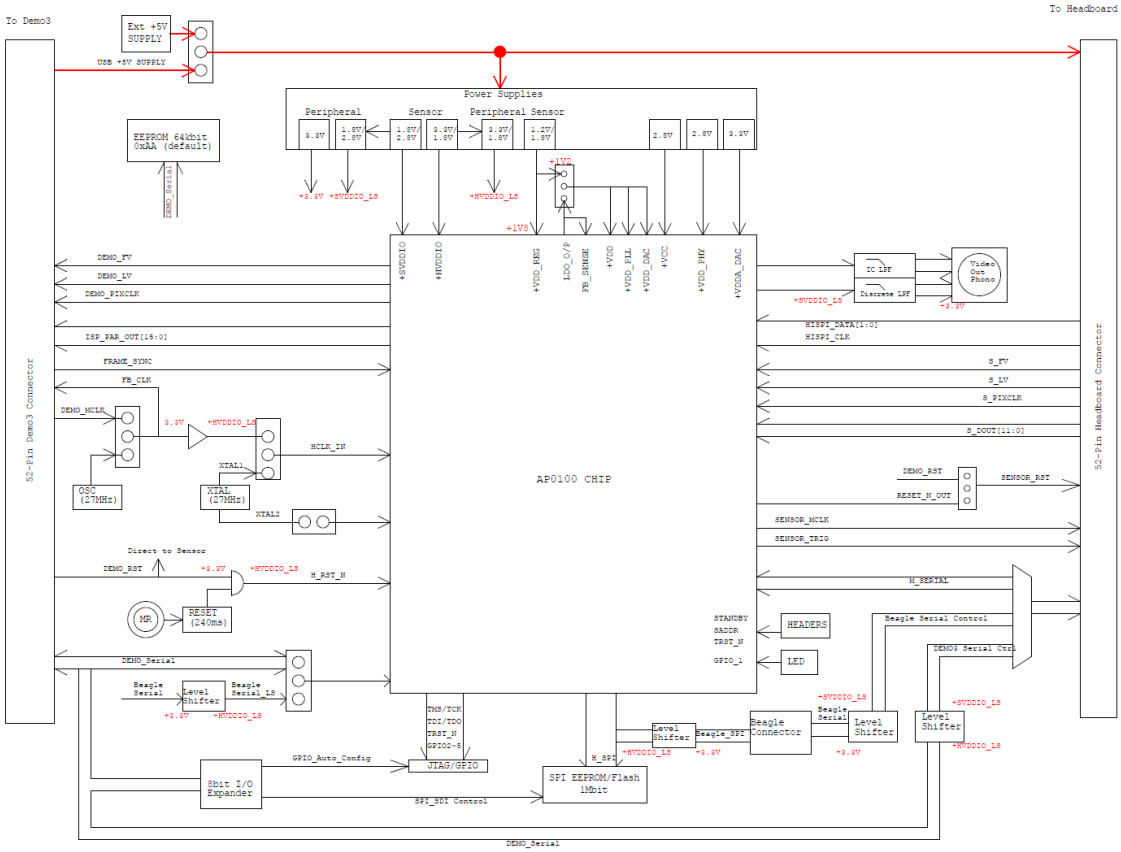

Figure 2. Block Diagram of AP0100AT2L00XUGAH3−GEVB

Top View

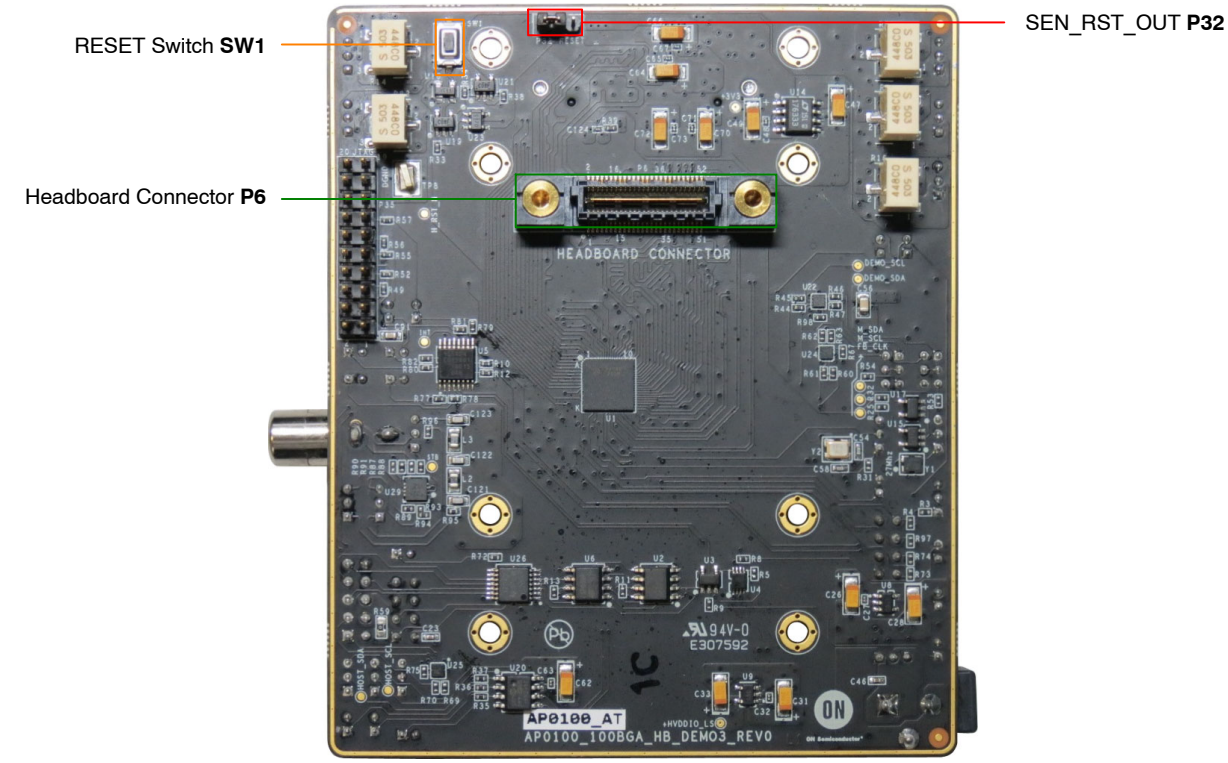

Figure 3. Top View of the Board with Default Jumpers

Bottom View

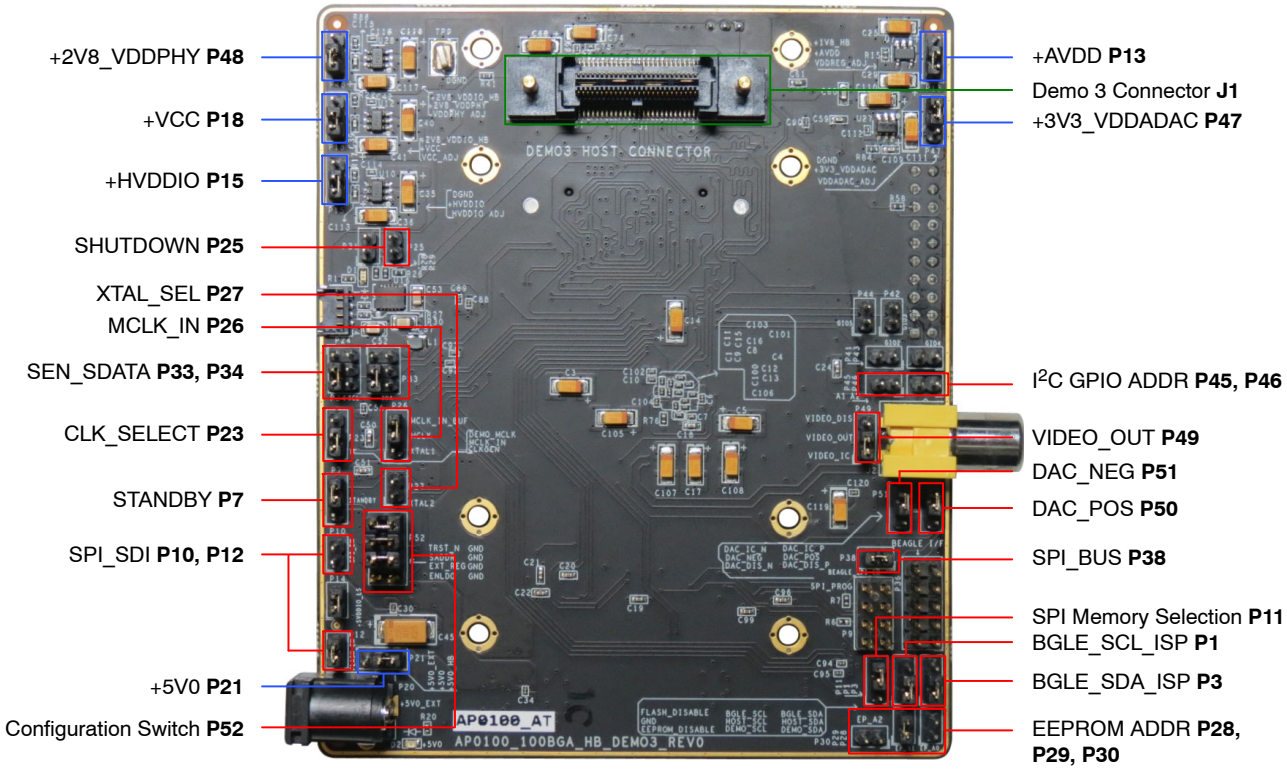

Figure 4. Bottom View of the Board

Jumper Pin Locations

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.

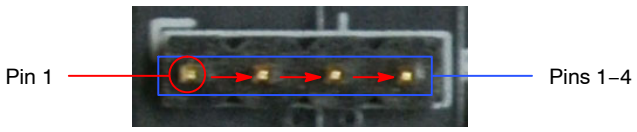

Figure 5. Pin Locations for a Single Jumper. Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right

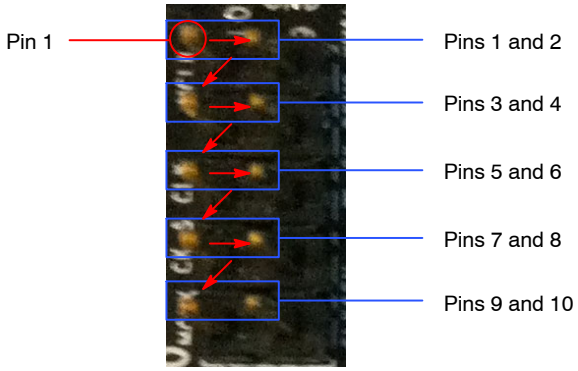

Figure 6. Pin Locations and Assignments of Grouped Jumpers. Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture

Jumper/Header Functions & Default Positions

Table 1. JUMPERS AND HEADERS

Jumper/Header No.	Jumper/Header Name	Pins	Description
P1	BGLE_SCL_ISP	1−2 (Default)	Demo 3 Baseboard I^2C is Master
		2−3	Beagle Board is Master
P3	BGLE_SDA_ISP	1−2 (Default)	Demo 3 Baseboard I^2C is Master
		2−3	Beagle Board is Master
P7	STANDBY	2−3 (Default)	Active Mode
		1−2	Standby Mode
		Open	Auto Serial Control
P11	SPI Memory Selection	2−3 (Default)	EEPROM Disable/Flash Enable
		1−2	Flash Disable/EEPROM Enable
P10, P12	SPI_SDI	P10 Open, P12 1−2 (Default)	HOST Mode
		P10 Open, P12 1−2	FLASH Mode
		P10 1−2, P12 1−2	AUTO Config Mode
P13	+AVDD	1−2(Default)	Adjusts On-Board Regulator to +1.8 V, Internal Regulator Use
		2−3	+1.8 V Supply from Demo 3
P15	+HVDDIO	1−2(Default)	Connects to On-Board +3.3 V Power Supply
		2−3	+1.8 V Supply from Demo 3

Table 1. JUMPERS AND HEADERS (continued)

Jumper/Header No.	Jumper/Header Name	Pins	Description
P18	+VCC	1−2(Default)	Connects to On-Board +VCC Power Supply
		2−3	External Power Supply Connection
P21	+5V0	1−2(Default)	Connects to On-Board +5.0 V Power Supply
		2−3	External Power Supply Connection
P23	CLK_SELECT	1−2(Default)	Selects On-Board 27 MHz Oscillator
		2−3	Selects External Demo 3 Clock
P25	SHUTDOWN	Open (Default)	Shutdown
		Closed	Normal Mode
P26	MCLK_IN	1−2 (Default)	Selects MCLK_IN Signal
		2−3	Selects Crystal Clock
P27	XTAL_SEL	Open (Default)	Selects Oscillator/Demo 3 Clock for XTAL2
		Closed	Selects Crystal Clock
P28, P29, P30	EEPROM ADDR	P28 Open, P29 Closed, P30 Open	EEPROM Address Set to 0xAA (Default)
		P28 Closed, P29 Closed, P30 Open	EEPROM Address Set to 0xA2
		P28 Closed, P29 Open, P30 Open	EEPROM Address Set to 0xA6
		P28 Open, P29 Open, P30 Open	EEPROM Address Set to 0xAE
P32	SEN_RST_OUT	2−3 (Default)	AP0100 Reset
		1−2	Demo 3 Reset
P33, P34	SEN_SDATA	3−5 (Default)	ISP Serial Control
		1−2	Beagle to ISP Serial Control
		1−3	Demo 3 Serial Control
		2−4	Beagle to Sensor Serial Control
P38	SPI_BUS	Closed (Default)	Beagle No Access to SPI Bus
		Open	Beagle Access to SPI Bus
P45, P46	I^2C GPIO ADDR	P46 Open, P45 Closed (Default)	Address Set to 0x48
		P46 Open, P45 Open	Address Set to 0x4C
		P46 Closed, P45 Open	Address Set to 0x44
		P46 Closed, P45 Closed	Address set to 0x40
P47	+3V3_VDDADAC	1−2 (Default)	Connects to On-Board +VDDADAC Power Supply
		2−3	Connection to External Power Supply
P48	+2V8_VDDPHY	1−2 (Default)	Connects to On-Board +VDDPHY Power Supply
		2−3	Connection to External Power Supply
P49	VIDEO_OUT	2−3 (Default)	Active Low Pass Filter
		1−2	Discrete Low Pass Filter
P50	DAC_POS	2−3 (Default)	Active Low Pass Filter
		1−2	Discrete Low Pass Filter
P51	DAC_NEG	2−3 (Default)	Active Low Pass Filter
		1−2	Discrete Low Pass Filter

Table 1. JUMPERS AND HEADERS (continued)

Jumper/Header No.	Jumper/Header Name	Pins	Description
P52	Configuration Header	1−2 Open (Default)	ENLDO: Enable Internal Regulator
		1−2 Closed	ENLDO: Disable Internal Regulator
		3−4 Closed (Default)	EXT_REG: Internal Regulator Selected
		3−4 Open	EXT_REG: External Regulator Selected
		5−6 Closed (Default)	SADDR: Address Set to 0x90
		5−6 Open	SADDR: Address Set to 0xBA
		7−8 Closed (Default)	TRST_N: Normal Operation
		7−8 Open	TRST_N: Test Mode
SW1	RESET	N/A	When Pushed, 240 ms Reset Signal will be Sent to AP0100 Chip

Interfacing to ON Semiconductor Demo 3 Baseboard

The ON Semiconductor Demo 3 headboard has a similar 52-pin connector which mates with P6 of the adapter board. The ON Semiconductor Demo 3 baseboard has a similar 52-pin connector which mates with J1 of the adapter board. The four mounting holes secure the baseboard and the headboard with spacers and screws.

PUBLICATION ORDERING INFORMATION

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