PSOC™ 4 MCU: PSOC™ 4100T Plus datasheet

Based on Arm® Cortex®-M0+ CPU

General description

PSOC™ 4 is a family of scalable MCUs with an Arm® Cortex®-M0+ CPU. It combines a high-performance capacitive sensing subsystem, programmable and reconfigurable analog and digital blocks. The new PSOC™ 4100T Plus series provides an upgrade path for PSOC™ 4100 and PSOC™ 4100S based designs to fifth-generation HMI technology with software and package compatibility.

PSOC™ 4100T Plus is a member of the PSOC™ 4 MCU family with fifth-generation CAPSENSE™ and multi-sense technology offering ultra-low power touch HMI solution based on an integrated “Always-On” sensing technology, improved performance to enable modern sleek user interface solutions with superior liquid tolerance and provides robust and reliable touch HMI solution for harsh environments.

PSOC™ 4100T Plus is a microcontroller with standard communication, timing peripherals and Infineon’s fifth-generation CAPSENSE™ and multi-sense HMI technology purpose built for varieties of low power applications including white goods, small home appliances, touch-controlled screens, and smart connected IoT products that needs low power operation and improved performance to enable next generation of user experience.

Features

- 32-bit MCU subsystem
  - 48-MHz Arm® Cortex®-M0+ CPU with single-cycle multiply
  - Up to 128 KB of flash with read accelerator
  - Up to 32 KB of SRAM
- Low-power 1.71 V to 5.5 V operation
  - Deep Sleep mode with 8 µA always-on touch sensing
  - Active touch detection and tracking with 300 µA (average)
- Fifth-generation CAPSENSE™ sensing
  - All-new ratio-metric sensing architecture in Multi-Sense Converter Low Power (MSCLP) provides best-in-class signal-to-noise ratio (SNR) (>5:1) and liquid tolerance for capacitive sensing.
  - “Always-On” sensing in Deep Sleep mode with hardware-based wake on touch detection for ultra-low power operation in standby mode.
  - Autonomous channel scanning without assistance from the MCU core for low power optimization with active touch detection and tracking
  - Advanced proximity sensing with directivity with machine learning based algorithms
  - Infineon-supplied software middleware makes capacitive sensing design easy
  - Automatic hardware tuning (SmartSense)
- Serial communication
  - Two independent runtime reconfigurable serial communication blocks (SCBs) with re-configurable I^2C, SPI, or UART functionality in one block with master/slave I^2C functionality in the other.
  - Three UART blocks with RTS and CTS
- Timing and pulse-width modulation
  - Six 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Center-aligned, edge, and pseudo-random modes
  - Comparator-based triggering of kill signals
  - Quadrature decoder
- Clock sources
  - ±1% internal main oscillator (IMO)
  - 40 kHz internal low-power oscillator (ILO)
  - 32-kHz watch crystal oscillator (WCO)

Features

- ADC conversion
  - 12-bit one megasample ADC with 8-channel sequencer
- Up to 53 programmable GPIO pins
  - 44LD TQFP (0.8mm pitch), 48LD TQFP (0.5mm pitch), 48L QFN (0.4mm pitch), and 64LD TQFP (0.5mm pitch)
  - GPIO pins can have sensing or digital functionality
- ModusToolbox™
  - Comprehensive collection of multi-platform tools and software libraries
  - Includes board support packages (BSPs), peripheral driver library (PDL), and middleware such as CAPSENSE™
- Industry-standard tool compatibility
  - After configuration, development can be done with Arm®-based industry-standard development tools

Development ecosystem

PSOC™ 4100T Plus resources

Infineon provides a wealth of data at **www.infineon.com** to help you select the right PSOC™ MCU device and quickly and effectively integrate it into your design. The following is an abbreviated, hyperlinked list of resources for PSOC™ 4100T Plus:

- **Overview: PSOC™ portfolio**
- **Product selectors: PSOC™ 4 MCU**
- **Application notes** cover a broad range of topics, from basic to advanced level; please refer to the following when using this device:
  - **AN79953**: Getting started with PSOC™ 4
  - **AN88619**: PSOC™ 4 MCU hardware design considerations
  - **AN85951**: PSOC™ 4 and PSOC™ 6 MCU CAPSENSE™ design guide
  - **AN234231**: PSOC™ 4 CAPSENSE™ ultra-low-power capacitive sensing techniques
  - **AN86233**: PSOC™ 4 MCU power reduction techniques
  - **AN239751**: Flyback inductive sensing design guide
  - **AN239805**: Liquid-level sensing with PSOC™ 4 CAPSENSE™
  - **AN241091**: Hover-touch sensing with PSOC™ 4 CAPSENSE™
  - **AN241228**: Wear detection with PSOC™ 4 CAPSENSE™
  - **AN241195**: Manufacturing test recommendations for PSOC™ 4 CAPSENSE™ designs
- **Code examples** demonstrate product features and usage, and are also available on **GitHub repositories**.
- **Technical reference manuals (TRMs)** provide detailed descriptions of PSOC™ 4 MCU architecture and registers.
- **PSOC™ 4 MCU programming specification** provides the information necessary to program PSOC™ 4 MCU nonvolatile memory.
- **Development tools**
  - **ModusToolbox™** enables cross platform code development with a robust suite of tools and software libraries.
  - Evaluation, system solution, and development kits will be available for the PSOC™ 4100T Plus at product release.
  - The **CY8CPROTO-041TP Prototyping Kit** enables you to evaluate and develop with Infineon's fifth-generation, low-power CAPSENSE™ solution using the PSOC™ 4100T Plus device.
  - **MiniProg4** and **MiniProg3** all-in-one development programmers and debuggers.
  - **PSOC™ 4 MCU CAD libraries** provide footprint and schematic support for common tools. IBIS models are also available.
- **Training videos** are available on a wide range of topics including the **PSOC™ 101 series**.
- **Infineon Developer Community** enables connection with fellow PSOC™ developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated **PSOC™ 4 MCU community**.

ModusToolbox™

ModusToolbox™ is comprehensive collection of multi-platform tools and software libraries that enable an immersive development experience for creating converged MCU and wireless systems. It is:

- Comprehensive - it has the resources you need
- Flexible - you can use the resources in your own workflow
- Atomic - you can get just the resources you want

Infineon provides a large collection of code **repositories on GitHub**, including:

- Board support packages (BSPs) aligned with Infineon kits
- Low-level resources, including a peripheral driver library (PDL)
- Middleware enabling industry-leading features such as CAPSENSE™
- An extensive set of thoroughly tested **code example applications**

ModusToolbox™ software is IDE-neutral and easily adaptable to your workflow and preferred development environment. It includes a project creator, peripheral and library configurators, a library manager, as well as the optional Eclipse IDE for ModusToolbox™ software, as **Figure 1** shows. For information on using Infineon tools, refer to the documentation delivered with ModusToolbox™ software, and **AN79953: Getting started with PSOC™ 4**.

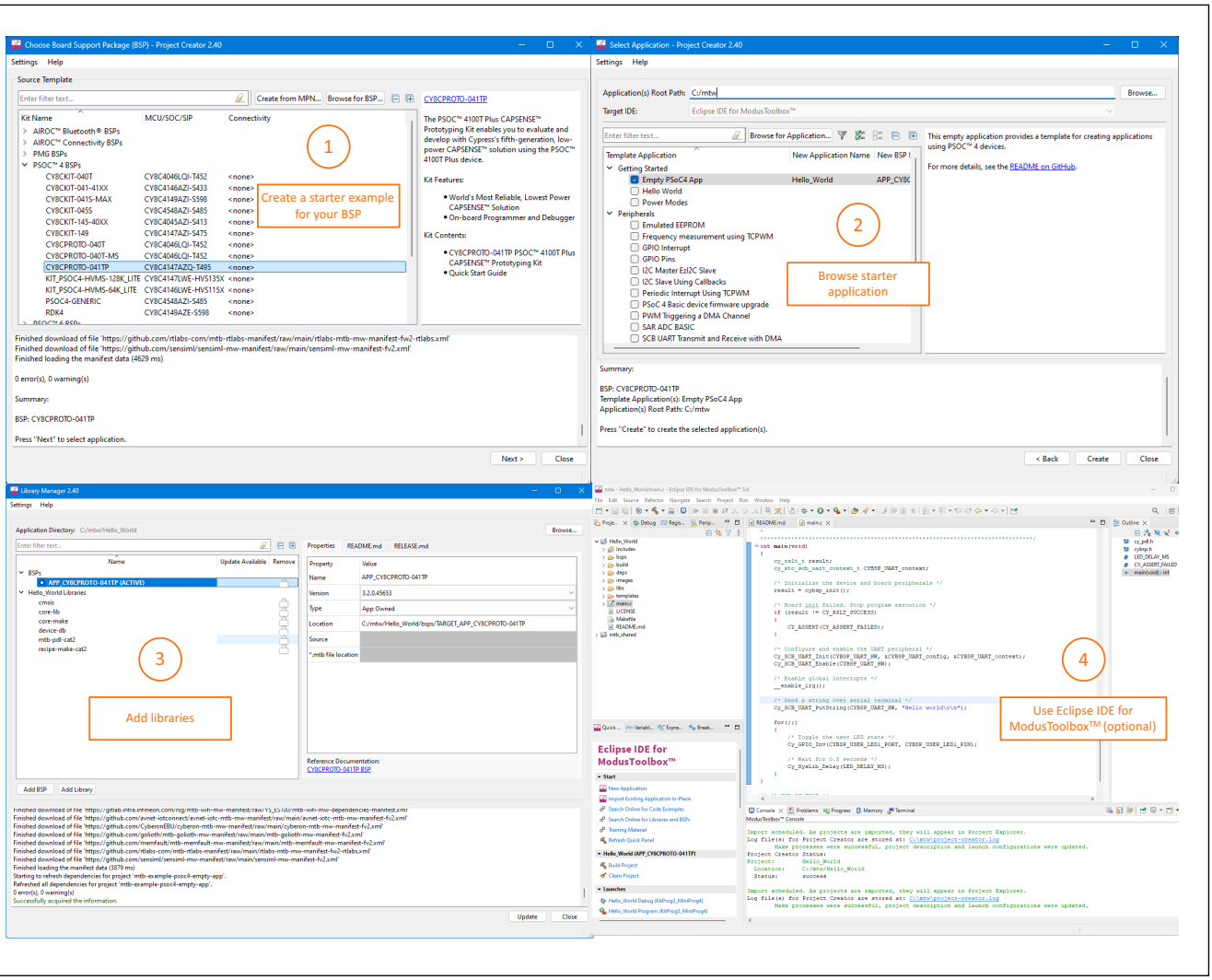

Figure 1 ModusToolbox™ tools

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Block diagram

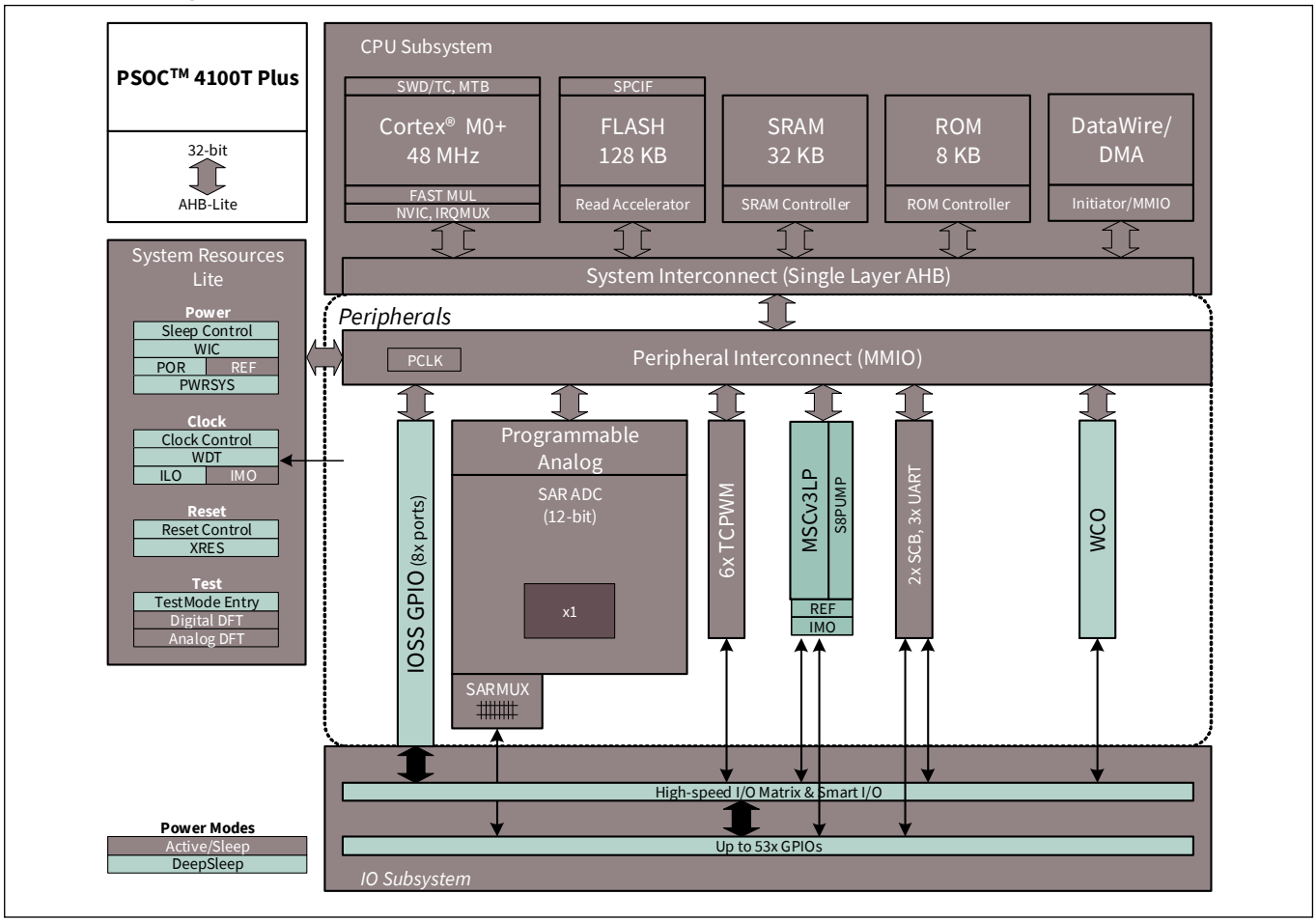


Figure 2 Block diagram

This device includes extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® serial-wire debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The ModusToolbox™ IDE provides fully integrated programming and debug support for this device. The SWD interface is fully compatible with industry-standard third-party tools. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device if not erase protected, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, this device, with device security enabled, may not be returned for failure analysis. This is a trade-off it allows the customer to make.

1 Functional definition

1.1 CPU and memory subsystem

1.1.1 CPU

The Cortex®-M0+ CPU in PSOC™ 4100T Plus is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a wakeup interrupt controller (WIC). The WIC can wake the processor from deep sleep mode, allowing power to be switched off to the main processor when the chip is in deep sleep mode.

The CPU subsystem includes the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSOC™ 4100T Plus has four breakpoint (address) comparators and two watchpoint (data) comparators. There are eight Datawire/DMA channels.

1.1.2 Flash

The PSOC™ 4100T Plus device has a 128 KB flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

1.1.3 SRAM

32 KB of SRAM are provided with zero wait-state access at 48 MHz.

1.1.4 SROM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

1.2 System resources

1.2.1 Power system

The power system is described in detail in the section **Power**. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brownout detection). It operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 2.0 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. PSOC™ 4100T Plus provides Active, Sleep, and DeepSleep low-power modes.

All subsystems are operational in active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In deep sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The touch sensing system can remain operational in Deep Sleep mode and provide an interrupt in wake-on-touch or proximity modes.

1.2.2 Clock system

The PSOC™ 4100T Plus clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSOC™ 4100T Plus consists of the IMO, ILO, and a 32-kHz watch crystal oscillator.

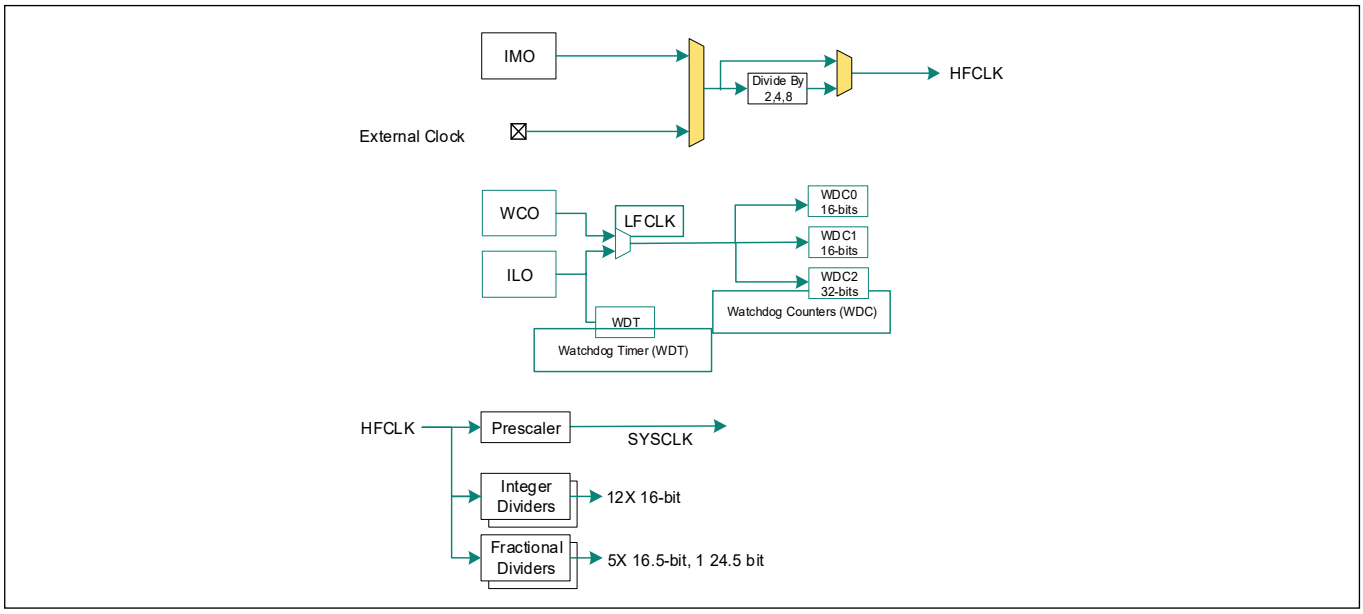


Figure 3 MCU clocking architecture

The HFCLK signal can be divided down as shown to generate synchronous clocks for the peripherals. There are 18 clock dividers for the PSOC™ 4100T Plus. There are 12 16-bit integer dividers allowing a lot of flexibility in generating fine-grained frequency values. And there are five 16.5-bit fractional dividers and one 24.5-bit fractional divider.

1.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSOC™ 4100T Plus. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance is ±1% over the entire voltage and temperature range.

1.2.4 ILO clock source

The ILO is a very low power, nominally 40 kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in deep sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy.

1.2.5 Watchdog timer and counters

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during deep sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a reset cause register, which is firmware readable. The timer can be used to generate interrupts if required in addition to generating resets.

1.2.6 Reset

PSOC™ 4100T Plus can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

1.3 Fixed function digital blocks

1.3.1 TCPWM block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a kill input to force outputs to a predetermined state. Each block also incorporates a quadrature decoder. There are six TCPWM blocks in PSOC™ 4100T Plus.

1.3.2 Serial communication block (SCB)

PSOC™ 4100T Plus has two serial communication blocks, which can be programmed to have SPI, I^2C, or UART functionality. One block can operate in any mode, the other block is an I^2C master/slave block primarily intended to be the interface to a host. In addition, it has three dedicated UART blocks.

1.3.2.1 I^2C mode

The hardware I^2C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 1000 kbps (fast mode plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of PSOC™ 4100T Plus and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode and Fast-mode devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

PSOC™ 4100T Plus is not completely compliant with the I^2C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.

1.3.2.2 UART mode

This is a full-feature UART operating at up to 1-Mbps. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

1.3.2.3 SPI mode

The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

1.4 GPIO

There are 53 GPIOs in the 64-TQFP package. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down (resistive pull-up)
  - Strong pull-up with weak pull-down (resistive pull-down)
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for ports 5 and 6). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

1.5 Special function peripherals

1.5.1 CAPSENSE™ sensing

CAPSENSE™ is supported in PSOC™ 4100T Plus via the MSCLP CAPSENSE™ block. There is one MSCLP block in the PSOC™ 4100T Plus which can be used to scan sense inputs autonomously (without CPU sequencing and intervention) in Deep Sleep and Active modes. CAPSENSE™ function can thus be provided on a pin or group of pins in a system via autonomous scanning or via firmware control.

The PSOC™ 4100T Plus MSCLP block provides the following improvements over previous generation capacitive sensing blocks:

- Improved SNR based on the all new ratio-metric analog architecture and advanced hardware filtering to enable modern sleek user interface solutions with superior liquid tolerance and provides robust and reliable touch HMI solution for harsh environments.
- Higher sensitivity to support smaller sensors, higher proximity detection range, and a much wider range of overlay thicknesses and materials.
- Ultra-low-power operation through “Always-On” sensing which provides hardware-based sensor-data-processing for automatic touch detection in device Deep Sleep mode, to allow wake-on-touch operation.
- Autonomous, i.e. CPU independent, channel sequencing and scanning, for low power optimization.
- Improved shield drive method and support for wider range of shield electrode capacitances for superior liquid tolerance.
- Higher sensor capacitance range to support easier layout and wider variety of sensors.
- Improved EMI performance
- A driver is provided for the CAPSENSE™ block for easy usability.
- The CAPSENSE™ block provides multiple sensing methods such as mutual capacitance sensing, self-capacitance sensing, and inductive sensing.
- The MSCLP has two very low power scanning modes: Wake-on-Touch (WoT) and Active Low Refresh (ALR). WoT is an autonomous scanning mode.

1.6 Programmable digital block (Smart I/O)

The Smart I/O block is a fabric of switches and LUTs that allows Boolean functions to be performed on signals that are routed to the pins of a GPIO port. The Smart I/O can perform functions on input pins to the chip and on signals going out as outputs. The Smart I/O block is associated with I/O Port 2 (8 GPIO pins).

1.7 12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

2 Pinouts

Table 1 provides the pin list for PSOC™ 4100T Plus for the 44LD TQFP, 48LD TQFP, 48L QFN, and 64LD TQFP packages.

Table 1 PSOC™ 4100T Plus pin list

64-TQFP		48-TQFP		48-QFN		44-TQFP	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
43	P0.0	27	P0.0	27	P0.0	23	P0.0
44	P0.1	28	P0.1	28	P0.1	24	P0.1
45	P0.2	29	P0.2	29	P0.2	25	P0.2
46	P0.3	30	P0.3	30	P0.3	26	P0.3
47	P0.4	31	P0.4	31	P0.4	27	P0.4
48	P0.5	32	P0.5	32	P0.5	28	P0.5
49	P0.6	33	P0.6	33	P0.6	29	P0.6
50	P0.7	34	P0.7	34	P0.7	30	P0.7
51	XRES	35	XRES	35	XRES	31	XRES
52	VCCD	36	VCCD	36	VCCD	32	VCCD
53	VSSD	37	VSSD	37	VSSD	33	VSSD
54	VDDD	38	VDDD	38	VDDD	34	VDDD
55	VDDA	39	VDDA	39	VDDA	35	VDDA
56	VSSA	40	VSSA	40	VSSA	36	VSSA
57	P1.0	41	P1.0	41	P1.0	37	P1.0
58	P1.1	42	P1.1	42	P1.1	38	P1.1
59	P1.2	43	P1.2	43	P1.2	39	P1.2
60	P1.3	44	P1.3	44	P1.3	40	P1.3
61	P1.4	45	P1.4	45	P1.4	41	P1.4
62	P1.5	46	P1.5	46	P1.5	42	P1.5
63	P1.6	47	P1.6	47	P1.6	43	P1.6
64	P1.7	48	P1.7	48	P1.7	44	P1.7
1	P2.0	1	P2.0	1	P2.0	1	P2.0
2	P2.1	2	P2.1	2	P2.1	2	P2.1
3	P2.2	3	P2.2	3	P2.2	3	P2.2
4	P2.3	4	P2.3	4	P2.3	4	P2.3
5	P2.4	5	P2.4	5	P2.4	5	P2.4
6	P2.5	6	P2.5	6	P2.5	6	P2.5
7	P2.6	7	P2.6	7	P2.6	7	P2.6
8	P2.7	8	P2.7	8	P2.7	8	P2.7
9	VSSD	9	VSSD	9	VSSD	9	VSSD
10	P3.0	–	–	–	–	–	–
11	P3.1	10	P3.1	10	P3.1	10	P3.1
12	P3.2	11	P3.2	11	P3.2	11	P3.2
13	P3.3	12	P3.3	12	P3.3	12	P3.3

Table 1 PSOC™ 4100T Plus pin list *(continued)*

64-TQFP		48-TQFP		48-QFN		44-TQFP	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
14	P3.4	–	–	–	–	–	–
15	P3.5	–	–	–	–	–	–
16	P3.6	–	–	–	–	–	–
17	P3.7	–	–	–	–	–	–
18	VDDD	13	VDDD	13	VDDD	13	VDDD
19	P4.0	14	P4.0	14	P4.0	14	P4.0
20	P4.1	15	P4.1	15	P4.1	15	P4.1
21	P4.2	16	P4.2	16	P4.2	16	P4.2
22	P4.3	17	P4.3	17	P4.3	17	P4.3
23	P4.4	18	P4.4	18	P4.4	18	P4.4
24	P4.5	19	P4.5	19	P4.5	19	P4.5
25	P4.6	20	P4.6	20	P4.6	20	P4.6
26	P4.7	–	–	–	–	–	–
27	P5.0	–	–	–	–	–	–
28	VSSD	21	VSSD	21	VSSD	21	VSSD
29	VDDD	22	VDDD	22	VDDD	22	VDDD
30	P5.1	23	P5.1	23	P5.1	–	–
31	P5.2	24	P5.2	24	P5.2	–	–
32	P5.3	25	P5.3	25	P5.3	–	–
33	P5.4	26	P5.4	26	P5.4	–	–
34	P5.5	–	–	–	–	–	–
35	P5.6	–	–	–	–	–	–
36	P5.7	–	–	–	–	–	–
37	P6.0	–	–	–	–	–	–
38	P6.1	–	–	–	–	–	–
39	P6.2	–	–	–	–	–	–
40	P6.3	–	–	–	–	–	–
41	P6.4	–	–	–	–	–	–
42	VSSD	–	–	–	–	–	–

Descriptions of the power pins are as follows:

VDDD, VDDA: Power supplies for the digital and analog sections respectively.

VSSD, VSSA: Ground pins for the digital and CAPSENSE™ sections respectively.

VCCD: Regulated digital supply (2.0 V ±5%)

GPIOs by package:

Number	44-TQFP	48-TQFP	48-QFN	64-TQFP
GPIO	34	38	38	53

2.1 Alternate pin functions

Each port pin has multiple alternate functions. These are defined in **Table 2**. The columns ACT #x and DS #y denote active and deep sleep mode signals respectively.

The notation for a signal is of the form “IPName[x].signal_name[u]:y”, where:

IPName = Name of the block (such as TCPWM)

x = Unique instance of the IP.

Signal_name = Name of the signal.

u = Signal number where there is more than one signal for a particular signal name.

y = Designates copies of the signal name.

For example, the name “tcpwm[0].line_compl[3]:4” indicates that this is instance 0 of a TCPWM block, the signal is “line_compl # 3 (complement of the line output)”, and this is the fourth occurrence (copy) of the signal.

Signal copies are provided to allow flexibility in routing and to maximize use of on-chip resources.

Table 2 Pin alternate functions table for PSOC™ 4100T Plus

Pin	Name	Analog	MSC/IOSS	PRGIO	CSD_ SENSE	CSD_ SHIELD	AMUXA	AMUXB	ACT #0	ACT #1	ACT #2	ACT #3	DS #0	DS #1	DS #2	DS #3
43	P0.0	–	csd.msc_gpio_ctrl_sns[0]	–	csd.sense:0	csd.shield:0	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[0]:0	scb[0].uart_rx:0	pass.dsi_sar_data_valid	tcpwm.tr_in[0]:0	csd.msc_drv[0]	–	scb[0].i2c_scl:0	scb[0].spi_select0:0
44	P0.1	–	csd.msc_gpio_ctrl_sns[1]	–	csd.sense:1	csd.shield:1	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[0]:0	scb[0].uart_tx:0	pass.tr_sar_out	tcpwm.tr_in[1]:0	csd.msc_drv[1]	–	scb[0].i2c_sda:0	scb[0].spi_select1:0
45	P0.2	wco.wco_in	csd.msc_gpio_ctrl_sns[2]	–	csd.sense:2	csd.shield:2	amuxbus_a_msc	amuxbus_b_msc	–	scb[0].uart_cts:0	pass.dsi_sar_sample_done	–	csd.msc_drv[2]	–	–	scb[0].spi_select2:0
46	P0.3	wco.wco_out	csd.msc_gpio_ctrl_sns[3]	–	csd.sense:3	csd.shield:3	amuxbus_a_msc	amuxbus_b_msc	–	scb[0].uart_rts:0	pass.dsi_sar_data[0]	–	csd.msc_drv[3]	–	–	scb[0].spi_select3:0
47	P0.4	–	csd.msc_gpio_ctrl_sns[4]	–	csd.sense:4	csd.shield:4	amuxbus_a_msc	amuxbus_b_msc	srss.ext_clk	–	pass.dsi_sar_data[1]	–	csd.msc_drv[4]	–	–	scb[0].spi_mosi:0
48	P0.5	–	csd.msc_gpio_ctrl_sns[5]	–	csd.sense:5	csd.shield:5	amuxbus_a_msc	amuxbus_b_msc		–	–	–	csd.msc_drv[5]	–	–	scb[0].spi_miso:0
49	P0.6	–	csd.msc_gpio_ctrl_sns[6]	–	csd.sense:6	csd.shield:6	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[1]:0	–	–	–	csd.msc_drv[6]	–	–	scb[0].spi_clk:0
50	P0.7	–	csd.msc_gpio_ctrl_sns[7]	–	csd.sense:7	csd.shield:7	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[1]:0	–	–	–	csd.msc_drv[7]	–	–	–
57	P1.0	csd.cmod1pads csd.cmod1pad_cref csd.cmod1pad_ccomp	csd.msc_gpio_ctrl_cmod1	–	csd.sense:8	csd.shield:8	amuxbus_a_msc	amuxbus_b_msc	–	–	–	–	csd.msc_cmod1_ddrv	–	–	–
58	P1.1	csd.cmod2pads csd.cmod2pad_cref csd.cmod2pad_ccomp	csd.msc_gpio_ctrl_cmod2	–	csd.sense:9	csd.shield:9	amuxbus_a_msc	amuxbus_b_msc	–	–	–	–	csd.msc_cmod2_ddrv	–	–	–

Table 2 Pin alternate functions table for PSOC™ 4100T Plus *(continued)*

Pin	Name	Analog	MSC/IOSS	PRGIO	CSD_ SENSE	CSD_ SHIELD	AMUXA	AMUXB	ACT #0	ACT #1	ACT #2	ACT #3	DS #0	DS #1	DS #2	DS #3
59	P1.2	–	csd.msc_gpio_ctrl_sns[8]	–	csd.sense:10	csd.shield:10	amuxbus_a_msc	amuxbus_b_msc	–	–	–	–	csd.msc_ddrv[8]	–	–	–
60	P1.3	–	csd.msc_gpio_ctrl_sns[9]	–	csd.sense:11	csd.shield:11	amuxbus_a_msc	amuxbus_b_msc	–	–	–	–	csd.msc_ddrv[9]	–	–	scb[1].spi_select0:0
61	P1.4	–	csd.msc_gpio_ctrl_sns[10]	–	csd.sense:12	csd.shield:12	amuxbus_a_msc	amuxbus_b_msc	–	scb[1].uart_rx:0	pass.dsi_sar_data[2]:0	tcpwm.tr_in[2]:0	csd.msc_ddrv[10]		scb[1].i2c_scl:0	scb[1].spi_select1:0
62	P1.5	–	csd.msc_gpio_ctrl_sns[11]	–	csd.sense:13	csd.shield:13	amuxbus_a_msc	amuxbus_b_msc	–	scb[1].uart_tx:0	pass.dsi_sar_data[3]:0	tcpwm.tr_in[3]:0	csd.msc_ddrv[11]	csd.ext_sync:0	scb[1].i2c_sda:0	scb[1].spi_mosi:0
63	P1.6	–	csd.msc_gpio_ctrl_sns[12]	–	csd.sense:14	csd.shield:14	amuxbus_a_msc	amuxbus_b_msc	–	scb[1].uart_cts:0	–	–	csd.msc_ddrv[12]	csd.ext_sync_clk:0	–	scb[1].spi_miso:0
64	P1.7	pass.sar_ext_vref0 pass.sar_ext_vref1	csd.msc_gpio_ctrl_sns[13]	–	csd.sense:15	csd.shield:15	amuxbus_a_msc	amuxbus_b_msc	–	scb[1].uart_rts:0	–	–	csd.msc_ddrv[13]	csd.ext_frm_start:0	–	scb[1].spi_clk:0
1	P2.0	pass.sarmux_pads[0]	csd.msc_gpio_ctrl_sns[14]	prgio[0].io[0]	csd.sense:16	csd.shield:16	amuxbus_a_pass	amuxbus_b_pass	tcpwm.line[2]:0	scb[2].uart_rx:0	pass.dsi_sar_data[4]:0	tcpwm.tr_in[4]:0	csd.msc_ddrv[14]	csd.obs_data[3]	scb[0].i2c_scl:1	scb[0].spi_select0:1
2	P2.1	pass.sarmux_pads[1]	csd.msc_gpio_ctrl_sns[15]	prgio[0].io[1]	csd.sense:17	csd.shield:17	amuxbus_a_pass	amuxbus_b_pass	tcpwm.line_compl[2]:0	scb[2].uart_tx:0	pass.dsi_sar_data[5]:0	tcpwm.tr_in[5]:0	csd.msc_ddrv[15]	csd.obs_data[2]	scb[0].i2c_sda:1	scb[0].spi_select1:1
3	P2.2	pass.sarmux_pads[2]	csd.msc_gpio_ctrl_sns[16]	prgio[0].io[2]	csd.sense:18	csd.shield:18	amuxbus_a_pass	amuxbus_b_pass	tcpwm.line[3]:0	scb[2].uart_cts:0	–	–	csd.msc_ddrv[16]	csd.obs_data[1]	–	scb[0].spi_select2:1
4	P2.3	pass.sarmux_pads[3]	csd.msc_gpio_ctrl_sns[17]	prgio[0].io[3]	csd.sense:19	csd.shield:19	amuxbus_a_pass	amuxbus_b_pass	tcpwm.line_compl[3]:0	scb[2].uart_rts:0	–	–	csd.msc_ddrv[17]	csd.obs_data[0]	–	scb[0].spi_select3:1
5	P2.4	pass.sarmux_pads[4]	csd.msc_gpio_ctrl_sns[18]	prgio[0].io[4]	csd.sense:20	csd.shield:20	amuxbus_a_pass	amuxbus_b_pass	tcpwm.line[4]:0	scb[3].uart_rx:1	pass.dsi_sar_data[6]:0	–	csd.msc_ddrv[18]	csd.ext_sync:1	–	scb[0].spi_mosi:1
6	P2.5	pass.sarmux_pads[5]	csd.msc_gpio_ctrl_sns[19]	prgio[0].io[5]	csd.sense:21	csd.shield:21	amuxbus_a_pass	amuxbus_b_pass	tcpwm.line_compl[4]:0	scb[3].uart_tx:1	pass.dsi_sar_data[7]:0	tcpwm.tr_in[6]:0	csd.msc_ddrv[19]	csd.ext_sync_clk:1	–	scb[0].spi_miso:1
7	P2.6	pass.sarmux_pads[6]	csd.msc_gpio_ctrl_sns[20]	prgio[0].io[6]	csd.sense:22	csd.shield:22	amuxbus_a_pass	amuxbus_b_pass	tcpwm.line[5]:0	scb[3].uart_cts:1	–	tcpwm.tr_in[0]:1	csd.msc_ddrv[20]	csd.ext_frm_start:1	–	scb[0].spi_clk:1
8	P2.7	pass.sarmux_pads[7]	csd.msc_gpio_ctrl_sns[21]	prgio[0].io[7]	csd.sense:23	csd.shield:23	amuxbus_a_pass	amuxbus_b_pass	tcpwm.line_compl[5]:0	scb[3].uart_rts:1	–	–	csd.msc_ddrv[21]	–	–	–
10	P3.0	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	–	scb[3].uart_cts:0	–	–		–	–	scb[0].spi_select0:2
11	P3.1	–	csd.msc_gpio_ctrl_sns[22]	–	csd.sense:24	csd.shield:24	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[0]:1	scb[3].uart_rts:0	pass.dsi_sar_data[8]:0	tcpwm.tr_in[1]:1	csd.msc_ddrv[22]	–	–	scb[0].spi_select1:2
12	P3.2	–	csd.msc_gpio_ctrl_sns[23]	–	csd.sense:25	csd.shield:25	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[0]:1	scb[3].uart_rx:0	pass.dsi_sar_data[9]:0	tcpwm.tr_in[2]:1	csd.msc_ddrv[23]	cpuss.swd_data:0	scb[0].i2c_sda:2	scb[0].spi_select2:2
13	P3.3	–	csd.msc_gpio_ctrl_sns[24]	–	csd.sense:26	csd.shield:26	amuxbus_a_msc	amuxbus_b_msc	–	scb[3].uart_tx:0	–	–	csd.msc_ddrv[24]	cpuss.swd_clk:0	scb[0].i2c_scl:2	scb[0].spi_select3:2
14	P3.4	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	–	–	–	–	–	–	–	scb[0].spi_mosi:2
15	P3.5	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	–	–	–	–	–	–	–	scb[0].spi_miso:2
16	P3.6	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	–	–	–	–	–	–	–	scb[0].spi_clk:2
17	P3.7	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	–	–	–	–	–	–	–	–

Table 2 Pin alternate functions table for PSOC™ 4100T Plus *(continued)*

Pin	Name	Analog	MSC/IOSS	PRGIO	CSD_ SENSE	CSD_ SHIELD	AMUXA	AMUXB	ACT #0	ACT #1	ACT #2	ACT #3	DS #0	DS #1	DS #2	DS #3
19	P4.0	–	csd.msc_gpio_ctrl_sns[25]	–	csd.sense:27	csd.shield:27	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[1]:1	scb[4].uart_rx:0	pass.dsi_sar_data[10]:0	tcpwm.tr_in[3]:1	csd.msc_ddrv[25]	–	scb[1].i2c_scl:1	scb[1].spi_select0:1
20	P4.1	–	csd.msc_gpio_ctrl_sns[26]	–	csd.sense:28	csd.shield:28	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[1]:1	scb[4].uart_tx:0	pass.dsi_sar_data[11]:0	tcpwm.tr_in[4]:1	csd.msc_ddrv[26]	–	scb[1].i2c_sda:1	scb[1].spi_select1:1
21	P4.2	–	csd.msc_gpio_ctrl_sns[27]	–	csd.sense:29	csd.shield:29	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[2]:1	scb[4].uart_cts:0	–	–	csd.msc_ddrv[27]	–	–	scb[1].spi_select2:0
22	P4.3	–	csd.msc_gpio_ctrl_sns[28]	–	csd.sense:30	csd.shield:30	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[2]:1	scb[4].uart_rts:0	–	–	csd.msc_ddrv[28]	–	–	scb[1].spi_select3:0
23	P4.4	–	csd.msc_gpio_ctrl_sns[29]	–	csd.sense:31	csd.shield:31	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[3]:1	–	–	tcpwm.tr_in[5]:1	csd.msc_ddrv[29]	–	–	scb[1].spi_mosi:1
24	P4.5	–	csd.msc_gpio_ctrl_sns[30]	–	csd.sense:32	csd.shield:32	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[3]:1	–	–	tcpwm.tr_in[6]:1	csd.msc_ddrv[30]	–	–	scb[1].spi_miso:1
25	P4.6	–	csd.msc_gpio_ctrl_sns[31]	–	csd.sense:33	csd.shield:33	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[4]:1	–	–	–	csd.msc_ddrv[31]	–	–	scb[1].spi_clk:1
26	P4.7	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[4]:1	–	–	–	–	–	–	–
27	P5.0	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	–	–	–	–	–	–	–	–
30	P5.1	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[5]:1	scb[0].uart_rx:1	–	tcpwm.tr_in[0]:2	–	–	scb[1].i2c_scl:2	scb[1].spi_mosi:2
31	P5.2	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[5]:1	scb[0].uart_tx:1	–	tcpwm.tr_in[1]:2	–	–	scb[1].i2c_sda:2	scb[1].spi_miso:2
32	P5.3	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[0]:2	scb[0].uart_cts:1	–	tcpwm.tr_in[2]:2	–	–	–	scb[1].spi_clk:2
33	P5.4	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[0]:2	scb[0].uart_rts:1	–	tcpwm.tr_in[3]:2	–	–	–	scb[1].spi_select0:2
34	P5.5	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[1]:2		–	–	–	–	–	scb[1].spi_select1:2
35	P5.6	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[1]:2		–	–	–	–	–	scb[1].spi_select2:1
36	P5.7	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc			–	–	–	–	–	scb[1].spi_select3:1
37	P6.0	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[2]:2	scb[1].uart_rx:1	–	tcpwm.tr_in[4]:2	–	–	scb[0].i2c_scl:3	scb[0].spi_select0:3
38	P6.1	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[2]:2	scb[1].uart_tx:1	–	tcpwm.tr_in[5]:2	–	–	scb[0].i2c_sda:3	scb[0].spi_select1:3
39	P6.2	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[3]:2	scb[1].uart_cts:1	–	tcpwm.tr_in[6]:2	–	–		scb[0].spi_mosi:3
40	P6.3	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line_compl[3]:2	scb[1].uart_rts:1	–	–	–	–	scb[1].i2c_scl:3	scb[0].spi_miso:3
41	P6.4	–	–	–	–	–	amuxbus_a_msc	amuxbus_b_msc	tcpwm.line[4]:2		–	–	–	–	scb[1].i2c_sda:3	scb[0].spi_clk:3

3 Power

There are two distinct modes of operation. In mode 1, the supply voltage range is 2.0 V to 5.5 V (unregulated externally; internal regulator operational). In mode 2, the supply range is 1.8 V ±5% (externally regulated; 1.71 to 1.89, internal regulator enabled).

3.1 Mode 1: 2.0 V to 5.5 V external supply

In this mode, PSOC™ 4100T Plus is powered by an external power supply that can be anywhere in the range of 2.0 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 2.0 V. In this mode, the internal regulator of PSOC™ 4100T Plus supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (2.2 µF; X5R ceramic or better) and must not be connected to anything else.

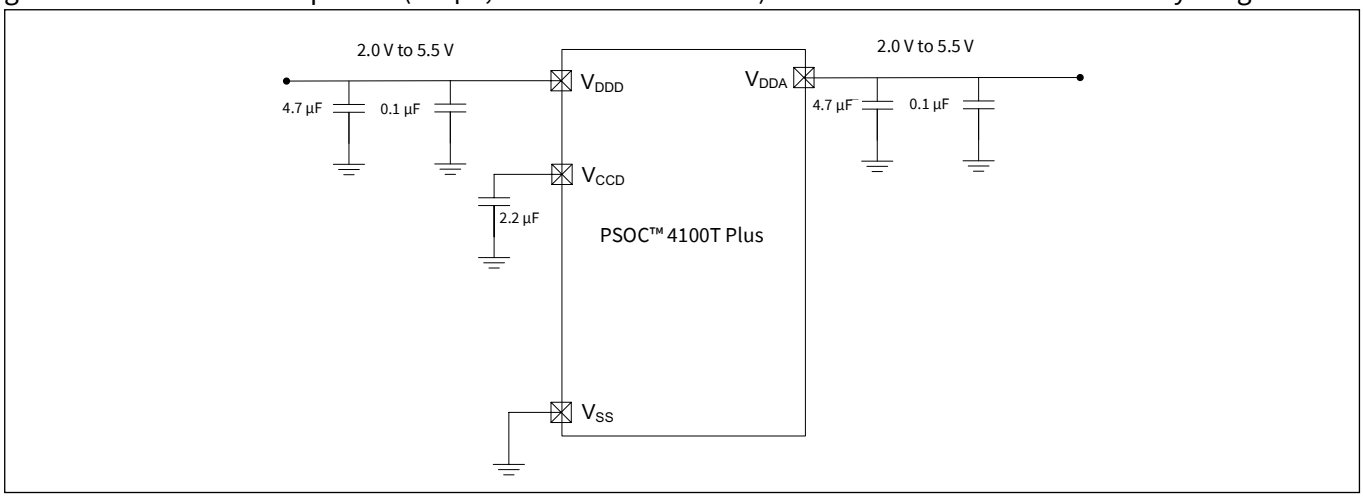


Figure 4 External supply range from 2.0 V to 5.5 V with internal regulator active

3.2 Mode 2: 1.8 V ±5% external supply

In this mode, PSOC™ 4100T Plus is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DDD} and V_{CCD} pins are shorted together and bypassed. The internal regulator must be kept enabled.

Bypass capacitors must be used from V_{DDD} to ground. The typical practice for systems in this frequency range is to use a capacitor as shown in **Figure 5**, in parallel with a smaller capacitance. (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Figure 5 shows an example of a bypass scheme.

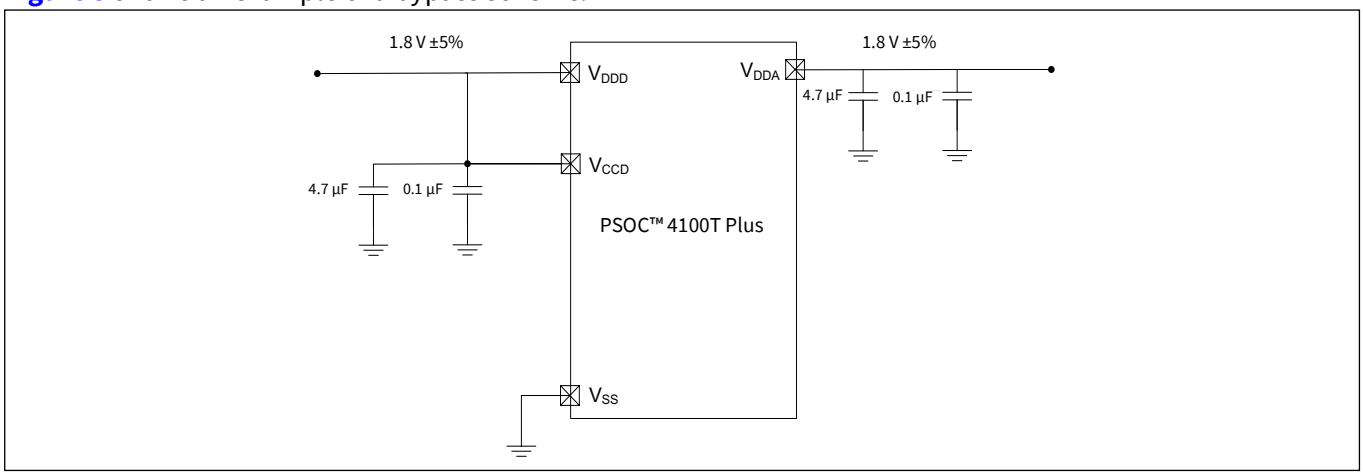


Figure 5 External supply of 1.8 V ±5%

4 Electrical specifications

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to V_{SS} ($V_{SSD} = V_{SSA}$)	–0.5	–	6.0	V	Absolute maximum
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to Vssd	–0.5	–	1.95	V	Absolute maximum
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	–0.5	–	V_{DDD}+ 0.5	V	Absolute maximum
SID4	I_{GPIO_ABS}	Current per GPIO	–25	–	25	mA	Absolute maximum
SID5	$I_{GPIO\_injection}$	GPIO injection current per pin	–0.5	–	0.5	mA	Absolute maximum
BID44	ESD_HBM	Electrostatic discharge voltage	6500			V	Human Body Model ESD
BID45	ESD_CDM	Electrostatic discharge voltage	2000			V	Charged Device Model ESD
BID46	I_LU	Latch-up current limits	–200		200	mA	Max/min current into any input or output, pin-to-pin, pin-to-supply at 125° C ambient

4.2 Device-level specifications

Table 4 DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID53	V_{DDD}	Power supply input voltage	2.0		5.5	V	With internal regulator enabled
SID255	V_{DDD}	Power supply input voltage	1.71	1.8	1.89	V	Internal regulator enabled; VCCD connected to VDDD
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	With internal regulator enabled
SID55	C_{EFC}	External regulator voltage bypass for VCCD	–	2.2	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply decoupling capacitor (±30% max) for VDDD	–	4.7	–	µF	X5R ceramic or better
Active mode, V_{DDD} = 1.71 V to 5.5 V							
SID10	I_{DD5}	Execute from flash; CPU at 6 MHz	–	1.8	2.7	mA	Typ = 25°C at V_{DDD} = 3.3 V. Max = 85°C at 5.5 V.
SID16	I_{DD11}	Execute from flash; CPU at 24 MHz	–	4.5	–	mA	Typ = 25°C at V_{DDD}= 3.3 V. Max = 85°C at 5.5 V.
SID19	I_{DD14}	Execute from flash; CPU at 48 MHz.	–	8.6	–	mA	Typ = 25°C at V_{DDD}= 3.3 V. Max = 85°C at 5.5 V.
Sleep mode, V_{DDD} = 2.0 to 5.5 V (Regulator on)							
SID22	I_{DD17}	I^2C wakeup, WDT, and comparators on. 6 MHz.	–	1.7	2.2	mA	Typ = 25°C at V_{DDD} = 3.3 V. Max = 85°C at 5.5 V.
SID25	I_{DD20}	I^2C wakeup, WDT, and comparators on. 12 MHz.	–	2.2	2.5	mA	Typ = 25°C at V_{DDD} = 3.3 V. Max = 85°C at 5.5 V.

Table 4 DC specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Sleep mode, V_{DDD} = 1.71 to 1.89 V							
SID28	I_{DD23}	I^2C wakeup, WDT, and comparators on. 6 MHz.	–	1.7	2.2	mA	Typ = 25 °C at V_{DDD} = 1.8 V. Max = 85 °C at 1.89 V.
SID28A	I_{DD23A}	I^2C wakeup, WDT, and comparators on. 12 MHz.	–	2.2	2.5	mA	Typ = 25 °C at V_{DDD} = 1.8 V. Max = 85 °C at 1.89 V.
Deep Sleep mode, V_{DDD} = 2.0 to 3.6 V							
SID31	I_{DD26}	I^2C wakeup and WDT on.	–	2.5	80	µA	Typ = 25°C at V_{DDD} = 3.3 V. Max = 85°C at 3.6 V.
SID31A	I_{DD26A}	I^2C wakeup and WDT on.	–	2.5	18	µA	Typ = 25°C at V_{DDD} = 3.3 V. Max = 55°C at 3.6 V
Deep Sleep mode, V_{DDD} = 3.6 to 5.5 V							
SID34	I_{DD29}	I^2C wakeup and WDT on.	–	2.5	80	µA	Typ = 25°C at V_{DDD}= 3.3 V. Max = 85°C at 5.5 V.
SID34A	I_{DD29A}	I^2C wakeup and WDT on.	–	2.5	19	µA	Typ = 25°C at V_{DDD}= 3.3 V. Max = 55°C at V_{DDD} = 5.5 V.
Deep Sleep mode, V_{DDD} = 1.71 to 1.89 V							
SID37	I_{DD32}	I^2C wakeup and WDT on.	–	2.5	80	µA	Typ = 25°C at VDDD = 1.8V. Max = 85°C at 1.89 V
SID37A	I_{DD32A}	I^2C wakeup and WDT on.	–	2.5	16	µA	Typ = 25°C at VDDD = 1.8V. Max = 55°C at 1.89 V.
XRES current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2.0	5	mA	–

Table 5 AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \le V_{DDD} \le 5.5$
SID49	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID50	$T_{DEEPSLEEP}$	Wakeup from deep sleep mode	–	–	35	µs	–

4.2.1 GPIO

Table 6 GPIO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID57	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID241	V_{IH}	LVTTL input, V_{DDD} < 2.7V	0.7 × V_{DDD}	–	–	V	–
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7V	–	–	0.3 × V_{DDD}	V	–
SID243	V_{IH}	LVTTL input, $V_{DDD} \geq$ 2.7V	2.0	–	–	V	–
SID244	V_{IL}	LVTTL input, $V_{DDD} \geq$ 2.7V	–	–	0.8	V	–
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 10 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25°C, V_{DDD} = 3.0 V
SID65A	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67	V_{HYSTTL}	Input hysteresis LVTTL $V_{DDD} \geq$ 2.7V	25	40	–	mV	–
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05× V_{DDD}	–	–	mV	–
SID69	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–
SID69A	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 7 GPIO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V ≤ V_{DDD} ≤ 3.3 V Fast strong mode	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Slow strong mode	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT}; 1.71 V ≤ V_{DDD} ≤ 3.3 V Slow strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

4.2.2 XRES

Table 8 XRES DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID79	R_{PULLUP}	Pull-up resistor	–	60	–	kΩ	–
SID80	C_{IN}	Input capacitance	–	–	7	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–

Table 9 XRES AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–
BID194	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

4.2.3 CAPSENSE™ block

Table 10 MSCLP CAPSENSE™ specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SIDMSC_1	V_{DD_RIPPLE}	Max allowed ripple on power supply, 1 kHz to 10 MHz	–	–	±50	mV	V_{DDD} ≥ 2 V (with ripple), 25 °C T_A, Sensitivity ≥ 50 counts/0.1 pF, 2 pF < Cs < 50 pF
SIDMSC_2	$V_{DD\_RIPPLE\_1.8}$	Max allowed ripple on power supply, 1 kHz to 10 MHz	–	–	±25	mV	V_{DDD} ≥ 1.75 V (with ripple), 25 °C T_A, Sensitivity ≥ 50 counts/0.1 pF, 2 pF < Cs < 50 pF
SIDMSC_2B	F_{MOD}	Modulator frequency	–	–	46	MHz	All V_{DDD}
SIDMSC_2C	$F_{MSCLP\_IMO\_TOL}$	MSCLP clock frequency variation at 25, 38, and 46 MHz	–3	–	+2.5	%	All V_{DDD}
SIDMSC_5	V_{MSC_LP}	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% Externally regulated, 2 V to 5.5 V Externally unregulated
SIDMSC_6	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5–50 pF Sensitivity ≥ 50 counts/0.1 pF VDDA ≥ 2 V
SIDMSC_6a	SNR_{High}	CAPSENSE Signal to Noise Ratio	–	500	–	Ratio	5V, C_p = 4 pF, Signal = 0.3pF, Shield capacitance 18 pF. CIC2 and IIR filter enabled.
SIDMSC_7	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating
SIDMSC_7a	CMOD accuracy	Required tolerance on CMOD capacitance value	–5	–	5	%	
SIDMSC_x8	$F_{CAPSENSE}$	Capacitive sense freq. range	45		6000	kHz	
SIDMSC_9	Noise Floor (CNS)	System Noise Floor	–	0.1	–	fF-rms	With 8 pF input capacitance
SIDMSC_10	CIN_Self	Input capacitance Range for Self Capacitance	2	–	250	pF	
SIDMSC_10A	CIN_Mutual	Input capacitance Range for Mutual Capacitance	0.5	–	30	pF	
SIDMSC_11	MSC_WOT	Average current. Wake On Touch mode. 16 Hz refresh rate	–	8	–	µA	52-pF sensor value, 0.2 pF sensitivity, 1.8 V
SIDMSC_11A	MSC_WOT2	Average current. Wake On Touch mode. 16 Hz refresh rate, SNR ≥ 10	–	15	–	µA	10 self-cap ganged sensors (Total Cp = 250 pF), Finger cap = 0.36 pF, Shield for entire panel = 1030 pF. 1.8 V

Table 10 MSCLP CAPSENSE™ specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SIDMSC_12	MSC_ALR	Average current. Active Low Refresh mode. 32 Hz refresh rate.	–	75	–	µA	13 sensors, 4 pF each, 0.1 pF sensitivity, 1.8 V
SIDMSC_13	MSC_ACT	Average current. CAPSENSE™ active scan mode. 128 Hz refresh rate.	–	300	–	µA	13 sensors, 4 pF each, 0.1 pF sensitivity, 1.8 V
SIDMSC_12A	MSC_ALR4	Average current. Active Low Refresh mode. 32 Hz refresh rate.	–	35	–	µA	4 sensors, 4 pF each, 0.1 pF sensitivity, 1.8 V
SIDMSC_13A	MSC_ACT4	Average current. CAPSENSE™ active scan mode. 128 Hz refresh rate.	–	140	–	µA	4 sensors, 4 pF each, 0.1 pF sensitivity, 1.8 V
SIDMSC_13B	MSC_SCAN27	Average current. CAPSENSE™ active scan self-cap mode. 128-Hz refresh rate, SNR >= 10.	–	1.9	–	mA	10 + 17 self-cap sensors (Cp = 52pF for 10 Cols, 30pF for 16 Rows), Finger cap = 0.25 pF. 1.8 V.
SIDMSC_13C	MSC_SCAN170	Average current. CAPSENSE™ active scan mutual cap mode. 128-Hz refresh rate, SNR >= 10.	–	4	–	mA	10 x 17 (Tx/Rx) Mutual-cap (Cm = 1 pF, Tx Self = 52pF, Rx Self = 30 pF), Finger cap = 0.17pF. 1.8 V.
SIDMSC_14	$I_{DD\_MSC\_S-CAN\_46}$	Sub-system current in CAPSENSE™ active scan mode at 46 MHz	–	2.5	–	mA	V_{DDD} = 1.8 V
SIDMSC_15	$I_{DD\_MSC\_S-CAN\_38}$	Subsystem current in CAPSENSE™ active scan mode at 38 MHz		2		mA	V_{DDD} = 1.8 V
SIDMSC_16	$I_{DD\_MSC\_S-CAN\_25}$	Subsystem current in CAPSENSE™ active scan mode at 25 MHz		1.5		mA	V_{DDD} = 1.8 V
SIDMSC_18	$I_{DD\_MSC\_SBY\_46}$	Subsystem current in Standby mode at 46 MHz (CAPSENSE™ block enabled and ready to begin frame)	–	1.5	–	mA	V_{DDD} = 1.8 V
SIDMSC_19	$I_{DD\_MSC\_SBY\_38}$	Subsystem current in Standby mode at 38 MHz (CAPSENSE™ block enabled and ready to begin frame)	–	1.25	–	mA	V_{DDD} = 1.8 V
SIDMSC_20	$I_{DD\_MSC\_SBY\_25}$	Subsystem current in Standby mode at 25 MHz (CAPSENSE™ block enabled and ready to begin frame)	–	1	–	mA	V_{DDD} = 1.8 V

4.3 Digital peripherals

4.3.1 Timer counter pulse-width modulator (TCPWM)

Table 11 TCPWM specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (Timer/counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	µA	All modes (Timer/counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	µA	All modes (Timer/counter/PWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 48 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	2/Fc	–	–	ns	Minimum possible width of overflow, underflow, and CC (counter equals compare value) trigger outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature phase inputs

4.3.2 I^2C

Table 12 I^2C DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	–
SID151	I_{I2C3}	Block current consumption at 1-Mbps	–	–	310	µA	–
SID152	I_{I2C4}	Block current in deep sleep mode	–	1	–	µA	–

Table 13 I^2C AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	HS I^2C slave mode

4.3.3 UART

Table 14 UART DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	55	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	µA	–

Table 15 UART AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

4.3.4 SPI

Table 16 SPI DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID163	ISPI1	Block current consumption at 1-Mbps	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4-Mbps	–	–	560	µA	–
SID165	ISPI3	Block current consumption at 8-Mbps	–	–	600	µA	–

Table 17 SPI AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	FSPI	SPI operating frequency (Master; 6x oversampling)	–	–	8	MHz	–
SPI master mode AC specifications							
SID167	TDMO	MOSI valid after sclock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before sclock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge
SPI slave mode AC specifications							
SID170	TDMI	MOSI valid before sclock capturing edge	40	–	–	ns	–
SID171	TDSO	MISO valid after sclock driving edge	–	–	42 + 3*Tcpu	ns	$T_{CPU} = 1/F_{CPU}$
SID171A	TDSO_EXT	MISO valid after sclock driving edge in Ext. Clk mode	–	–	48	ns	–
SID172	THSO	Previous MISO data hold time	0	–	–	ns	–
SID172A	TSSELSSCK	SSEL valid to first SCK valid edge	100	–	–	ns	–

4.4 Memory

Table 18 Flash DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–
SID173A	I_{PW}	Page write current at 16 MHz	–	–	3.5	mA	5.5 V V_{DDD}

Table 19 Flash AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID174	$T_{ROWWRITE}$	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	16	ms	–
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	4	ms	–
SID178	$T_{BULKERASE}$	Bulk erase time (32 KB)	–	–	35	ms	–
SID180	$T_{DEVPROG}$	Total device program time	–	–	7	Seconds	–
SID181	F_{END}	Flash endurance	100K	–	–	Cycles	–
SID182	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	Years	–
SID182A	–	Flash retention. $T_A \leq 85$ °C, 10K P/E cycles	10	–	–	Years	–
SID256	TWS48	Number of wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of wait states at 24 MHz	1	–	–		CPU execution from Flash

4.5 System resources

4.5.1 Power-on reset (POR)

Table 20 Power-on reset (PRES)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#6	SR_POW-ER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	–
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4	V	–

Table 21 Brownout detect (BOD) for V_{CCD}

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in deep sleep	1.11	–	1.5	V	–

4.5.2 SWD interface

Table 22 SWD interface specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DDD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 FCPU
SID214	F_SWDCLK2	1.71 V ≤ V_{DDD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 FCPU
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	–
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

4.5.3 Internal main oscillator

Table 23 IMO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180	µA	–

Table 24 IMO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID223	$F_{IMOTOL1}$	Frequency variation at 24, 32, and 48 MHz (trimmed) with software calibration	–1	–	1	%	Operating ambient temperature –40°C to 105°C. See **KBA** for more information on software calibration.
SID223A		Frequency variation at 24, 32, and 48 MHz (trimmed) without software calibration	–1	–	1	%	Operating ambient temperature 5°C to 50°C.
SID223B			–2	–	2	%	Operating ambient temperature –20°C to 105°C.
SID223C			–4	–	2	%	Operating ambient temperature –40°C to 105°C.
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–

4.5.4 Internal low-speed oscillator

Table 25 ILO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID231	I_{ILO2}	ILO operating current at 32 KHz	–	0.3	1.05	µA	–

Table 26 ILO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	–
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	–

Table 27 Temperature sensor

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

Table 28 SAR ADC DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16		8 full speed.
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	-		Yes.
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	Vss	–	VDDA	V	
SID102	A_VIND	Input voltage range - differential[	Vss	–	VDDA	V	
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	
SID104	A_INCAP	Input capacitance	–	–	10	pF	
SID260	V_{REFSAR}	Trimmed internal reference to SAR	1.18	1.2	1.22	V	

Table 29 SAR ADC AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	MSPS	
SID109	A_SNR	Signal-to-noise and Distortion ratio (SINAD)	65	–	–	dB	Fin = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–	–	A_samp/2	KHz	
SID111	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	–1.7	–	2	LSB	Vref = 1 to V_{DD}
SID111A	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6, 1 Msps	–1.5	–	1.7	LSB	Vref = 1.71 to V_{DD}
SID111B	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 500 Ksps	–1.5	–	1.7	LSB	Vref = 1 to V_{DD}
SID112	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	–1	–	2.2	LSB	Vref = 1 to V_{DD}
SID112A	A_DNL	Differential non linearity. V_{DD} = 1.71 to 3.6, 1 Msps	–1	–	2	LSB	Vref = 1.71 to V_{DD}
SID112B	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5, 500 Ksps	–1	–	2.2	LSB	Vref = 1 to V_{DD}
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	Fin = 10 kHz
SID261	$F_{SARINTREF}$	SAR operating speed without external ref. bypass	–	–	100	Ksps	12-bit resolution

5 Ordering information

Table 30 lists the marketing part numbers for the PSOC™ 4100T Plus devices.

Table 30 PSOC™ 4100T Plus ordering information

Category	Product	Features											Packages				Temperature range (°C)
		Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	CAPSENSE™	Multi-Sense[1]	12-bit SAR ADC	TCPWM blocks	UART	SCB blocks	Smart I/Os	GPIO	48-QFN (6×6×0.6, 0.4)	44-TQFP (10×10×1.4, 0.8)	48-TQFP (7×7×1.4, 0.5)	64-TQFP (10×10×1.4, 0.5)	
4146	CY8C4146LQI-T403	48	64	16	0	0	1	6	3	2	8	37	X				–40 to 85
	CY8C4146AXI-T403	48	64	16	0	0	1	6	3	2	8	34		X			–40 to 85
	CY8C4146AZI-T403	48	64	16	0	0	1	6	3	2	8	38			X		–40 to 85
	CY8C4146AZI-T405	48	64	16	0	0	1	6	3	2	8	53				X	–40 to 85
	CY8C4146LQI-T413	48	64	16	1	0	1	6	3	2	8	37	X				–40 to 85
	CY8C4146AXI-T413	48	64	16	1	0	1	6	3	2	8	34		X			–40 to 85
	CY8C4146AZI-T413	48	64	16	1	0	1	6	3	2	8	38			X		–40 to 85
	CY8C4146AZQ-T413	48	64	16	1	0	1	6	3	2	8	38			X		–40 to 105
	CY8C4146AZI-T415	48	64	16	1	0	1	6	3	2	8	53				X	–40 to 85
	CY8C4146LQI-T453	48	64	16	1	1	1	6	3	2	8	37	X				–40 to 85
	CY8C4146AXI-T453	48	64	16	1	1	1	6	3	2	8	34		X			–40 to 85
	CY8C4146AZI-T453	48	64	16	1	1	1	6	3	2	8	38			X		–40 to 85
	CY8C4146AZQ-T453	48	64	16	1	1	1	6	3	2	8	38			X		–40 to 105
	CY8C4146AZI-T455	48	64	16	1	1	1	6	3	2	8	53				X	–40 to 85
4147	CY8C4147LQI-T403	48	128	16	0	0	1	6	3	2	8	37	X				–40 to 85
	CY8C4147AXI-T403	48	128	16	0	0	1	6	3	2	8	34		X			–40 to 85
	CY8C4147AZI-T403	48	128	16	0	0	1	6	3	2	8	38			X		–40 to 85
	CY8C4147AZI-T405	48	128	16	0	0	1	6	3	2	8	53				X	–40 to 85
	CY8C4147LQI-T413	48	128	16	1	0	1	6	3	2	8	37	X				–40 to 85
	CY8C4147AXI-T413	48	128	16	1	0	1	6	3	2	8	34		X			–40 to 85
	CY8C4147AZI-T413	48	128	16	1	0	1	6	3	2	8	38			X		–40 to 85
	CY8C4147AZI-T415	48	128	16	1	0	1	6	3	2	8	53				X	–40 to 85
	CY8C4147AZQ-T415	48	128	16	1	0	1	6	3	2	8	53				X	–40 to 105
	CY8C4147LQI-T453	48	128	16	1	1	1	6	3	2	8	37	X				–40 to 85
	CY8C4147AXI-T453	48	128	16	1	1	1	6	3	2	8	34		X			–40 to 85
	CY8C4147AZI-T453	48	128	16	1	1	1	6	3	2	8	38			X		–40 to 85
	CY8C4147AZI-T455	48	128	16	1	1	1	6	3	2	8	53				X	–40 to 85
	CY8C4147AZQ-T455	48	128	16	1	1	1	6	3	2	8	53				X	–40 to 105
	CY8C4147LQI-T463	48	128	32	0	0	1	6	3	2	8	37	X				–40 to 85
	CY8C4147AXI-T463	48	128	32	0	0	1	6	3	2	8	34		X			–40 to 85
	CY8C4147AZI-T463	48	128	32	0	0	1	6	3	2	8	38			X		–40 to 85

Note
1. Multi-Sense includes CAPSENSE™, inductive sensing, and liquid sensing.

Table 30 PSOC™ 4100T Plus ordering information

Category	Product	Features											Packages				Temperature range (°C)
		Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	CAPSENSE™	Multi-Sense[1]	12-bit SAR ADC	TCPWM blocks	UART	SCB blocks	Smart I/Os	GPIO	48-QFN (6×6×0.6, 0.4)	44-TQFP (10×10×1.4, 0.8)	48-TQFP (7×7×1.4, 0.5)	64-TQFP (10×10×1.4, 0.5)	
4147	CY8C4147AZI-T465	48	128	32	0	0	1	6	3	2	8	53				X	–40 to 85
	CY8C4147LQI-T473	48	128	32	1	0	1	6	3	2	8	37	X				–40 to 85
	CY8C4147AXI-T473	48	128	32	1	0	1	6	3	2	8	34		X			–40 to 85
	CY8C4147AZI-T473	48	128	32	1	0	1	6	3	2	8	38			X		–40 to 85
	CY8C4147AZI-T475	48	128	32	1	0	1	6	3	2	8	53				X	–40 to 85
	CY8C4147LQQ-T493	48	128	32	1	1	1	6	3	2	8	37	X				–40 to 105
	CY8C4147AXQ-T493	48	128	32	1	1	1	6	3	2	8	34		X			–40 to 105
	CY8C4147AZQ-T493	48	128	32	1	1	1	6	3	2	8	38			X		–40 to 105
	CY8C4147AZQ-T495	48	128	32	1	1	1	6	3	2	8	53				X	–40 to 105

Note

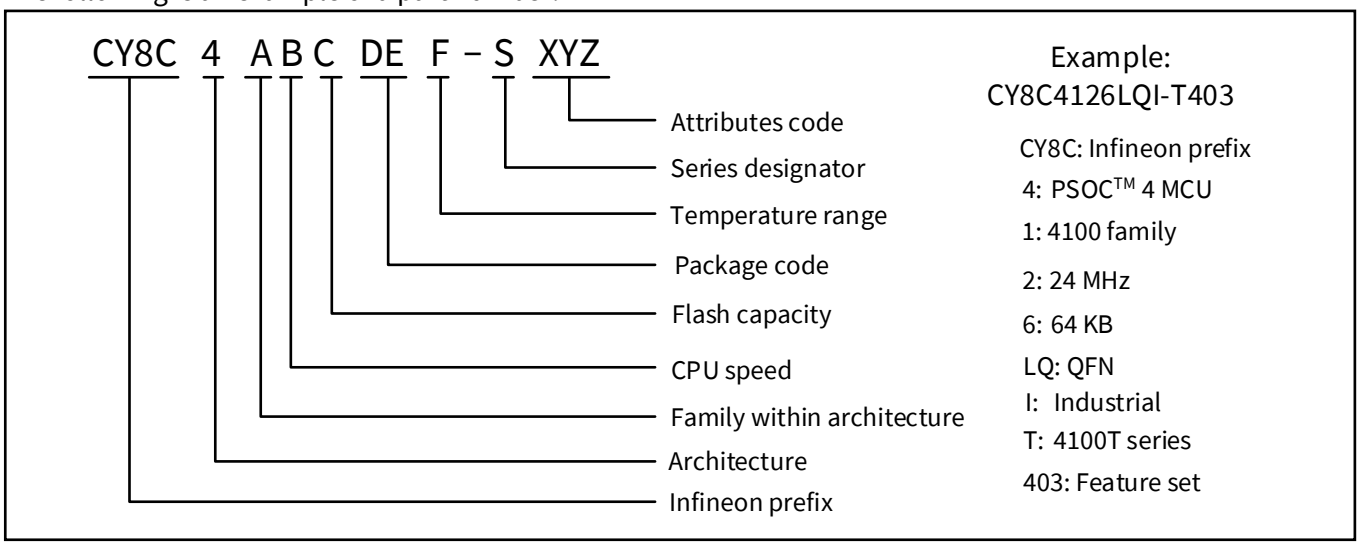
1. Multi-Sense includes CAPSENSE™, inductive sensing, and liquid sensing.

Ordering information

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Infineon prefix	-	-
4	Architecture	4	PSOC™ 4
A	Family	0	PSOC™ 4000 family
		1	PSOC™ 4100 family
		2	PSOC™ 4200 family
B	CPU speed	2	24 MHz
		4	48 MHz
C	Flash capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
		8	256 KB
		9	384 KB
DE	Package code	AX	TQFP (0.8-mm pitch)
		AZ	TQFP (0.5-mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature range	I	Industrial
		Q	Extended industrial
S	Series designator	S	PSOC™ 4 S-series
		M	PSOC™ 4 M-series
		L	PSOC™ 4 L-series
		BL	PSOC™ 4 Bluetooth® LE-series
		T	PSOC™ 4 T series
XYZ	Attributes code	000-999	Code of feature set in the specific family

The following is an example of a part number:



6 Application example schematic

Figure 6 shows a reference implementation schematic of the following touch HMI sensors using PSOC™ 4100T Plus:

- CAPSENSE™ CSD button with shield
- CAPSENSE™ CSX button
- CAPSENSE™ 4x5 touchpad
- 2 Inductive buttons

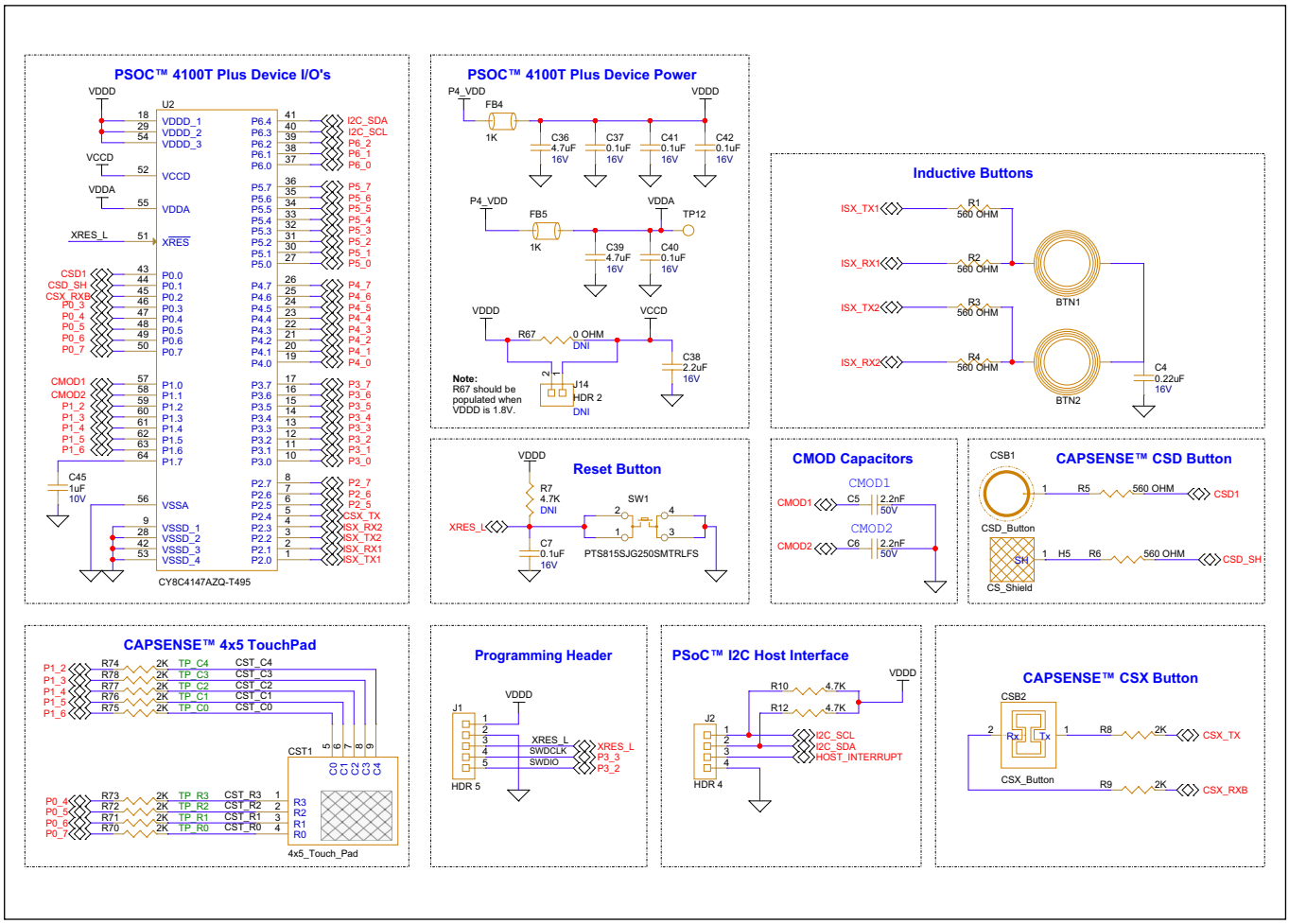


Figure 6 Application example schematic

This schematic can be modified based on your application needs. However, it must conform to this datasheet and **AN88619** - PSOC™ 4 MCU hardware design considerations.

For more details, see the following:

- **AN85951** - PSOC™ 4 and PSOC™ 6 CAPSENSE™ design guide
- **AN239751** - Flyback inductive sensing design guide for inductive sensing applications

7 Packaging

The PSOC™ 4100T Plus is offered in 44LD TQFP, 48LD TQFP, 48L QFN, and 64LD TQFP packages.

Table 31 provides the package dimensions and Infineon drawing numbers.

Table 31 Package list

Spec ID#	Package	Description	Package diagram
BID20	44-TQFP	TQFP 10 ×10 ×1.4 mm, 0.8 mm pitch	51-85064
BID27	48-TQFP	TQFP 7 ×7 ×1.4 mm, 0.5 mm pitch	51-85135
BID34	48-QFN	QFN 6 × 6 × 0.6 mm, 0.4 mm pitch	001-57280
BID34A	64-TQFP	TQFP 10 × 10 × 1.4mm, 0.5 mm pitch	51-85051

Table 32 Package thermal characteristics

Parameter	Description	Package	Min	Typ	Max	Unit
T_A	Operating ambient temperature	–	–40	25	105	°C
T_J	Operating junction temperature	–	–40	25	125	°C
T_{JA}	Package θ_{JA}	44-TQFP 10 × 10 (0.8 mm pitch)	–	47	–	°C/Watt
T_{JC}	Package $\theta_{JC(top)}$	44-TQFP 10 × 10 (0.8 mm pitch)	–	23	–	°C/Watt
T_{JC}	Package $\theta_{JC(bottom)}$	44-TQFP 10 × 10 (0.8 mm pitch)	–	35	–	°C/Watt
T_{JA}	Package θ_{JA}	48-TQFP 7 × 7 (0.5 mm pitch)	–	49	–	°C/Watt
T_{JC}	Package $\theta_{JC(top)}$	48-TQFP 7 × 7 (0.5 mm pitch)	–	27	–	°C/Watt
T_{JC}	Package $\theta_{JC(bottom)}$	48-TQFP 7 × 7 (0.5 mm pitch)	–	39	–	°C/Watt
T_{JA}	Package θ_{JA}	48-QFN 6 × 6 (0.4 mm pitch)	–	22	–	°C/Watt
T_{JC}	Package $\theta_{JC(top)}$	48-QFN 6 × 6 (0.4 mm pitch)	–	19	–	°C/Watt
T_{JC}	Package $\theta_{JC(bottom)}$	48-QFN 6 × 6 (0.4 mm pitch)	–	3	–	°C/Watt
T_{JA}	Package θ_{JA}	64-TQFP 10 × 10 (0.5 mm pitch)	–	44	–	°C/Watt
T_{JC}	Package $\theta_{JC(top)}$	64-TQFP 10 × 10 (0.5 mm pitch)	–	22	–	°C/Watt
T_{JC}	Package $\theta_{JC(bottom)}$	64-TQFP 10 × 10 (0.5 mm pitch)	–	34	–	°C/Watt

7.1 Package diagram

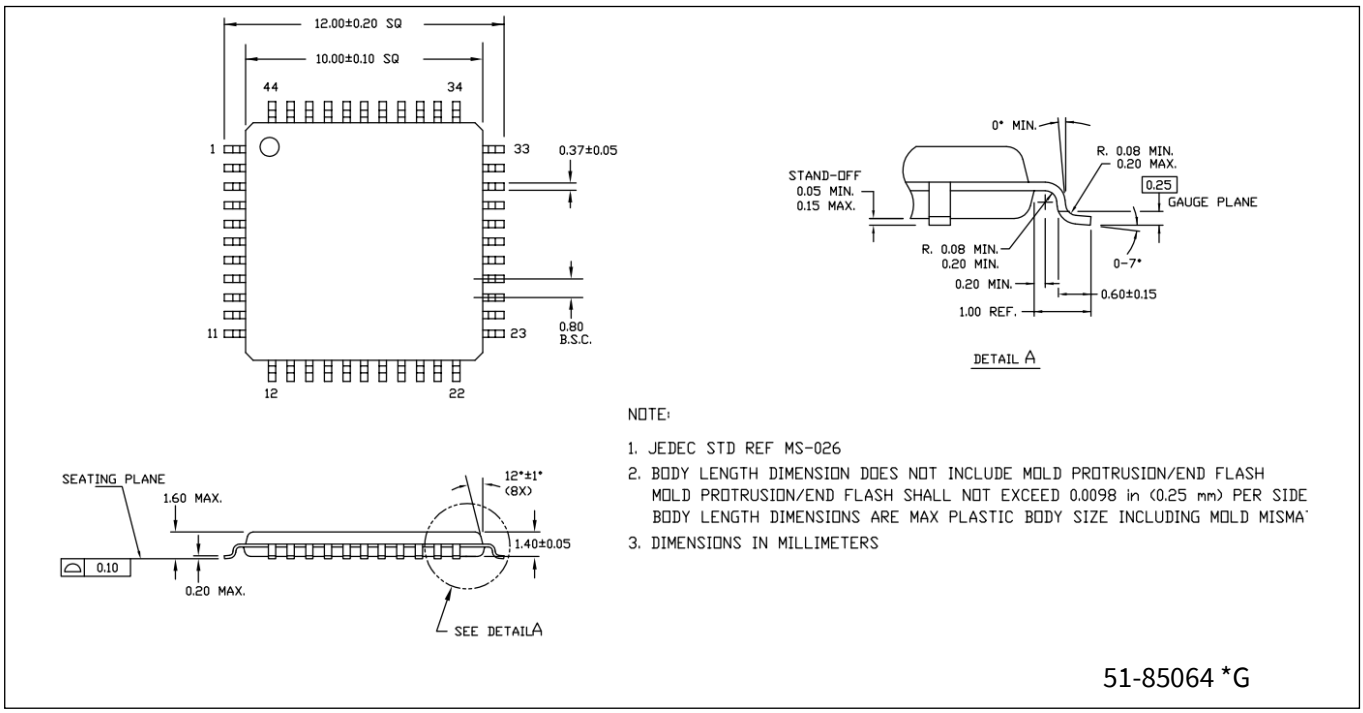


Figure 7 44LD TQFP (10 × 10 × 1.4 mm) A44S (PG-TQFP-44) package outline

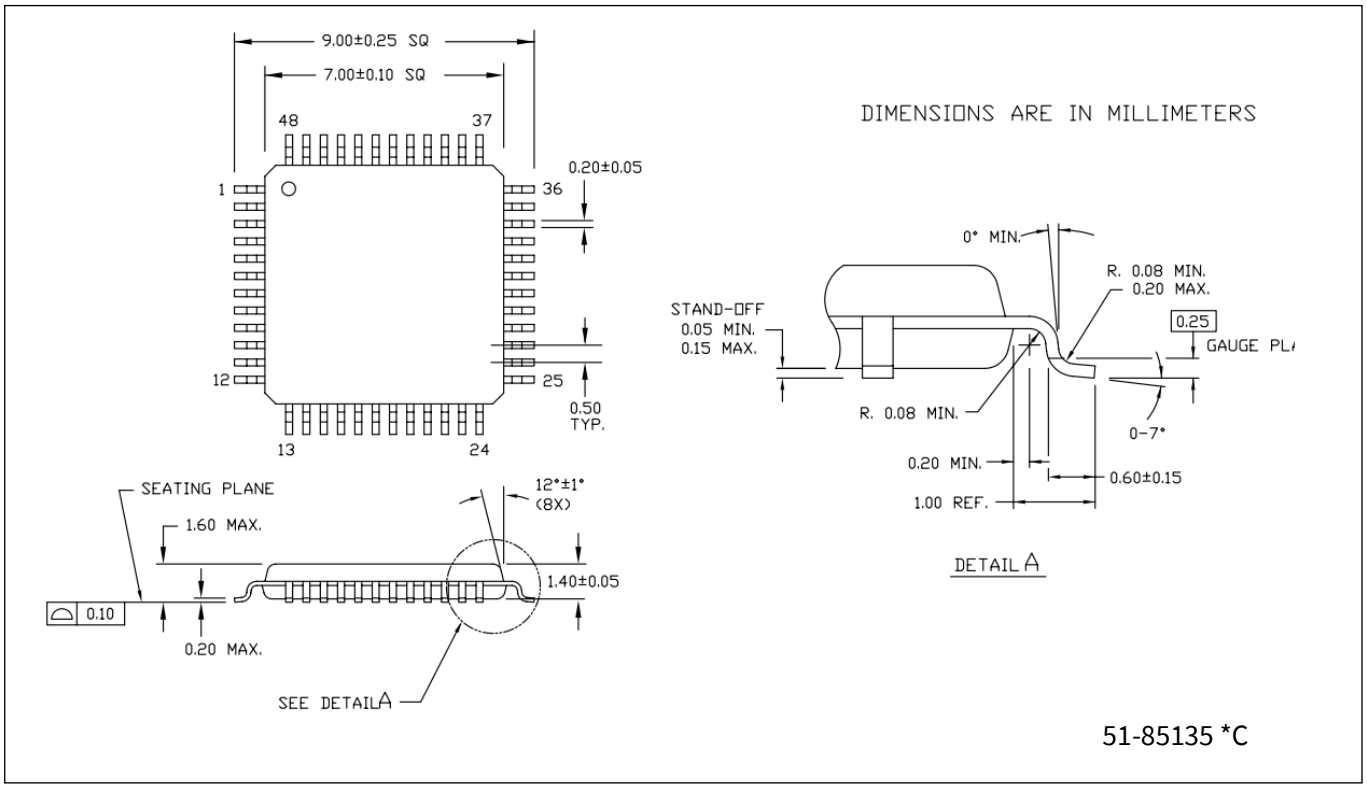


Figure 8 48LD TQFP (7 × 7 × 1.4 mm) A48 (PG-TQFP-48) package outline

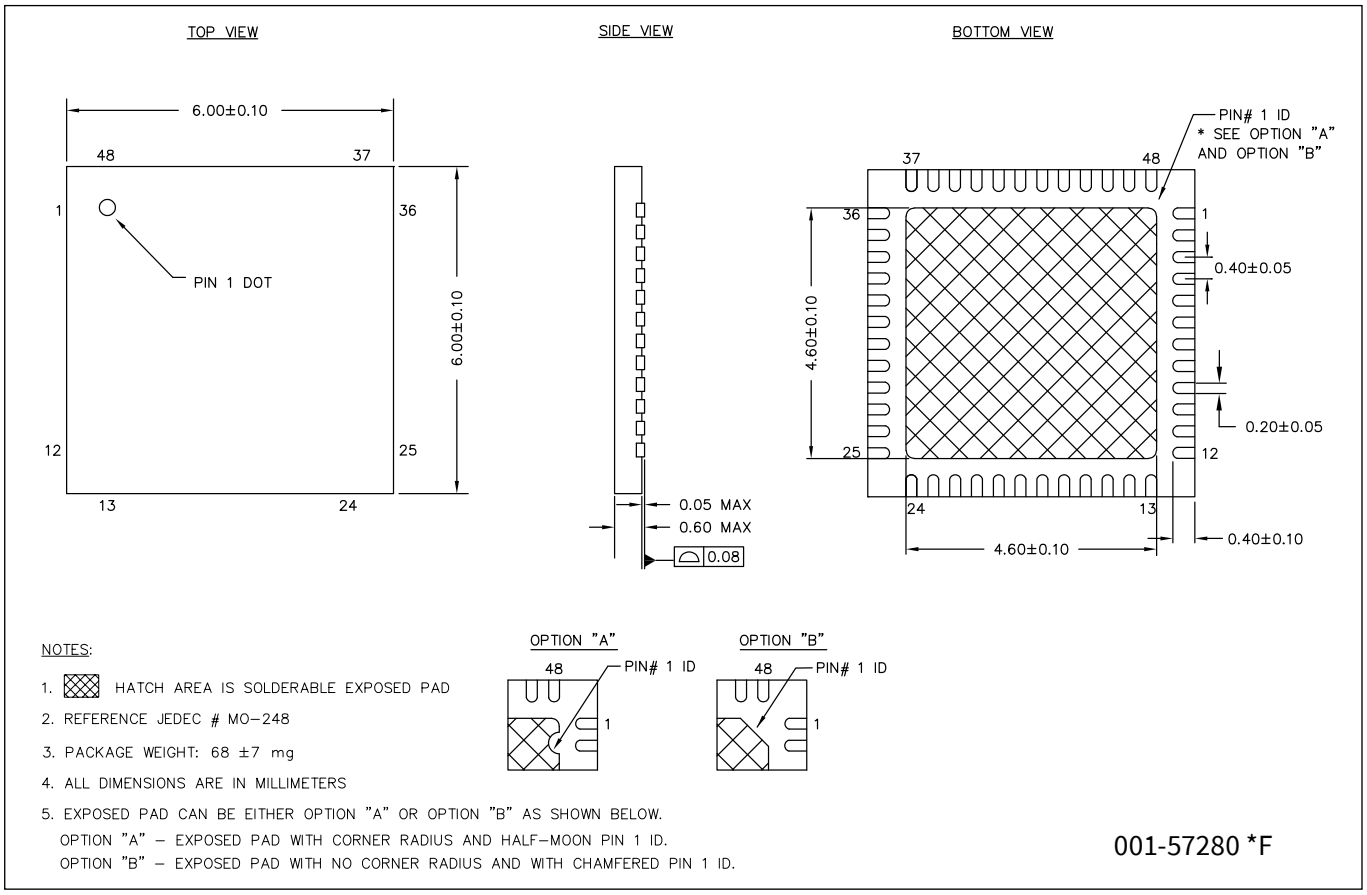


Figure 9 48L QFN (6 × 6 × 0.6 mm) LR48A/LQ48A (4.6 × 4.6 E-PAD) SAWN (PG-VQFN-48) package outline

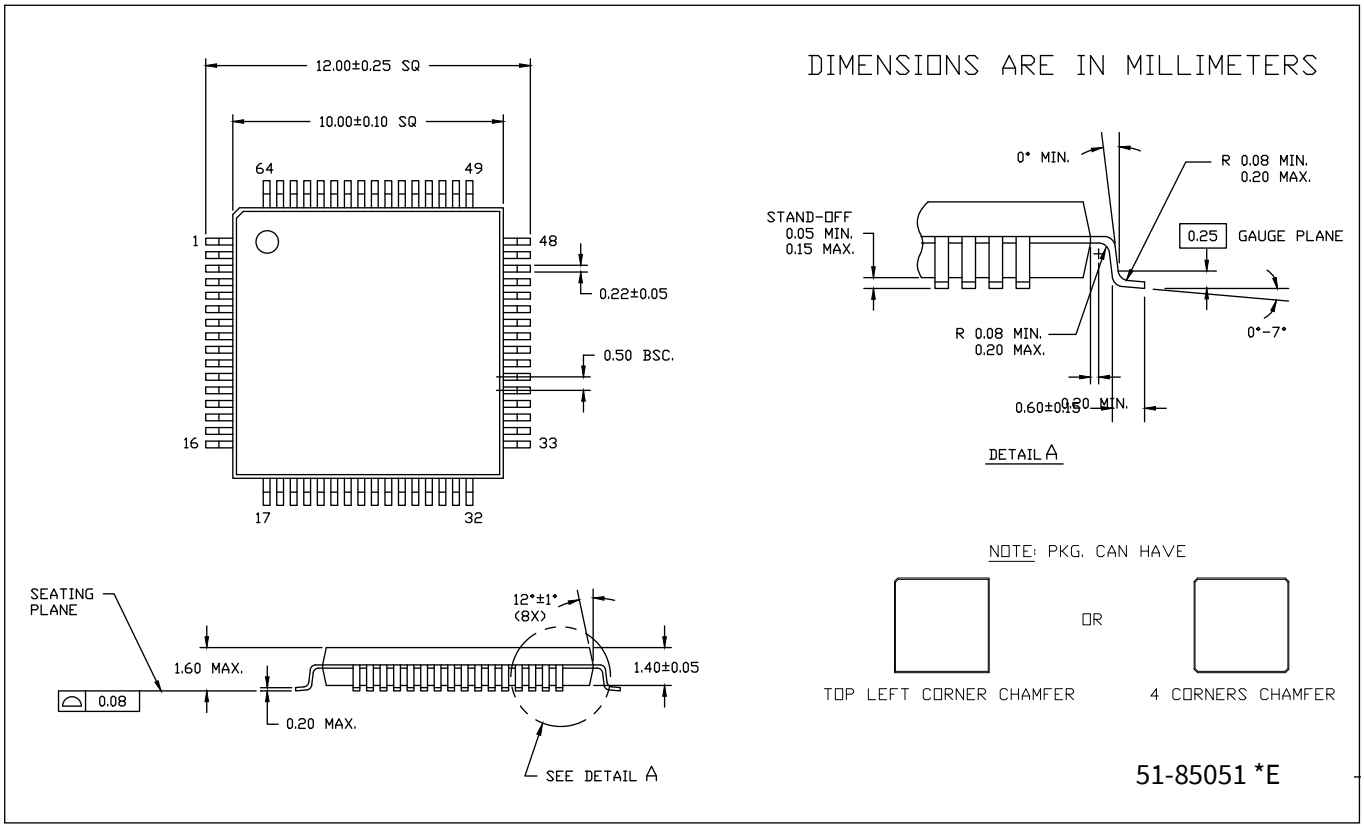


Figure 10 64LD TQFP (10 × 10 × 1.4 mm) A64SB (PG-TQFP-64) package outline

8 Acronyms

Table 33 Acronyms used in this document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	controller area network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint

Table 33 Acronyms used in this document *(continued)*

Acronym	Description
FS	full-speed
GPIO	general-purpose input/output, applies to a PSOC™ pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	local interconnect network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low voltage detect, see also LVI
LVI	low voltage interrupt, see also HVI
LVTTL	low voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array

Table 33 Acronyms used in this document *(continued)*

Acronym	Description
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus

Table 33 Acronyms used in this document *(continued)*

Acronym	Description
USBIO	USB input/output, PSOC™ pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

9 Document conventions

9.1 Units of measure

Table 34 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kiloohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision history

Document revision	Date	Description of changes
*E	2025-04-10	Published to web.
*F	2025-05-08	Updated application note resources under **Development ecosystem**. Updated **Figure 4** and added **Figure 5**. Updated Spec ID# ‘SID19B’ to ‘SID19’ in **Table 4**. Updated the minimum value for Spec ID# ‘SIDMSC_2C’ in **Table 10**. In **Table 24**, updated Spec ID# ‘SID223’, and added Spec ID# ‘SID223B’. Updated package thermal characteristics in **Table 32**.
*G	2025-05-09	In **Table 24**, added Spec ID# ‘SID223C’ and updated link for KBA.

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