

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC123AF, TC74VHC123AFT, TC74VHC123AFK TC74VHC221AF, TC74VHC221AFT, TC74VHC221AFK

Dual Monostable Multivibrator

TC74VHC123AF/AFT/AFK Retriggerable
TC74VHC221AF/AFT/AFK Non-Retriggerable

The TC74VHC123A/221A are high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C²MOS technology.

There are two trigger inputs, $\overline{A}$ input (negative edge), and B input (positive edge). These inputs are valid for a slow rise/fall time signal ($t_r = t_f = 1$ s) as they are schmitt trigger inputs. This device may also be triggered by using $\overline{CLR}$ input (positive edge).

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor (R_X , C_X). A low level at the $\overline{CLR}$ input breaks this state.

Limits for C_X and R_X are:

External capacitor, C_X : No limit

External resistor, R_X : $V_{CC} = 2.0$ V more than 5 k Ω

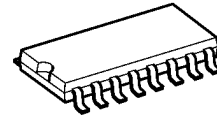
$V_{CC} \geq 3.0$ V more than 1 k Ω

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

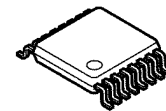
- High speed: $t_{pd} = 8.1$ ns (typ.) at $V_{CC} = 5$ V
- Low power dissipation
Standby state: 4 μ A (max) at $T_a = 25^\circ\text{C}$
Active state: 600 μ A (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Power down protection is equipped with all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC}(\text{opr}) = 2$ to 5.5 V
- Pin and function compatible with 74HC123A/221A

TC74VHC123AF, TC74VHC221AF



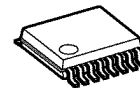
SOP16-P-300-1.27A

TC74VHC123AFT, TC74VHC221AFT



TSSOP16-P-0044-0.65A

TC74VHC123AFK, TC74VHC221AFK



VSSOP16-P-0030-0.50

Weight

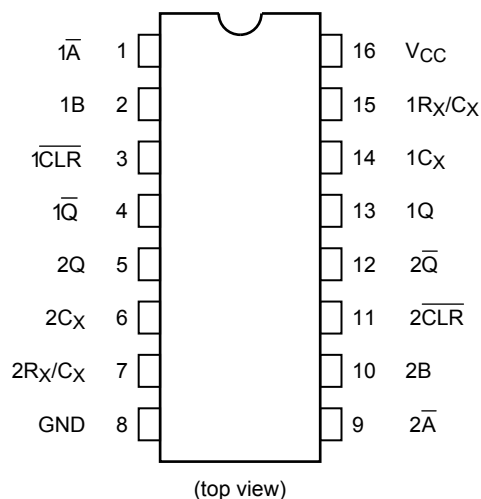
SOP16-P-300-1.27A : 0.18 g (typ.)

TSSOP16-P-0044-0.65A : 0.06 g (typ.)

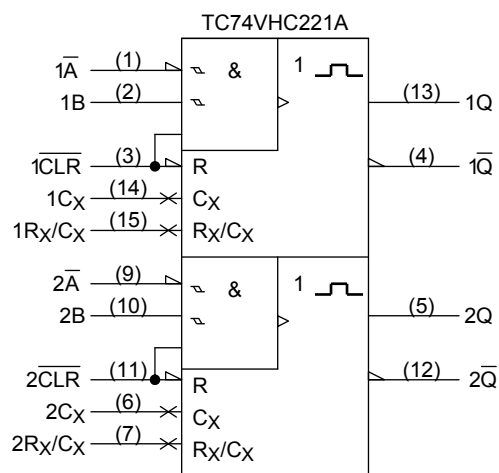
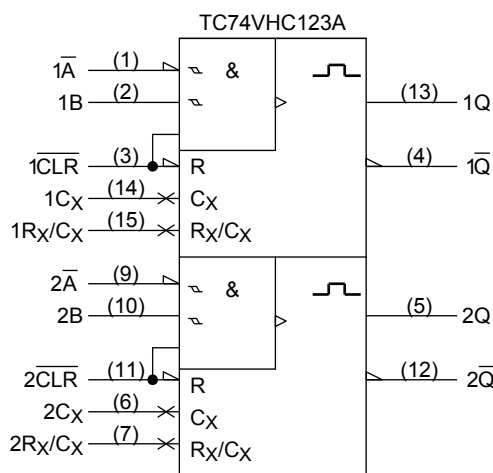
VSSOP16-P-0030-0.50 : 0.02 g (typ.)

Start of commercial production
1991-11

Pin Assignment



IEC Logic Symbol

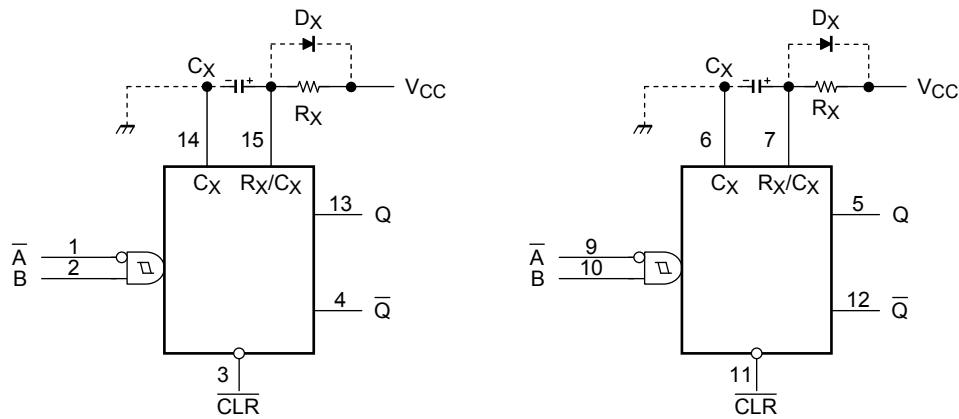


Truth Table

Inputs			Outputs		Function
A	B	CLR	Q	Q	
	H	H			Output Enable
X	L	H	L	H	Inhibit
H	X	H	L	H	Inhibit
L		H			Output Enable
L	H				Output Enable
X	X	L	L	H	Reset

X: Don't care

Block Diagram (Note 1) (Note 2)



Note 1: C_X , R_X , D_X are external capacitor, resistor, and diode, respectively.

Note 2: External clamping diode, D_X ;

The external capacitor is charged to V_{CC} level in the wait state, i.e. when no trigger is applied.

If the supply voltage is turned off, C_X is discharges mainly through the internal (parasitic) diode. If C_X is sufficiently large and V_{CC} drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V_{CC} drops slowly, the in rush current is automatically limited and damage to the IC is avoided.

The maximum value of forward current through the parasitic diode is ± 20 mA.

In the case of a large C_X , the limit of fall time of the supply voltage is determined as follows:

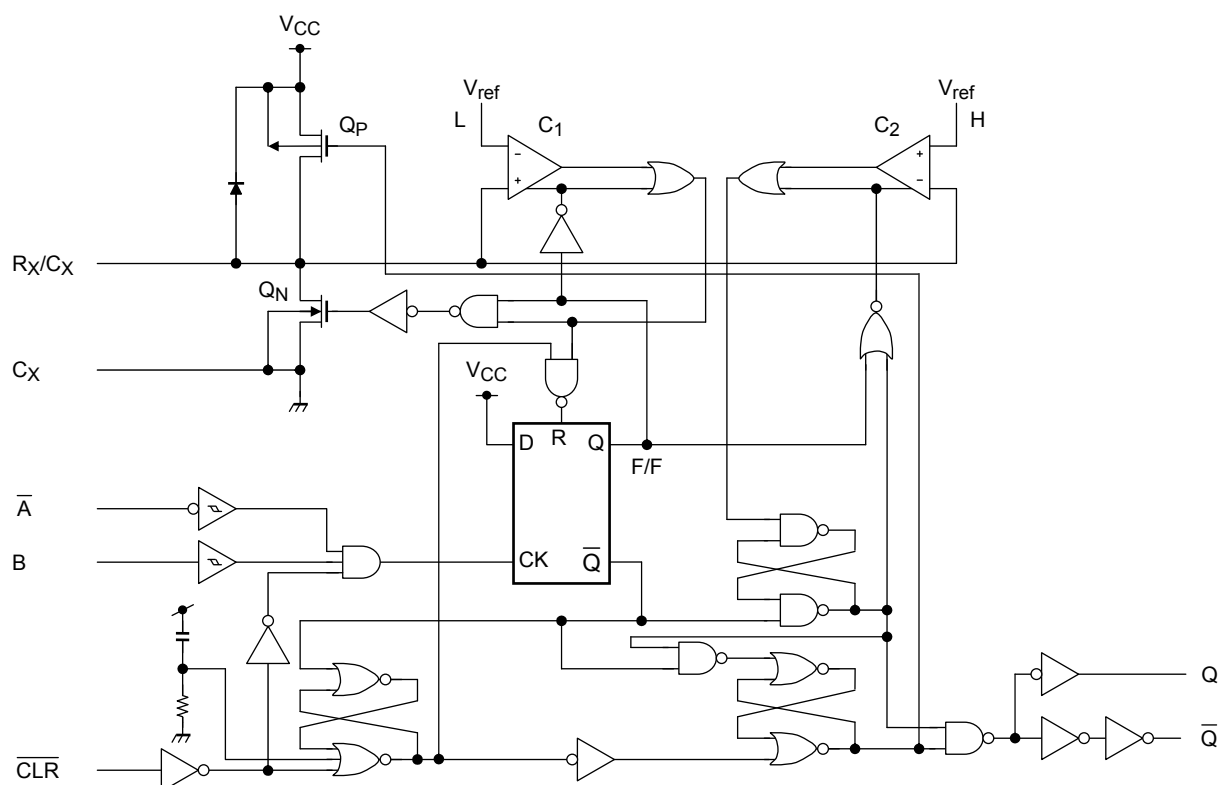
$$t_f \geq (V_{CC} - 0.7) C_X / 20 \text{ mA}$$

(t_f is the time between the supply voltage turn off and the supply voltage reaching $0.4 V_{CC}$.)

In the even a system does not satisfy the above condition, an external clamping diode (D_X) is needed to protect the IC from rush current.

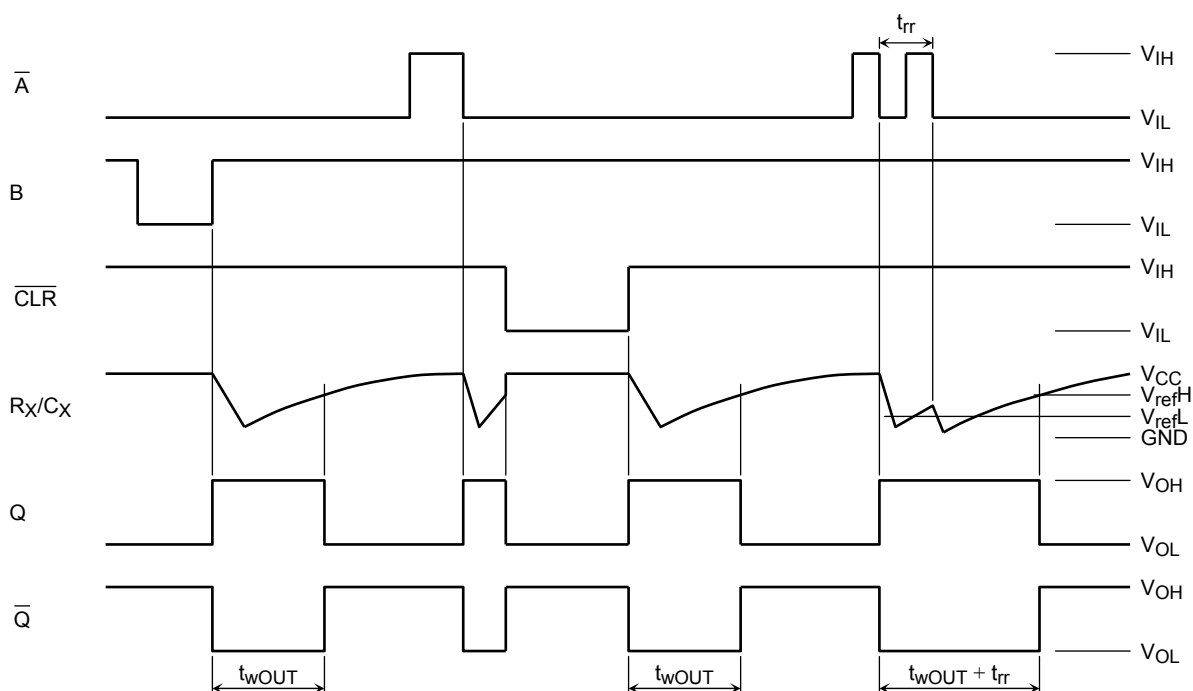
System Diagram

TC74VHC123A



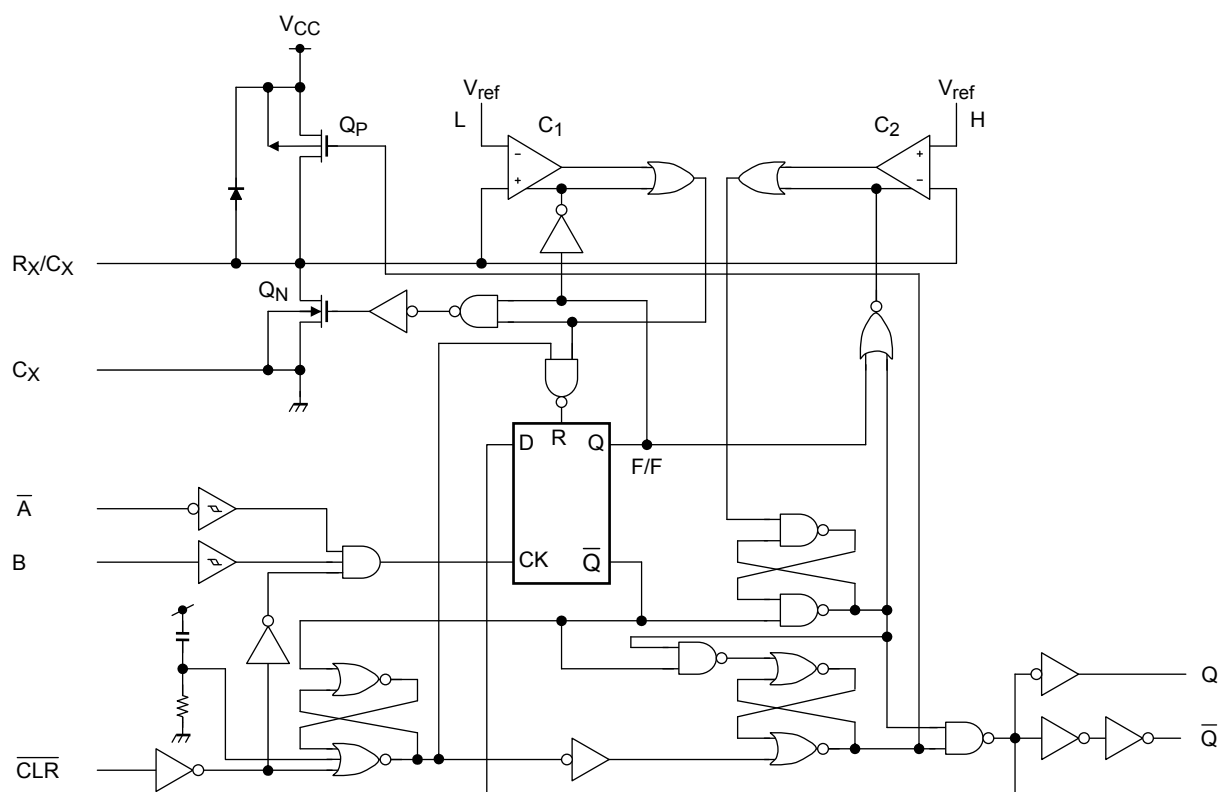
Timing Chart

TC74VHC123A



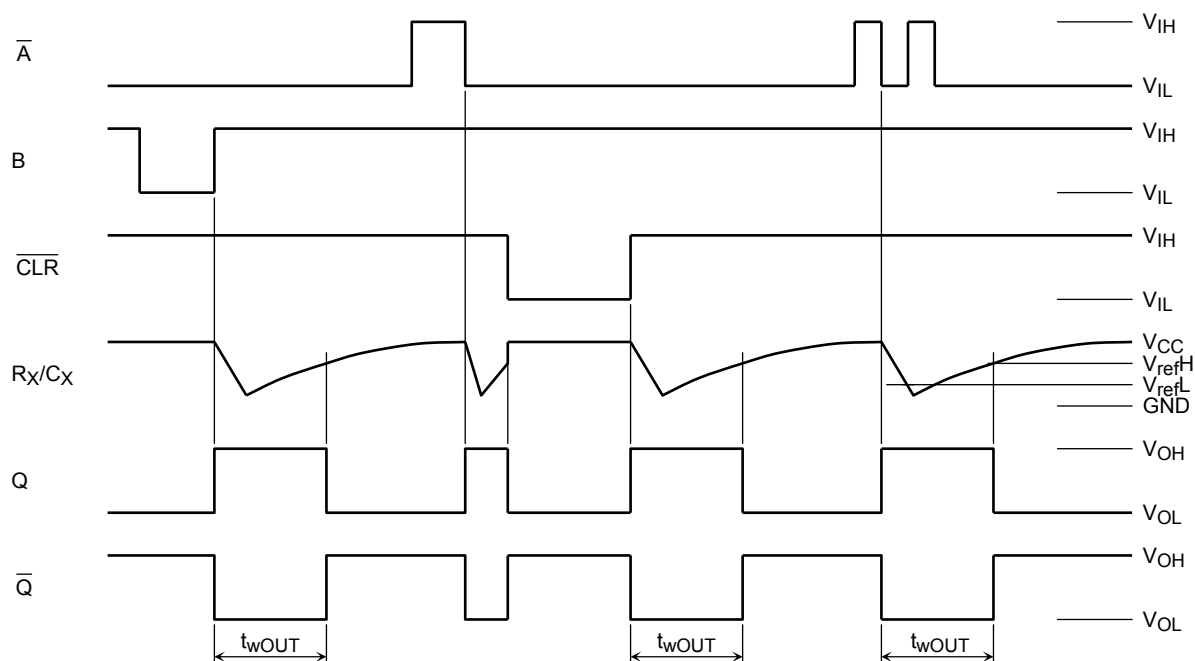
System Diagram

TC74VHC221A



Timing Chart

TC74VHC221A



Functional Description

(1) Standby state

The external capacitor (C_X) is fully charged to V_{CC} in the stand-by state. That means, before triggering, the Q_P and Q_N transistors which are connected to the R_X/C_X node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2) Trigger operation

Trigger operation is effective in any of the following three cases. First, the condition where the $\overline{A}$ input is low, and the B input has a rising signal; second, where the B input is high, and the $\overline{A}$ input has a falling signal; and third, where the $\overline{A}$ input is low and the B input is high, and the $\overline{CLR}$ input has a rising signal.

After a trigger becomes effective, comparators C₁ and C₂ start operating, and Q_N is turned on. The external capacitor discharges through Q_N. The voltage level at the R_X/C_X node drops. If the R_X/C_X voltage level falls to the internal reference voltage V_{refL}, the output of C₁ becomes low. The flip-flop is then reset and Q_N turns off. At that moment C₁ stops but C₂ continues operating.

After Q_N turns off, the voltage at the R_X/C_X node starts rising at a rate determined by the time constant of external capacitor C_X and resistor R_X.

Upon triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of R_X/C_X changes from falling to rising. When R_X/C_X reaches the internal reference voltage V_{refH}, the output of C₂ becomes low, the output Q goes low and C₂ stops its operation. That means, after triggering, when the voltage level of the R_X/C_X node reaches V_{refH}, the IC returns to its MONOSTABLE state.

With large values of C_X and R_X, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, t_w (OUT), is as follows:

$$t_w (\text{OUT}) = 1.0 \cdot C_X \cdot R_X$$

(3) Retrigger operation (TC74VHC123A)

When a new trigger is applied to either input $\overline{A}$ or B while in the MONOSTABLE state, it is effective only if the IC is charging C_X. The voltage level of the R_X/C_X node then falls to V_{refL} level again. Therefore the Q output stays high if the next trigger comes in before the time period set by C_X and R_X.

If the new trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

The minimum time for a trigger to be effective 2nd trigger, t_{rr} (min.), depends on V_{CC} and C_X.

(4) Reset operation

In normal operation, the $\overline{CLR}$ input is held high. If $\overline{CLR}$ is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also, Q_P turns on and C_X is charged rapidly to V_{CC}.

This means if $\overline{CLR}$ is set low, the IC goes into a wait state.

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC} /ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V
External capacitor	C_X	No limitation (Note 2)	F
External resistor	R_X	≥ 5 k ($V_{CC} = 2.0$ V) (Note 2) ≥ 1 k ($V_{CC} \geq 3.0$ V) (Note 2)	Ω

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: The maximum allowable values of C_X and R_X are a function of leakage of capacitor C_X , the leakage of TC74VHC123A/221A, and leakage due to board layout and surface resistance.

Susceptibility to externally induced noise signals may occur for $R_X > 1$ MΩ.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = –40 to 85°C		Unit	
			V _{CC} (V)	Min	Typ.	Max	Min	Max		
High-level input voltage	V _{IH}	—		2.0 3.0 to 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	— —	V
Low-level input voltage	V _{IL}	—		2.0 3.0 to 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = –50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I _{OH} = –4 mA	3.0	2.58	—	—	2.48	—	
I _{OH} = –8 mA	4.5	3.94		—	—	3.80	—			
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I _{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
I _{OL} = 8 mA	4.5	—		—	0.36	—	0.44			
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
R _X /C _X terminal off-state current	I _{IN}	V _{IN} = V _{CC} or GND		5.5	—	—	±0.25	—	±2.5	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	μA
Active-state supply current (Note)	I _{CC}	V _{IN} = V _{CC} or GND		3.0	—	160	250	—	280	μA
		R _X /C _X = 0.5 V _{CC}		4.5	—	380	500	—	650	
				5.5	—	560	750	—	975	

Note: Per circuit

Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit
			V _{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width	$t_w (L)$	—	3.3 ± 0.3	—	5.0	5.0	ns
	$t_w (H)$		5.0 ± 0.5	—	5.0	5.0	
Minimum clear width ($\overline{\text{CLR}}$)	$t_w (L)$	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum retrigger time (Note)	t_{rr}	$R_X = 1 \text{ k}\Omega$ $C_X = 100 \text{ pF}$	3.3 ± 0.3	60	—	—	ns
			5.0 ± 0.5	39	—	—	
		$R_X = 1 \text{ k}\Omega$ $C_X = 0.01 \text{ }\mu\text{F}$	3.3 ± 0.3	1.5	—	—	μs
			5.0 ± 0.5	1.2	—	—	

Note: For TC74VHC123A only

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit		
			VCC (V)	CL (pF)	Min	Typ.	Max	Min	Max			
Propagation delay time ($\overline{A}$, B-Q, $\overline{Q}$)	t _{pLH} t _{pHL}	—	3.3 ± 0.3	15	—	13.4	20.6	1.0	24.0	ns		
				50	—	15.9	24.1	1.0	27.5			
			5.0 ± 0.5	15	—	8.1	12.0	1.0	14.0		1.0	16.0
				50	—	9.6	14.0	1.0	16.0			
Propagation delay time ($\overline{\text{CLR}}$ trigger-Q, $\overline{Q}$)	t _{pLH} t _{pHL}	—	3.3 ± 0.3	15	—	14.5	22.4	1.0	26.0	ns		
				50	—	17.0	25.9	1.0	29.5			
			5.0 ± 0.5	15	—	8.7	12.9	1.0	15.0		1.0	17.0
				50	—	10.2	14.9	1.0	17.0			
Propagation delay time ($\overline{\text{CLR}}$ -Q, $\overline{Q}$)	t _{pLH} t _{pHL}	—	3.3 ± 0.3	15	—	10.3	15.8	1.0	18.5	ns		
				50	—	12.8	19.3	1.0	22.0			
			5.0 ± 0.5	15	—	6.3	9.4	1.0	11.0		1.0	13.0
				50	—	7.8	11.4	1.0	13.0			
Output pulse width	t _{wOUT}	CX = 28 pF RX = 2 kΩ	3.3 ± 0.3	50	—	160	240	—	300	ns		
			5.0 ± 0.5		—	133	200	—	240			
		CX = 0.01 μF RX = 10 kΩ	3.3 ± 0.3	50	90	100	110	90	110	μs		
			5.0 ± 0.5		90	100	110	90	110			
		CX = 0.1 μF RX = 10 kΩ	3.3 ± 0.3	50	0.9	1.0	1.1	0.9	1.1	ms		
			5.0 ± 0.5		0.9	1.0	1.1	0.9	1.1			
Output pulse width error between circuits (in same package)	Δt _{wOUT}	—			—	±1	—	—	—	%		
Input capacitance	C _{IN}	—			—	4	10	—	10	pF		
Power dissipation capacitance	C _{PD}	(Note)			—	73	—	—	—	pF		

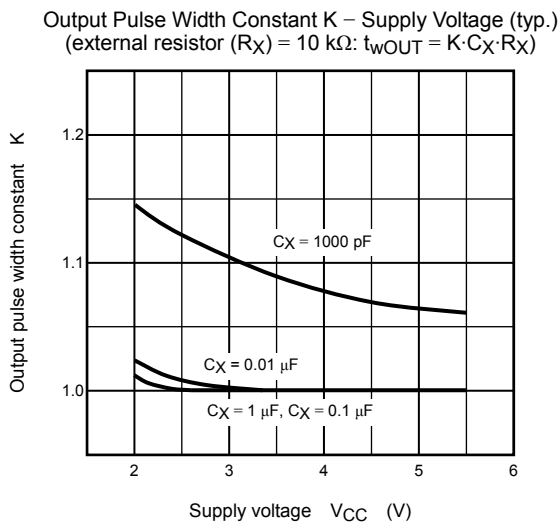
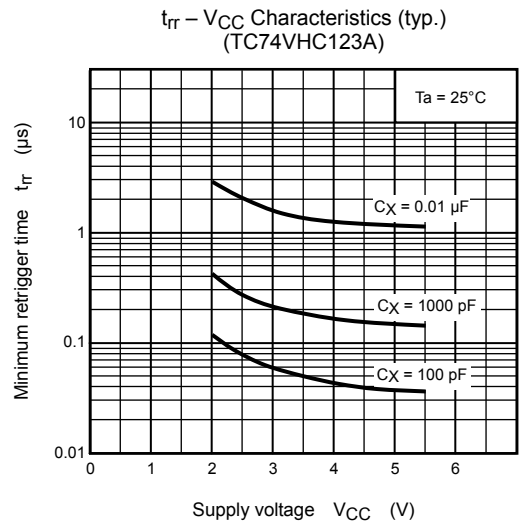
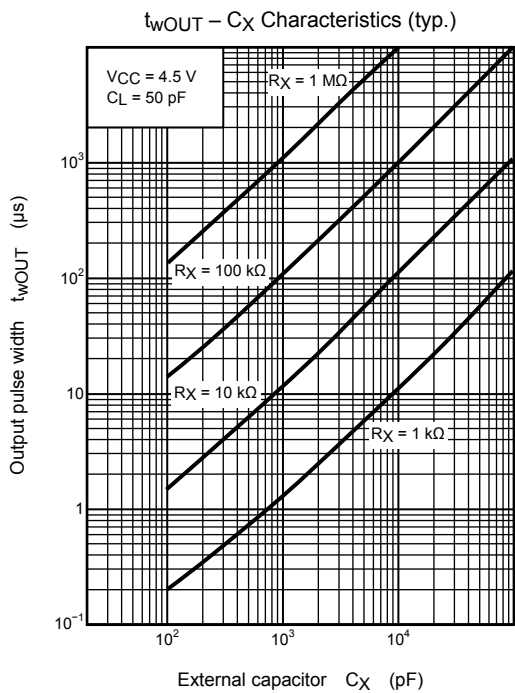
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

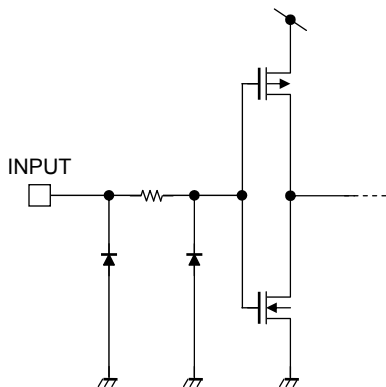
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} \cdot \text{Duty}/100 + I_{CC}/2 \text{ (per circuit)}$$

(I_{CC} : active supply current)

(Duty: %)



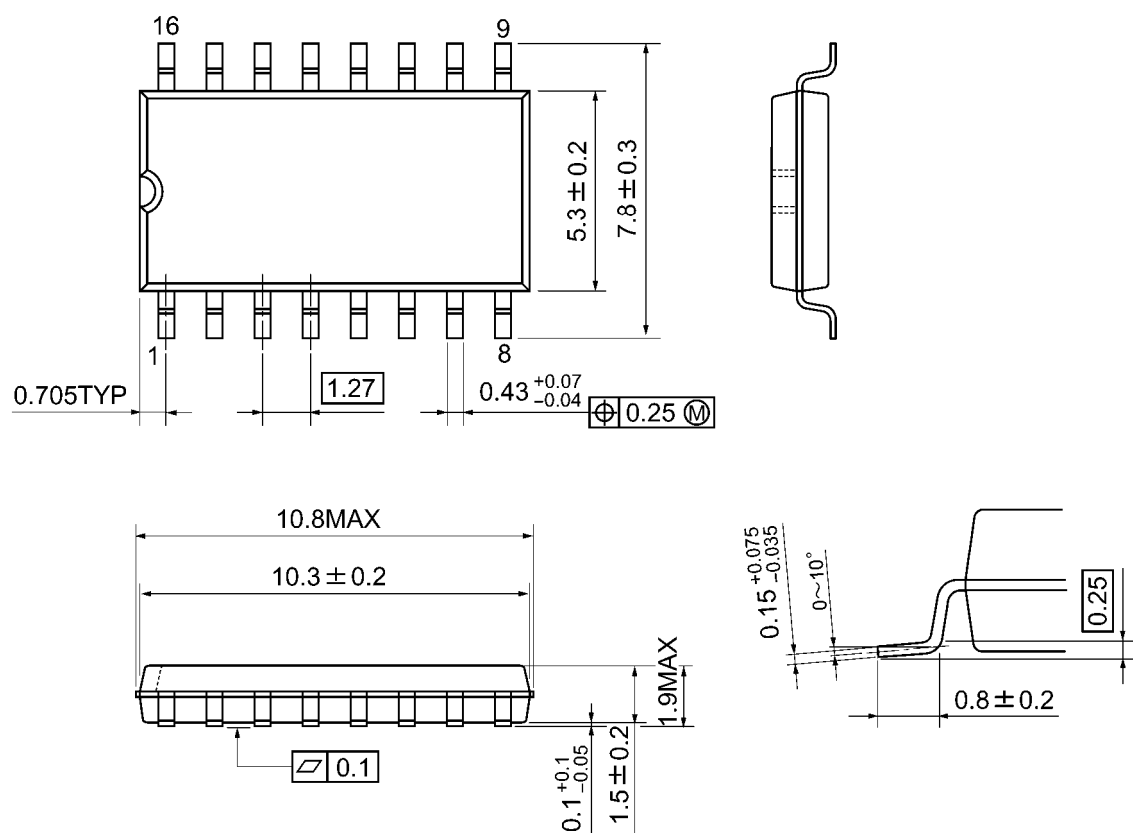
Input Equivalent Circuit



Package Dimensions

SOP16-P-300-1.27A

Unit: mm

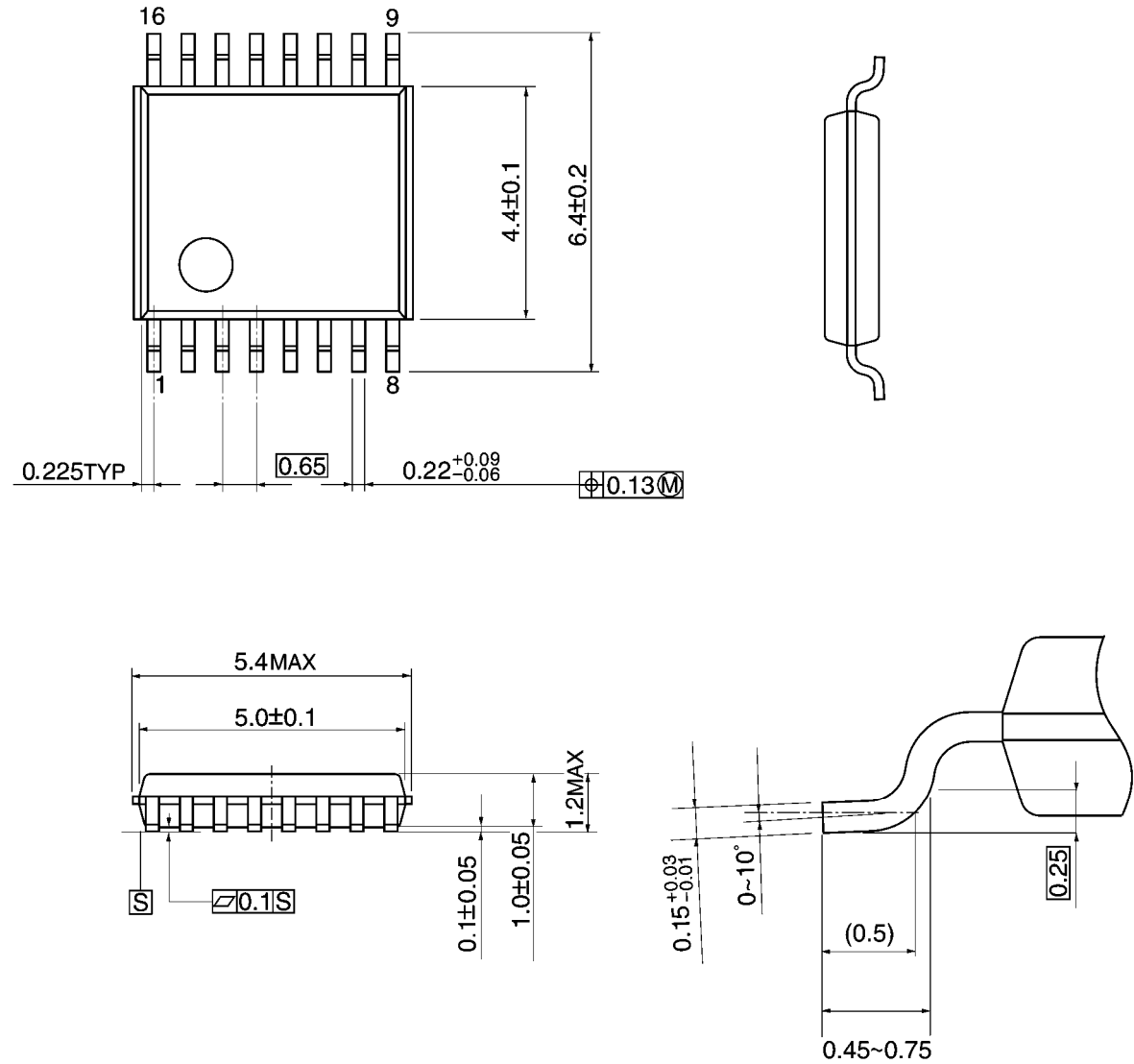


Weight: 0.18 g (typ.)

Package Dimensions

TSSOP16-P-0044-0.65A

Unit: mm

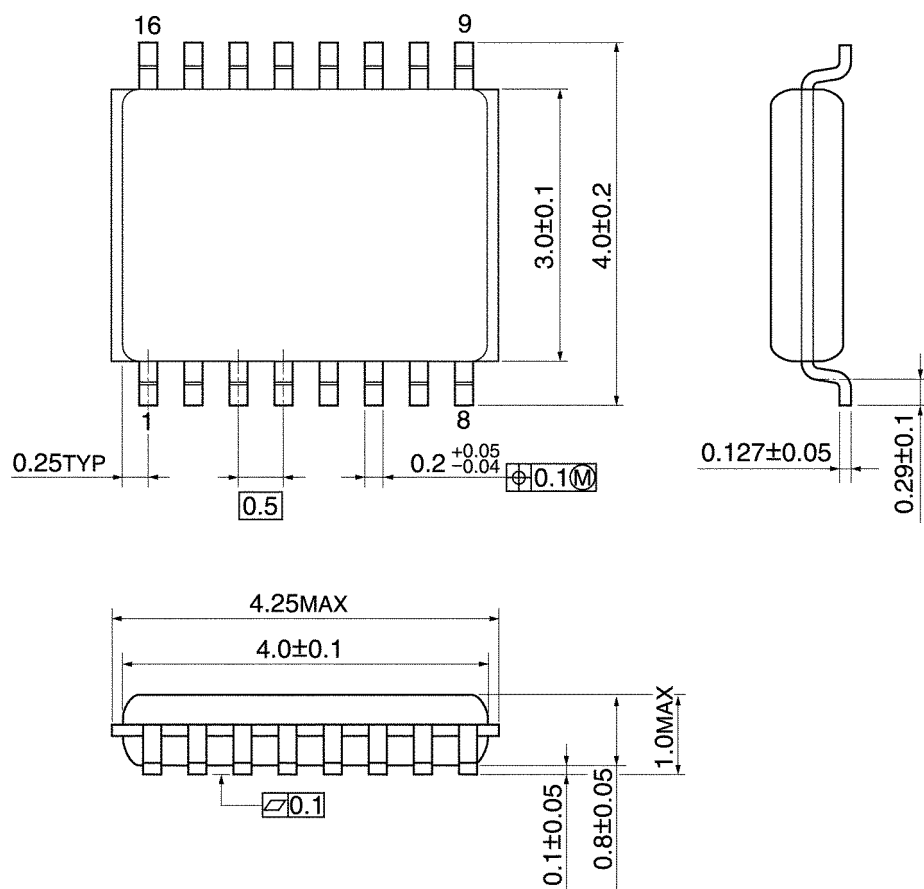


Weight: 0.06 g (typ.)

Package Dimensions

VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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