The documentation and process conversion measures necessary to comply with this document shall be completed by 6 August 2020.

INCH-POUND

MIL-PRF-19500/356M
W/AMENDMENT 1
4 May 2020
SUPERSEDING
MIL-PRF-19500/356M
27 July 2019

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DIODE, SILICON, VOLTAGE REGULATOR,
TYPES 1N4954 THROUGH 1N4996, 1N5968, 1N5969, AND 1N6632 THROUGH 1N6637,
ENCAPSULATED (AXIAL LEADED AND SURFACE MOUNT PACKAGE) AND UNENCAPSULATED,
5, 2, AND 1 PERCENT VOLTAGE TOLERANCE,
QUALITY LEVELS JAN, JANTX, JANTXV, JANS, JANHC AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for silicon, voltage regulator diodes with voltage tolerances of 5 percent, 2 percent, and 1 percent. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device type as specified in MIL-PRF-19500, and two levels of product assurance (JANHC and JANKC) for each unencapsulated device type die.

1.2 Physical dimensions.

1.2.1 Package outlines. The device package outlines are as follows: an axial leaded package in accordance with figure 1 and square end-cap surface mount (US) in accordance with figure 2.

1.2.2 Unencapsulated die. The dimensions and topography for JANHC and JANKC unencapsulated die are in accordance with figures 3 and 4.

1.3 Maximum ratings. Maximum ratings are as shown in maximum test ratings herein (see 3.8) and as follows:

P_T at T_L = +65°C L = .375 inch (9.53 mm)	P_T at T_L = +25°C L = .375 inch (9.53 mm)	P_T at T_{EC} = +140°C	P_T at T_{EC} = +125°C	$P_{T(PCB)}$ at T_A = +55°C	T_J and T_{STG}	Barometric pressure (reduced)
1N4954 through 1N4996	1N5968, 1N5969, 1N6632 through 1N6637	1N4954US through 1N4996US	1N5968US, 1N5969US, 1N6632US through 1N6637US	1N4954, US through 1N4996, US 1N5968, US, 1N5969, US, 1N6632, US through 1N6637, US	1N4954 through 1N4996 1N5968, 1N5969, 1N6632 through 1N6637 including US suffix	1N4954 through 1N4996 1N5968, 1N5969, 1N6632 through 1N6637 including US suffix
(1) 5 W	(2) 5 W	(3) 5 W	(4) 5 W	(5) 0.8 W	-65°C to +175°C	8 mm Hg

See notes on next page.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A

FSC 5961

1.3 Maximum ratings - Continued.

(1) Derate: See figure 5 herein.
(2) Derate: See figure 6 herein.
(3) Derate: See figure 7 herein.
(4) Derate: See figure 8 herein.
(5) For PCB ratings on all surface mount (US) devices, the pads = .061 inch (1.55 mm) x .168 inch (4.27 mm); for the axial-leaded devices, the pads (axial) = .092 inch (2.34 mm) diameter, strip = .030 inch (0.762 mm) x 1 inch (25.4 mm) long, axial lead length L ≤ .187 inch (4.75 mm). Also see application data in 6.7 herein for further details in various copper pad sizes and weights for PCB mounting.

1.4 Primary electrical characteristics. Primary electrical characteristics are as shown in maximum test ratings herein (see 3.8) and as follows:

$R_{\theta JL}$ = 22°C/W (max) L = .375 inch (9.53 mm)	$R_{\theta JL}$ = 30°C/W (max) L = .375 inch (9.53 mm)	$R_{\theta JEC}$ = 7°C/W (max) L = 0 inch	$R_{\theta JEC}$ = 10°C/W (max) L = 0 inch	$R_{\theta JA(PCB)}$ = 150°C/W (see note 5 in 1.3)
1N4954 through 1N4996	1N5968, 1N5969, 1N6632 through 1N6637	1N4954US through 1N4996US	1N5968US, 1N5969US, 1N6632US through 1N6637US	1N4954, US through 1N4996, US 1N5968,US, 1N5969, US, 1N6632, US through 1N6637, US

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs, and 6.6 for supersession information.

1.5.1 JAN certification mark and quality level.

1.5.1.1 Quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".

1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices that are applicable for this specification sheet are "JANHC" and "JANKC".

1.5.2 Device type. The designation system for the devices covered by this specification sheet is as follows.

1.5.2.1 First number and first letter symbols. The devices of this specification sheet use the first number and letter symbols "1N".

1.5.2.2 Second number symbols. The second number symbols for the devices covered by this specification sheet are as follows:

4954	4960	4965	4970	4975	4980	4985	4991	6632
4955	4961	4966	4971	4976	4981	4986	4992	6633
4956	4962	4967	4972	4977	4982	4987	4993	6634
4957	4963	4968	4973	4978	4983	4988	4994	6635
4958	4964	4969	4974	4979	4984	4989	4995	6636
4959		5968	5969			4990	4996	6637

1.5.3 Suffix symbols. The following suffix symbol(s) are incorporated into the PINs for this specification sheet. The package designator suffix symbols (when needed) follow the voltage tolerance suffix symbol.

1.5.3.1 First suffix symbols (voltage tolerance). All devices covered by this specification sheet have a voltage tolerance. Those voltage tolerances are designated by the use a first suffix symbol or no suffix symbol (blank) as indicated as follows.

Blank	Indicates a non-modified version of the diode that have a nominal voltage tolerance of ±5 percent.
C	Indicates a modified version of the diode that have a nominal voltage tolerance of ±2 percent over the basic numbered (non-suffix) device for all types covered by this specification.
D	Indicates a modified version of the diode that have a nominal voltage tolerance of ±1 percent over the basic numbered (non-suffix) device for all types covered by this specification.

1.5.3.2 Second suffix symbol (package designators). The second suffix symbols (or lack thereof) that designate the package outline for the devices covered by this specification sheet are as follows.

Blank	A blank package designator identifies that the package is an axial leaded package (see figure 1).
US	This designator identifies the package is surface mount package with square ends (see figure 2).

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

1.5.5 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "A", "C" and "D" (see 6.5.2 and figures 3 and 4).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 or 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 or 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

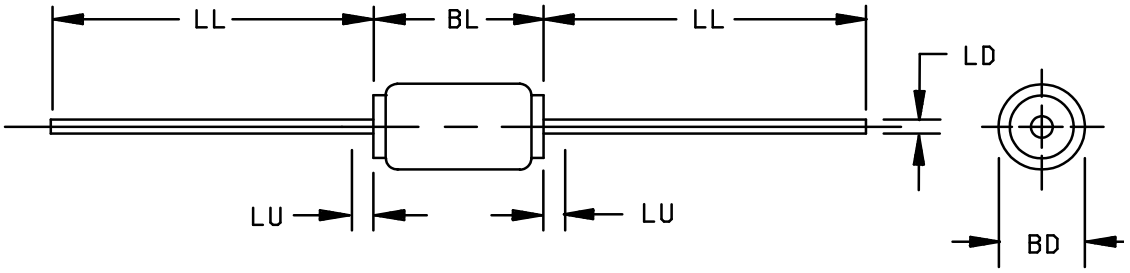
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

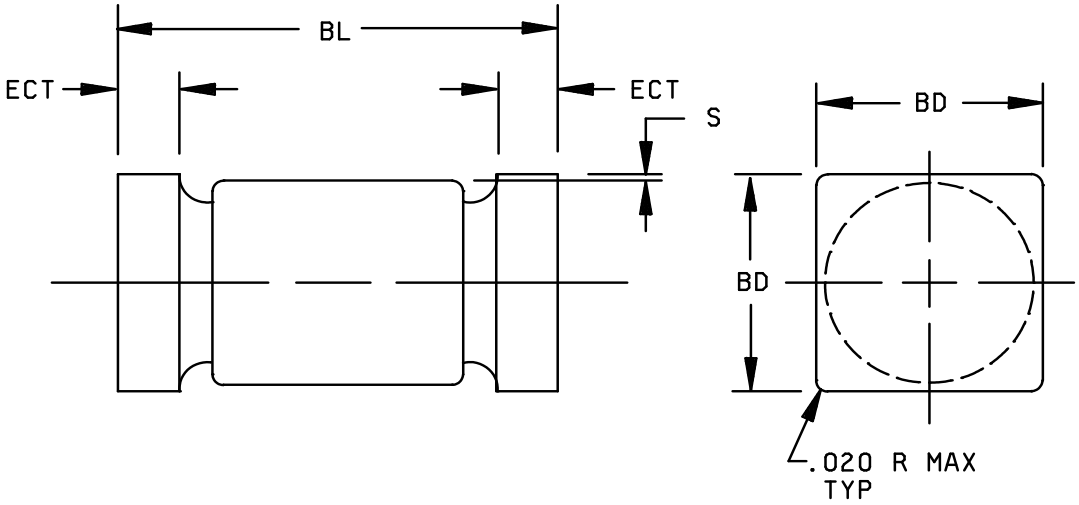
2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



Dimensions					
LTR	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BD	.090	.145	2.29	3.68	3
BL	.130	.300	3.30	7.62	3
LD	.037	.043	0.94	1.09	
LL	1.00	1.300	25.40	33.02	
LU		.050		1.27	4

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Dimensions are pre-solder dip.
3. Package contour optional within dimension BD and length dimension BL. Heat slugs, if any, shall be included within this cylinder length but shall not be subject to minimum limit of dimension BD.
4. The specified lead diameters apply in the zone between .050 inch (1.27 mm) from the diode body and the end of the lead.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

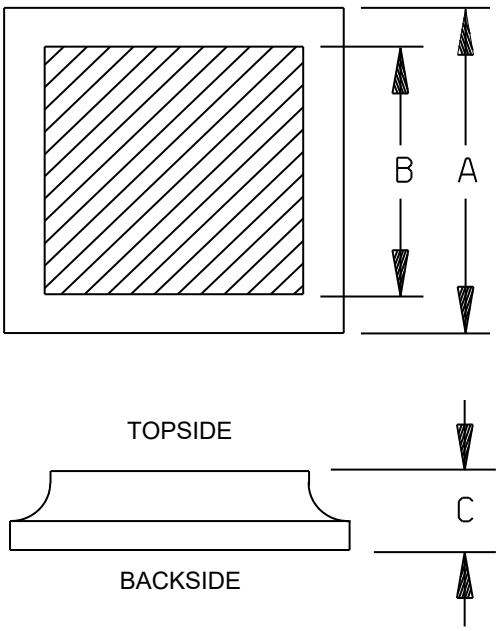
FIGURE 1. Physical dimensions of axial leaded, non-surface mount devices.



Dimensions				
LTRr	Inches		Millimeters	
	Min	Max	Min	Max
BD	.137	.148	3.48	3.76
BL	.200	.225	5.08	5.72
ECT	.019	.028	0.48	0.71
S	.003		0.08	

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Dimensions are pre-solder dip.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions of square ended SMD devices (US).

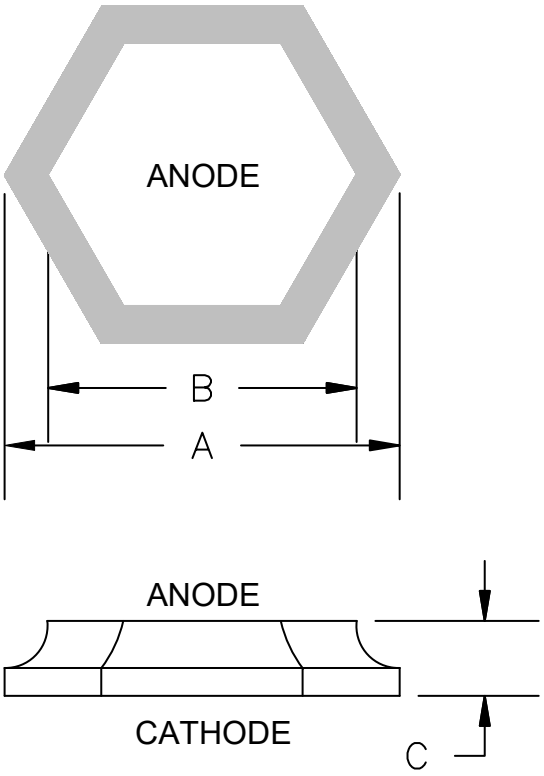


Die versions A and C

LTR	JANHCA and JANKCA				LTR	JANHCC and JANKCC			
	Inches		Millimeters			Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.059 sq	.072 sq	1.50 sq	1.83 sq	A	.062 sq	.064 sq	1.57 sq	1.63 sq
B	.056 sq	.065 sq	1.42 sq	1.65 sq	B	.052 sq	.056 sq	1.32 sq	1.42 sq
C	.006	.012	0.15	0.30	C	.007	.012	0.18	0.30

NOTES:
1. Dimensions are in inches. Metric equivalents are given for general information only.
2. The circuit layout data for JANHCA and JANKCA die are as follows: The backside is the anode and the topside is the cathode for all device types.
3. The metallization characteristics of the JANHCA and JANKCA die are as follow:
   a. Topside – Silver.
   b. Backside – Silver.
   c. See 3.4.3 herein.
4. The circuit layout data for JANHCC and JANKCC die are as follow:
   a. Backside is the anode on device types 1N4954 through 1N4996.
   b. Backside is the cathode on device types 1N5968, 1N5969, and 1N6632 through 1N6637.
5. The metallization characteristics of the JANHCC and JANKCC die are as follow:
   a. Topside – Aluminum.
   b. Backside – Gold.
   c. See 3.4.3 herein.

FIGURE 3. Physical dimensions for JANHC and JANKC die (A and C versions).



Die version D

LTR	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.086	.092	2.18	2.34
B	.069	.075	1.75	1.91
C	.008	.012	0.20	0.30

NOTES:
1. Dimensions are in inches. Metric equivalents are given for general information only.
2. The circuit layout data for JANHCD and JANKD die are as follows: The backside is the cathode and the topside is the anode for all device types.
3. The metallization characteristics of the JANHCD and JANKCD die are as follow:
   a. Topside – Al (34,000 Å minimum).
   b. Backside – Ti/Ni/Ag (1,200Å/1,800Å/30,000Å nominal).
4. See 3.4.3 herein.

FIGURE 4. Physical dimensions JANHC and JANKC die (D version).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500, and as follows.

C suffix	±2 percent voltage tolerance.
D suffix	±1 percent voltage tolerance.
I_{ZM}	Maximum zener current.
I_{ZSM}	Maximum zener surge current.
$V_{Z(reg)}$	Voltage regulation.
Z_K	Knee impedance.
Z_Z	Zener impedance.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1, 2, 3, and 4 herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2). When solder alloy is used for lead finish the maximum lead temperature shall be 175°C max.

3.4.2 Diode construction. All encapsulated devices shall be metallugically bonded, double plug construction, thermally matched, and noncavity in accordance with the requirements of MIL-PRF-19500. The internal construction of "US" version devices shall be structurally identical to the axial leaded type except for lead attachment.

3.4.2.1 Metallurgical bond for diodes with V_Z greater than 6.8 V dc. These devices shall be constructed utilizing category I metallurgical bonds for diodes with V_Z greater than 6.8 V dc as defined in MIL-PRF-19500 shall be utilized.

3.4.2.2 Metallurgical bond for diodes with V_Z less than or equal to 6.8 V dc. These devices shall be constructed utilizing category I or category III metallurgical bonds as defined in MIL-PRF-19500.

3.4.3 JANHC and JANKC metallization. Metallization on JANHC and JANKC is optional and may be specified on the order.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500 and herein.

3.5.1 Marking of US-version devices. At the option of the manufacturer, US-version devices may include laser marking on an end cap, to include part number and lot date code for all levels. JANS levels shall also include serialization. The prefixes JAN, JANTX, JANTXV, or JANS may be abbreviated as J, JX, JV, or JS, respectively. (example: The part number may be reduced to JS4954). All device marking, except for polarity and serial numbers, shall also appear on the unit package used as the initial protection for delivery.

3.5.2 Marking for JANHC and JANKC die. Marking of JANHC and JANKC die shall be in accordance with MIL-PRF-19500.

3.5.3 Polarity of encapsulated devices. The polarity of all encapsulated devices shall be indicated with a contrasting color band to denote the cathode end. Alternatively, for US suffix devices, a minimum of three contrasting color dots spaced around the periphery on the cathode end may be used.

3.5.4 Polarity of JANHC and JANKC devices. Polarity marking is not required on JANHC or JANKC devices. All marking shall be retained on the initial container.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4 and tables I, II, III, and IV.

3.6.1 Selection of tight tolerance devices. The suffix "C" and "D" voltage tolerance devices shall be selected from JAN, JANTX, JANTXV, or JANS devices which have successfully completed all applicable screening, and groups A, B, and C testing as ±5 percent tolerance devices. All sublots of suffix "C" and "D" voltage tolerance devices shall pass table I, subgroup 2 at the tightened tolerances.

3.6.2 Mounting clip tolerance. Tighter tolerances for mounting clip temperature shall be maintained for reference purpose to establish correlation. For suffix "C" and "D" voltage tolerance devices, T_A = +25°C ±2°C at .375 inch (9.53 mm) from body for leaded devices, or zero inches for surface mount devices or equivalent.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I herein.

3.8 Maximum and primary characteristics test ratings. The maximum and primary characteristics test ratings for the voltage regulator diodes shall be as specified in table IV herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspection. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4, and tables I, II, III, and IV).

d. Element evaluation of unencapsulated die (see 4.6).

4.1.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-PRF-19500 and herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed herein for qualification or requalification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot to this revision to maintain qualification.

4.2.2 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with appendix G of MIL-PRF-19500.

4.3 Screening of encapsulated devices (quality levels JANS, JANTX, and JANTXV only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance, see 4.3.1	Thermal impedance, see 4.3.1
9	I_{R1} and V_Z	Not applicable
10	100 percent	Not applicable
11	I_{R1} and V_Z, ΔI_{R1} ≤ ±100 percent of initial reading or 250 nA dc, whichever is greater. ΔV_Z ≤ ±2.5 percent of initial reading	I_{R1} and V_Z
12	Required, see 4.3.2	Required, see 4.3.2
13	Required, subgroups 2 and 3 of table I herein; ΔI_{R1} (max) ≤ ±100 percent of initial reading or 250 nA, whichever is greater; ΔV_Z ≤ ±2.5 percent of initial reading, scope display, see 4.5.5 herein	Required, subgroups 2 of table I herein; ΔI_{R1} (max) ≤ ±100 percent of initial reading or 25 percent of column 12 of table IV (1N6632 - 1N4964); 250 nA (1N4965 - 1N4996), whichever is greater, ΔV_Z ≤ ±2.5 percent of initial reading
14a	Not applicable	Not applicable
(2) 14b	Required	Required

(1) Thermal impedance may be performed any time after sealing provided temperature cycling is performed in accordance with MIL-PRF-19500, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.
(2) For clear glass diodes, the test for hermetic seal (gross leak) may be performed at any time after temperature cycling.

4.3.1 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 of MIL-STD-750, as applicable, using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, t_{MD} (V_C and V_H where appropriate). See table II, subgroup 4 herein.

4.3.2 Free air power burn-in conditions. The power burn-in conditions shall be in accordance with condition B of method 1038 of MIL-STD-750. The details of 4.5.2 and those that follows shall apply: T_A = 75°C maximum. Adjust I_Z or T_A to achieve the required T_J, and $I_{Z(min)}$ shall be ≥ 25 percent of column 8 of table IV. T_J = 135°C minimum. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500, and table I herein. Electrical measurements (end-points) shall be in accordance with the applicable steps of table III herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX and JANTXV) of MIL-PRF-19500, and as follows. Electrical measurements (end-points) and delta measurements shall be in accordance with the applicable steps of table III herein.

4.4.2.1 Quality level JANS.

Subgroup	Method	Conditions
B4	1037	I_Z = 40 percent of column 8 of table IV.
B5	1027	I_Z = 35 percent of column 8 of table IV. Adjust either T_A or I_Z or both to achieve T_J = +175°C minimum, t = 1,000 hours. Temporary leads may be added for surface mount devices. n = 45, c = 0.

4.4.2.2 Quality levels JAN, JANTX and JANTXV.

Subgroup	Method	Conditions
B2	1071	Test condition E only. NOTE: For non-transparent devices, hermetic seal may be performed after electrical measurements.
B3	1027	The test current I_Z shall be adjusted to produce a junction temperature of +150°C minimum and $I_{Z(min)} \geq 25$ percent of column 8 (I_Z) of table IV. Temporary leaded samples from the same lot may be used in lieu of the US suffix sample life test.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and as follows. Electrical measurements (end-points) and delta measurements shall be in accordance with the applicable steps of table III herein.

Subgroup	Method	Conditions
C2	1056	0°C to +100°C, 15 cycles, n = 22 c = 0.
C2	1051	−55°C to +175°C, 25 cycles, n = 22 c = 0.
C2	2036	Tension - test condition A; 20 pounds (9.07 kg); t = 15 s ±3 s. Lead fatigue - test condition E. NOTE: Not applicable to US versions.
C2	2038	US devices - Condition B, 20 pounds (9.07 kg), t = 15s.
C5	4081	See 4.3.1.
C6	1027	The test current I_Z shall be adjusted to produce a junction temperature of +150°C minimum and $I_{Z(min)} \geq 25$ percent of column 8 (I_Z) of table IV. Temporary leaded samples from the same lot may be used in lieu of the US suffix sample life test.
C8	4071	See 4.5.6 herein. I_Z = column 5 of table IV, T_1 = +25°C ±5°C, T_2 = +125°C ±5°C. n = 22, c = 0. The maximum limits are column 13 of table IV.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and table II herein. Delta electrical measurements (end-points) shall be as specified in table III.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of MIL-STD-750.

4.5.2 Free-air burn-in. The use of a current limiting or ballast resistors is permitted provided that each DUT still sees at least the $I_{Z(min)}$ described in 4.3.2 and that the minimum applied voltage, where applicable, is maintained throughout the burn-in period. Use method 3100 of MIL-STD-750 to measure T_J.

4.5.3 Maximum zener surge current (I_{ZSM}). The test for maximum zener surge current shall be performed in accordance with condition B of test method 4066 of MIL-STD-750. The peak currents specified in column 10 of table IV shall be applied in the reverse direction and shall be superimposed on the current (I_Z = column 5 of table IV) a total of five (5) surges at 1 minute intervals. Each individual surge shall be at one-half square wave pulse of 8.3 ms duration or an equivalent sine wave with the same effective (rms) current.

4.5.4 Regulator voltage (V_Z) measurements. The regulator voltage shall be measured in accordance with method 4022 of MIL-STD-750, except that the test shall be performed by the pulse method with tp = 0.2 ms to 300 ms. The thermal equilibrium requirement does not apply. For JANHC and JANKC, this measurement shall be made with the die resting on a metal heat sink maintained at +25°C ±3°C. For tight tolerance suffix "C" and "D" voltage tolerance devices, see 3.6.1 herein.

4.5.5 Scope display. The scope display inspection shall be conducted in accordance with condition B (sharp and stable) of method 4023 of MIL-STD-750.

4.5.5.1 Scope display evaluation. Scope display evaluation shall be performed on a scope. The reverse current (I_{BR}) over the knee shall be 500 µA peak.

4.5.5.2 Scope display option. At the suppliers option, 100 percent scope display evaluation may be discontinued after three consecutive lots are 100 percent tested with zero failures. Any group A failure shall require 100 percent scope display to be reinvoked.

4.5.6 Temperature coefficient of regulator voltage (α_{VZ}). The temperature coefficient of regulator voltage shall be measured in accordance with test method 4071 of MIL-STD-750. The device shall be temperature stabilized with current applied prior to reading regulator voltage at the ambient temperature specified in subgroup 7 of table I.

4.5.7 Voltage regulation ($V_{Z(reg)}$). The breakdown voltage shall be measured at I_Z = 10 percent of column 8 of table IV and at I_Z = 50 percent of column 8 of table IV. The difference between these voltages shall then be determined and shall not exceed column 9 of table IV. The voltage measurement at I_Z = 10 percent of column 8 of table IV shall be a pulse measurement in accordance with 4.5.1. The measurement at I_Z = 50 percent of column 8 of table IV shall be made after current has been applied for 30 ±3 seconds. For this time interval, the axial leaded device shall be suspended in free air by its leads with mounting clips with inside edge .375 inch (9.53 mm) from the body, and the point of connection shall be maintained at a temperature of +25°C, +8°C, −2°C. No forced air across the device shall be permitted. US suffix devices shall be mounted with the end-caps maintained at +25°C, +8°C, −2°C. For JANHC and JANKC, the die shall be stabilized at +25°C and the test shall be performed utilizing pulse conditions. The ΔV_Z measurement may be performed after a shorter time interval following application of the test current if correlation can be established to the satisfaction of the qualifying activity.

4.6 Element evaluation of unencapsulated die. The element evaluation of unencapsulated die shall be in accordance with appendix G of MIL-PRF-19500. For subgroup 4, the burn-in duration for the JANKC level shall follow the JANS requirements and the JANHC shall follow the JANTX requirements.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance	3101	See 4.3.1.	$Z_{\theta JX}$			°C/W
1N4954 through 1N4996					1.8	
1N5968 and 1N5969					3.0	
1N6632 through 1N6637					3.0	
Forward voltage	4011	Condition A or B, I_F = 1 A dc.	V_F		1.5	V dc
Reverse current	4016	DC method; V_R = column 11 of table IV herein.	I_{R1}		Column 12 of table IV	µA dc
Regulator voltage	4022	I_Z = column 5 of table IV herein; 0.2 ms ≤ t_p ≤ 300 ms. (pulsed) (see 4.5.1 and 4.5.4)	V_Z	Column 3 of table IV	Column 4 of table IV	V dc
Subgroup 3						
High temperature operation:		T_A = +150°C.				
Reverse current	4016	DC method; V_R = column 11 of table IV herein; pulsed (see 4.5.1).	I_{R2}		Column 14 of table IV	µA dc
Subgroup 4						
Small-signal reverse breakdown impedance	4051	I_Z = column 5 of table IV herein; I_{sig} = 10 percent of I_Z.	Z_Z		Column 6 of table IV	ohms
Knee impedance	4051	I_{ZK} =column 14 of table IV herein; I_{sig} = 10 percent of I_{ZK}	Z_{ZK}		Column 7 of table IV	ohms
Scope display	4023	See 4.5.5.				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Not applicable						
Subgroup 6						
Surge current	4066	Condition B, I_{ZSM} = column 10 of table IV herein; five surges, 1 per minute, 1/120 second duration superimposed on I_Z = column 5 of table IV (see 4.5.3).	I_{ZSM}			
End-point electrical measurements		See table III, steps 1 and 2				
Subgroup 7						
Voltage regulation		See 4.5.7.	$V_{Z(reg)}$		Column 9 of table IV	V dc
Temperature coefficient of regulator voltage	4071	JANS level only I_Z = column 5 of table IV herein; T_1 = +25°C ±5°C; T_2 = +120°C ≤ T_2 ≤ +130°C (see 4.5.6)	α_{VZ}		Column 13 of table IV	%/°C

1/ For sampling plan, see MIL-PRF-19500.

TABLE II. Group E inspection (all quality levels except die) - for qualification and requalification only.

Inspection 1/ 2/	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			22 devices, c = 0
Thermal shock	1056	20 cycles, condition D except low temperature shall be achieved using liquid nitrogen (−195°C). Perform a visual inspection for cracked glass.	
Temp cycling	1051	−65°C to +175°C, 500 cycles.	
Hermetic seal	1071		
Electrical measurements		See table III, steps 1, 2, 3, 4, 5, 6, and 7.	
Subgroup 2			22 devices, c = 0
Intermittent operation life	1037	I_Z = 40 percent of column 8 of table IV herein; T_L = +95°C minimum, L = .375 inch (9.53 mm), ton = toff = 3 minutes minimum for 10,000 cycles. No heat sink or forced air cooling on the devices shall be permitted.	
Electrical measurements		See table III, steps 1, 2, 3, 4, 5, 6, and 7.	
Subgroup 4			N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			22 devices, c = 0
Barometric pressure (reduced)	1001	V_R = column 11 of table IV herein, (1N4990 - 1N4996 only) pressure = 8 mm Hg.	
Subgroup 6			
Not applicable			
Subgroup 8			
Not applicable			
Subgroup 9			n = 45
Resistance to glass cracking	1057	Condition B. Step stress to destruction by increased cycles or up to a maximum of 25 cycles.	

1/ Unless otherwise specified, for sampling plan, see MIL-PRF-19500.
2/ A separate sample may be pulled for each test.

TABLE III. Groups A, B, C, and E electrical and delta measurements. 1/ 2/ 3/ 4/

Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Reverse current	4016	DC method; V_R = column 11 of table IV herein	I_{R1}		Column 12 of table IV	µA dc
2.	Regulator voltage (see 4.5.4)	4022	I_Z = column 5 of table IV herein	V_Z	Column 3 of table IV	Column 4 of table IV	V dc
3.	Small signal breakdown impedance 1N5968 only	4051	I_Z = column 5 of table IV herein, I_{sig} = 10 percent of I_Z I_{SIG} = .5 mA ac	Z_Z		Column 6 of table IV	ohms
4.	Knee impedance	4051	I_{ZK} = column 15 of table IV	Z_{ZK}		Column 7 of table IV	ohms
5.	Forward voltage	4011	Condition B, I_F = 1.0 A dc, pulsed	V_F		1.5	V dc
6.	Forward voltage	4011	Condition B, I_F = 1.0 A dc, pulsed	ΔV_F 5/		≤ 50 mV dc change from previous measured value.	
7.	Thermal impedance	3101	See 4.3.1	$Z_{\theta JX}$			°C/W

1/ The electrical measurements for table E-VIA (JANS) of MIL-PRF-19500 are as follows:
   a. Subgroup 3, see table III herein, steps 1, 2, 3, 4, 5, 6, and 7.
   b. Subgroup 4, see table III herein, steps 1, 2, 3, 4, 5, 6, and 7.
   c. Subgroup 5, see table III herein, steps 1, 2, 3, 4, 5, 6, and 7.

2/ The electrical measurements for table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 are as follows:
   a. Subgroup 2, see table III herein, steps 1, 2, 3, and 7.
   b. Subgroup 3, see table III herein, steps 1, 2, 3, and 7.
   c. Subgroup 6, see table III herein, steps 1, 2, and 3.

3/ The electrical measurements for table E-VII of MIL-PRF-19500 are as follows:
   a. Subgroup 2, see table III herein, steps 1, 2, 3, 4, 5, 6, and 7 (JANS) and 1, 2, 3, and 7 for (JAN, JANTX, and JANTXV).
   b. Subgroup 6, see table III herein, steps 1, 2, 3, 4, 5, 6, and 7 (JANS) and steps 1, 2, 3, and 7 (JAN, JANTX, and JANTXV).

4/ The electrical measurements for table E-IX of MIL-PRF-19500 are as follows:
   a. Subgroup 1, see table III herein, steps 1, 2, 3, 4, 5, 6, and 7.
   b. Subgroup 2, see table III herein, steps 1, 2, 3, 4, 5, 6, and 7.

5/ Devices which exceed the table I limits, for this test, shall not be accepted.

TABLE IV. Test ratings. 1/ 2/ 3/ 4/

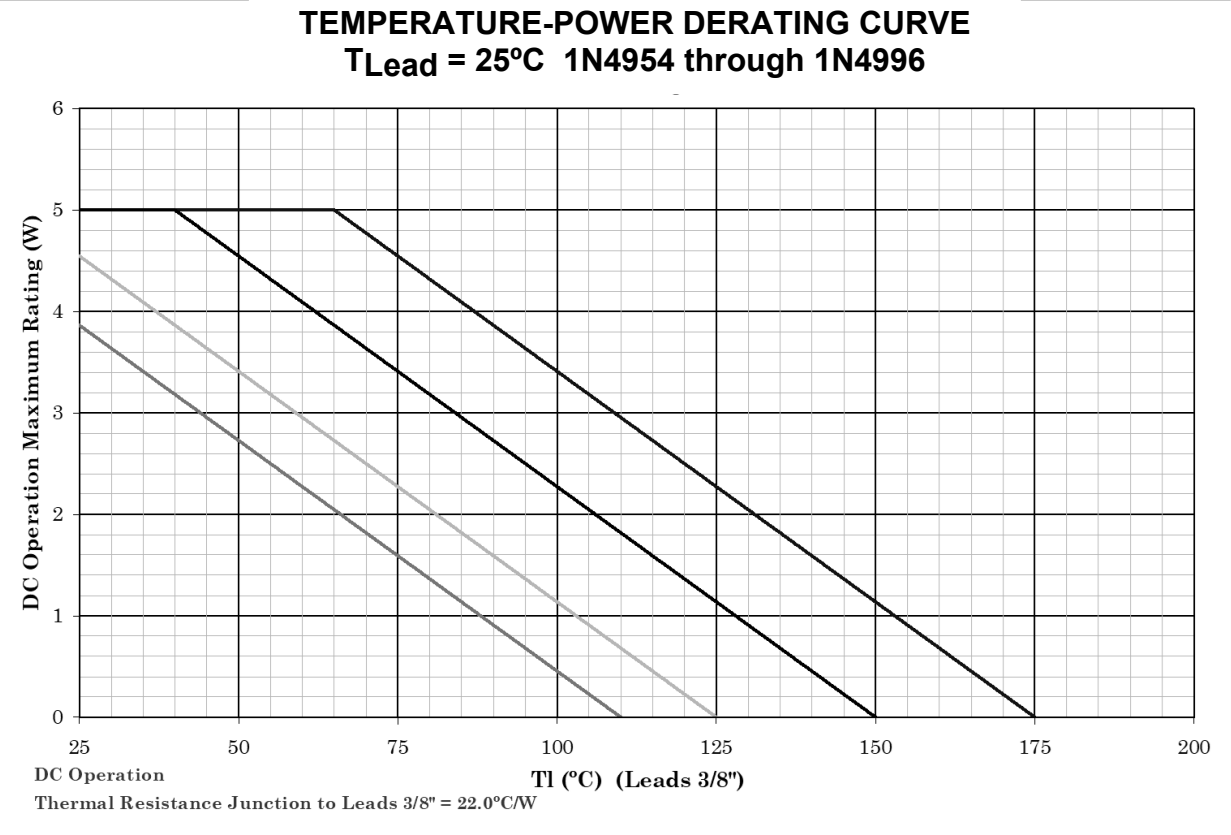
Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10	Col 11	Col 12	Col 13	Col 14	Col 15
Device type	V_Z Nom	V_Z Min 1/ 2/ 3/	V_Z Max 1/ 2/ 3/	I_{ZT} T_A = +25°C	Z_Z	Z_K	I_{ZMax} 4/	$V_{Z(reg)}$ 5/	I_{ZSM} T_A = +25°C 6/	V_R	I_{R1}	α_{VZ}	I_{R2} T_A = +150°C	I_{ZK}
	V	V	V	mA	Ω	Ω	mA dc	V	A	V	µAdc	%/°C	µAdc	mA
1N6632	3.3	3.14	3.46	380	3	500	1,440	.9	20.0	1.0	300	-.075	2,500	5.0
1N6633	3.6	3.42	3.78	350	2.5	500	1,320	.8	18.7	1.0	250	-.070	1,000	5.0
1N6634	3.9	3.71	4.09	320	2	500	1,220	.75	17.6	1.0	175	-.060	500	5.0
1N6635	4.3	4.09	4.51	290	2	500	1,100	.7	16.4	1.0	25	-.050	500	5.0
1N6636	4.7	4.47	4.93	260	2	450	1,010	.6	15.3	1.0	20	±.025	500	5.0
1N6637	5.1	4.85	5.35	240	1.5	400	930	.5	14.4	1.0	5	±.030	500	5.0
1N5968	5.6	5.32	5.88	220	1	400	865	.4	20	4.28	5,000	.040	15,000	5.0
1N5969	6.2	5.89	6.51	220	1	1,000	765	.5	20	4.74	1,000	.040	4,000	1.0
1N4954	6.8	6.46	7.14	175	1	1,000	700	.7	29.3	5.2	150	.05	750	1.0
1N4955	7.5	7.13	7.87	175	1.5	800	630	.7	26.4	5.7	100	.06	500	1.0
1N4956	8.2	7.79	8.61	150	1.5	600	580	.7	24	6.2	50	.06	300	1.0
1N4957	9.1	8.65	9.55	150	2	400	520	.7	22	6.9	25	.06	200	1.0
1N4958	10.0	9.50	10.50	125	2	125	475	.8	20	7.6	25	.07	200	1.0
1N4959	11.0	10.45	11.55	125	2.5	130	430	.8	19	8.4	10	.07	150	1.0
1N4960	12.0	11.40	12.60	100	2.5	140	395	.8	18	9.1	10	.07	150	1.0
1N4961	13.0	12.35	13.65	100	3	145	365	.9	16	9.9	10	.08	150	1.0
1N4962	15	14.25	15.75	75	3.5	150	315	1.0	12	11.4	5.0	.08	100	1.0
1N4963	16	15.20	16.80	75	3.5	155	294	1.1	10	12.2	5.0	.08	100	1.0
1N4964	18	17.10	18.90	65	4.0	160	264	1.2	9.0	13.7	5.0	.085	100	1.0
1N4965	20	19.00	21.00	65	4.5	165	237	1.5	8.0	15.2	2.0	.085	100	1.0
1N4966	22	20.90	23.10	50	5.0	170	216	1.8	7.0	16.7	2.0	.085	100	1.0
1N4967	24	22.8	25.2	50	5	175	198	2.0	6.5	18.2	2.0	.09	100	1.0
1N4968	27	25.7	28.3	50	6	180	176	2.0	6.0	20.6	2.0	.09	100	1.0
1N4969	30	28.5	31.5	40	8	190	158	2.5	5.5	22.8	2.0	.09	100	1.0
1N4970	33	31.4	34.6	40	10	200	144	2.8	5.0	25.1	2.0	.095	100	1.0
1N4971	36	34.2	37.8	30	11	220	132	3.0	4.5	27.4	2.0	.095	100	1.0

See footnotes at end of table.

TABLE IV. Test ratings - Continued. 1/ 2/ 3/ 4/

Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10	Col 11	Col 12	Col 13	Col 14	Col 15
Device type	V_Z Nom	V_Z Min 1/ 2/ 3/	V_Z Max 1/ 2/ 3/	I_{ZT} T_A = +25°C	Z_Z	Z_K	I_{ZMax} 4/	$V_{Z(reg)}$ 5/	I_{ZSM} T_A = +25°C 6/	V_R	I_{R1}	α_{VZ}	I_{R2} T_A = +150°C	I_{ZK}
	V	V	V	mA	Ω	Ω	mA dc	V	A	V	µAdc	%/°C	µAdc	mA
1N4972	39	37.1	40.9	30	14	230	122	3.0	4.0	29.7	2.0	.095	100	1.0
1N4973	43	40.9	45.1	30	20	240	110	3.3	3.5	32.7	2.0	.095	100	1.0
1N4974	47	44.7	49.3	25	25	250	100	3.5	3.2	35.8	2.0	.095	100	1.0
1N4975	51	48.5	53.5	25	27	270	92	4.0	3.0	38.8	2.0	.095	100	1.0
1N4976	56	53.2	58.8	20	35	320	84	4.4	2.8	42.6	2.0	.095	100	1.0
1N4977	62	58.9	65.1	20	42	400	76	5.0	2.5	47.1	2.0	.100	100	1.0
1N4978	68	64.6	71.4	20	50	500	70	5.5	2.2	51.7	2.0	.100	100	1.0
1N4979	75	71.3	78.7	20	55	620	63	6.0	2.0	56.0	2.0	.100	100	1.0
1N4980	82	77.9	86.1	15	80	720	58	6.6	1.8	62.2	2.0	.100	100	1.0
1N4981	91	86.5	95.5	15	90	760	52.5	7.5	1.6	69.2	2.0	.100	100	1.0
1N4982	100	95.0	105	12	110	800	47.5	8.0	1.4	76.0	2.0	.100	100	1.0
1N4983	110	104.5	115.5	12	125	1,000	43	9.0	1.2	83.6	2.0	.100	100	1.0
1N4984	120	114.0	126.0	10	170	1,150	39.5	10	1.0	91.2	2.0	.100	100	1.0
1N4985	130	123.5	136.5	10	190	1,250	36.6	11	.8	98.8	2.0	.105	100	1.0
1N4986	150	142.5	157.5	8	330	1,500	31.6	13	.75	114.0	2.0	.105	100	1.0
1N4987	160	152	168	8	350	1,650	29.4	14	.70	121.6	2.0	.105	100	1.0
1N4988	180	171	189	5	450	1,750	26.4	16	.60	136.8	2.0	.110	100	1.0
1N4989	200	190	210	5	500	1,850	23.6	18	.50	152.0	2.0	.110	100	1.0
1N4990	220	209	231	5	550	2,000	21.6	19	.50	167.0	2.0	.115	100	1.0
1N4991	240	228	252	5	650	2,050	19.8	22	.40	182.0	2.0	.115	100	1.0
1N4992	270	257	283	5	800	2,100	17.5	25	.35	206	2.0	.120	100	1.0
1N4993	300	285	315	4	950	2,150	15.6	28	.30	228	2.0	.120	100	1.0
1N4994	330	314	346	4	1,175	2,200	14.4	32	.25	251	2.0	.120	100	1.0
1N4995	360	342	378	3	1,400	2,300	13.0	35	.22	274	2.0	.120	100	1.0
1N4996	390	371	409	3	1,800	2,500	12.0	40	.20	297	2.0	.120	100	1.0

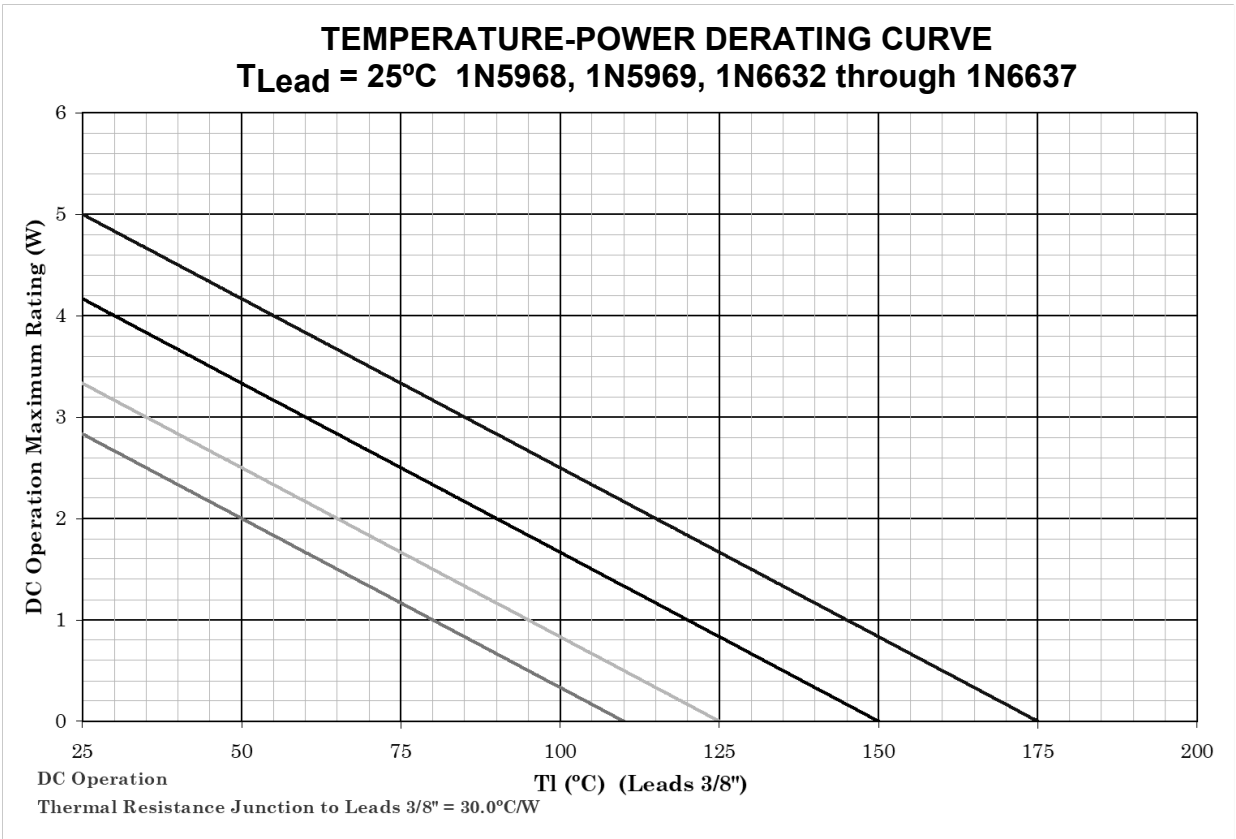
1/ Unless otherwise specified, ratings apply to all case outlines.
2/ Voltage tolerance devices (examples: 1N6632 is ±5 percent, 1N6632C is ±2 percent, and 1N6632D is ±1 percent tolerance).
3/ Min/max shown only for ±5 percent tolerance.
4/ See 1.3 for P_T temperature conditions for lead or end-cap where I_{ZM} is applicable.
5/ See 4.5.7 herein.
6/ See 4.5.3 herein.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C, and 110°C to show power rating where most users want to limit T_J in their application.

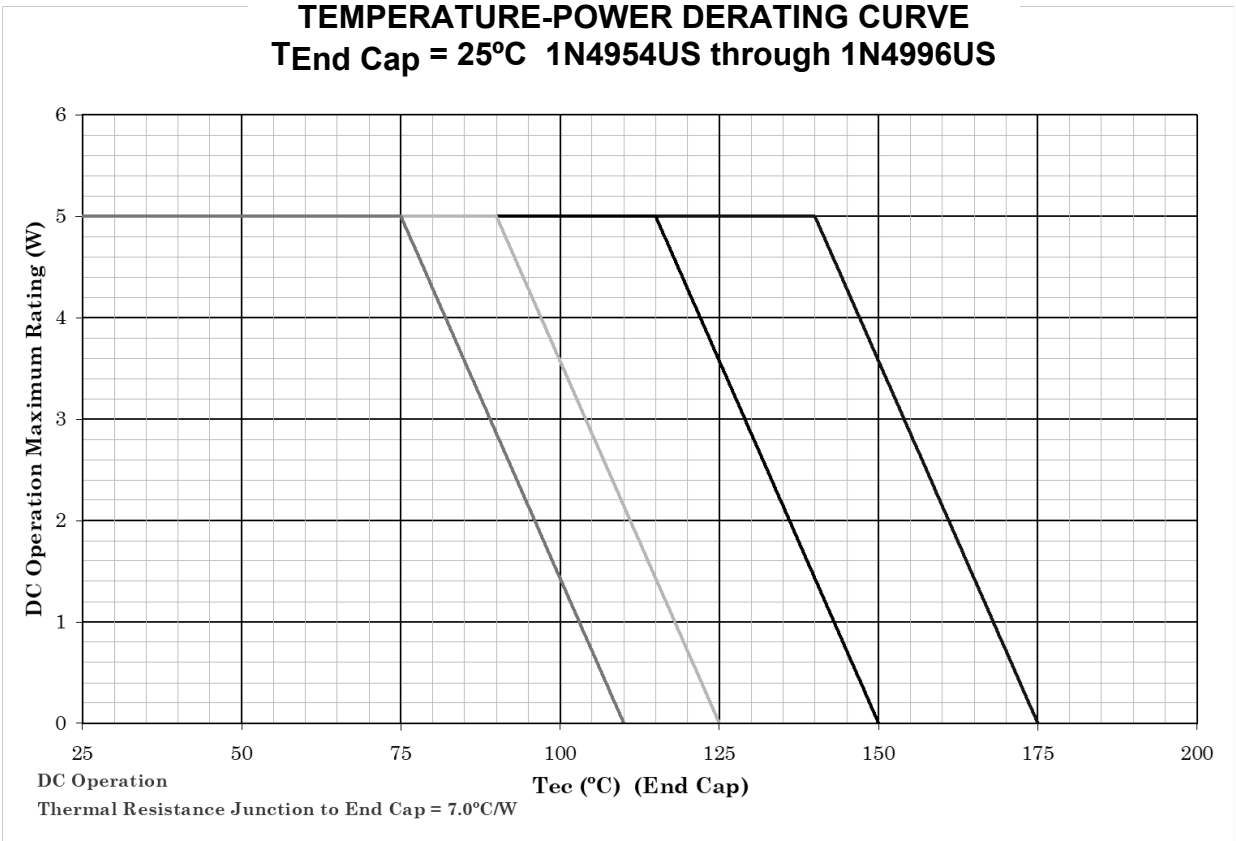
FIGURE 5. Temperature/power derating curve.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C, and 110°C to show power rating where most users want to limit T_J in their application.

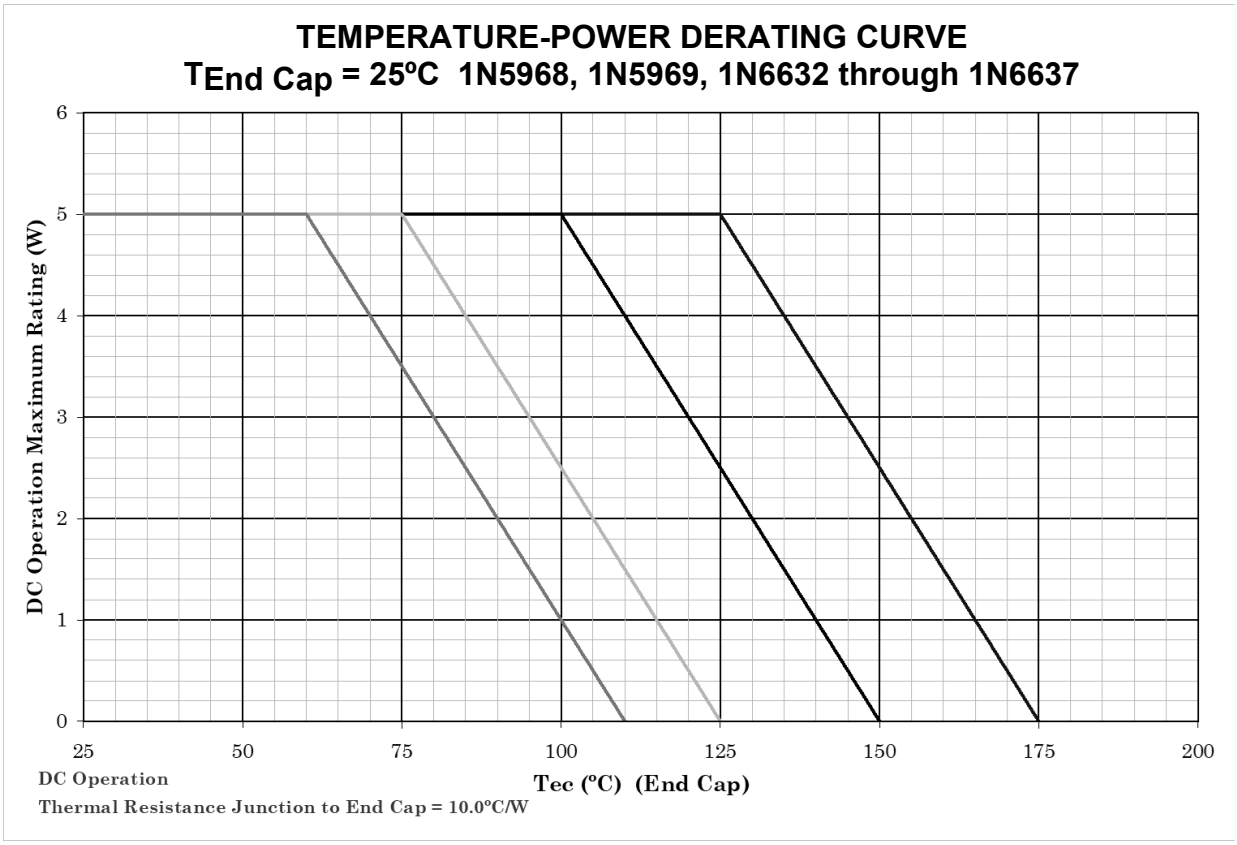
FIGURE 6. Temperature/power derating curve.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 7. Temperature/power derating curve.



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +175°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 8. Temperature/power derating curve.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

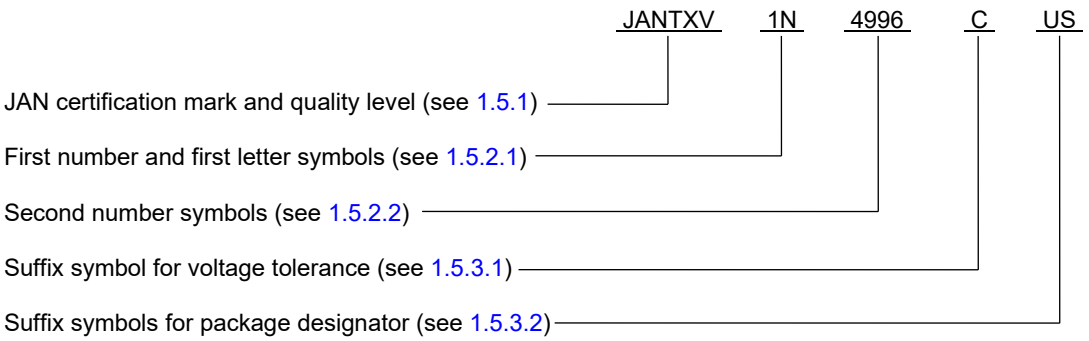
c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.4.

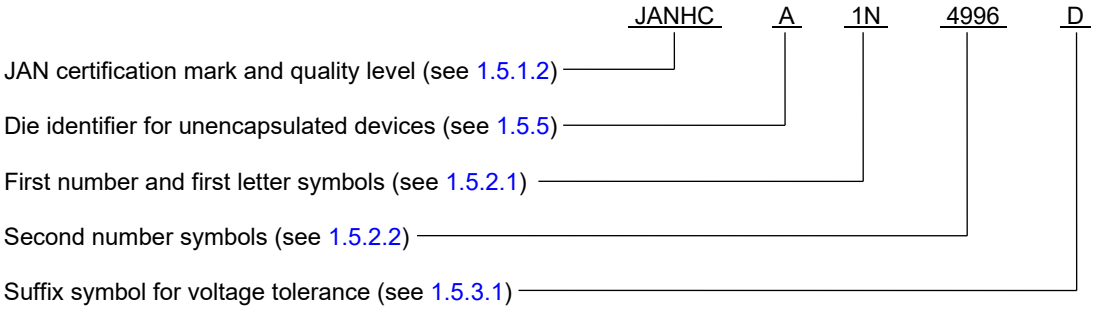
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://qpldocs.dla.mil.

6.4 PIN construction example. The PINs for encapsulated and unencapsulated devices and are constructed using the following forms.

6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.4.2 Unencapsulated devices. The PINs for unencapsulated devices are constructed using the following form.



6.5 List of PINs.

6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs available for encapsulated devices covered by this specification sheet.

PINs for devices of the base quality level (1)	PINs for devices of the "TX" quality level (1)	PINs for devices of the "TXV" quality level (1)	PINs for devices of the "S" quality level (1)
JAN1N4954#@	JANTX1N4954#@	JANTXV1N4954#@	JANS1N4954#@
JAN1N4955#@	JANTX1N4955#@	JANTXV1N4955#@	JANS1N4955#@
JAN1N4956#@	JANTX1N4956#@	JANTXV1N4956#@	JANS1N4956#@
JAN1N4957#@	JANTX1N4957#@	JANTXV1N4957#@	JANS1N4957#@
JAN1N4958#@	JANTX1N4958#@	JANTXV1N4958#@	JANS1N4958#@
JAN1N4959#@	JANTX1N4959#@	JANTXV1N4959#@	JANS1N4959#@
JAN1N4960#@	JANTX1N4960#@	JANTXV1N4960#@	JANS1N4960#@
JAN1N4961#@	JANTX1N4961#@	JANTXV1N4961#@	JANS1N4961#@
JAN1N4962#@	JANTX1N4962#@	JANTXV1N4962#@	JANS1N4962#@
JAN1N4963#@	JANTX1N4963#@	JANTXV1N4963#@	JANS1N4963#@
JAN1N4964#@	JANTX1N4964#@	JANTXV1N4964#@	JANS1N4964#@
JAN1N4965#@	JANTX1N4965#@	JANTXV1N4965#@	JANS1N4965#@
JAN1N4966#@	JANTX1N4966#@	JANTXV1N4966#@	JANS1N4966#@
JAN1N4967#@	JANTX1N4967#@	JANTXV1N4967#@	JANS1N4967#@
JAN1N4968#@	JANTX1N4968#@	JANTXV1N4968#@	JANS1N4968#@
JAN1N4969#@	JANTX1N4969#@	JANTXV1N4969#@	JANS1N4969#@
JAN1N4970#@	JANTX1N4970#@	JANTXV1N4970#@	JANS1N4970#@
JAN1N4971#@	JANTX1N4971#@	JANTXV1N4971#@	JANS1N4971#@
JAN1N4972#@	JANTX1N4972#@	JANTXV1N4972#@	JANS1N4972#@
JAN1N4973#@	JANTX1N4973#@	JANTXV1N4973#@	JANS1N4973#@
JAN1N4974#@	JANTX1N4974#@	JANTXV1N4974#@	JANS1N4974#@
JAN1N4975#@	JANTX1N4975#@	JANTXV1N4975#@	JANS1N4975#@
JAN1N4976#@	JANTX1N4976#@	JANTXV1N4976#@	JANS1N4976#@
JAN1N4977#@	JANTX1N4977#@	JANTXV1N4977#@	JANS1N4977#@
JAN1N4978#@	JANTX1N4978#@	JANTXV1N4978#@	JANS1N4978#@
JAN1N4979#@	JANTX1N4979#@	JANTXV1N4979#@	JANS1N4979#@

See note at end of listing.

6.5.1 List of PINs for encapsulated devices – Continued.

PINs for devices of the base quality level (1)	PINs for devices of the "TX" quality level (1)	PINs for devices of the "TXV" quality level (1)	PINs for devices of the "S" quality level (1)
JAN1N4980#@	JANTX1N4980#@	JANTXV1N4980#@	JANS1N4980#@
JAN1N4981#@	JANTX1N4981#@	JANTXV1N4981#@	JANS1N4981#@
JAN1N4982#@	JANTX1N4982#@	JANTXV1N4982#@	JANS1N4982#@
JAN1N4983#@	JANTX1N4983#@	JANTXV1N4983#@	JANS1N4983#@
JAN1N4984#@	JANTX1N4984#@	JANTXV1N4984#@	JANS1N4984#@
JAN1N4985#@	JANTX1N4985#@	JANTXV1N4985#@	JANS1N4985#@
JAN1N4986#@	JANTX1N4986#@	JANTXV1N4986#@	JANS1N4986#@
JAN1N4987#@	JANTX1N4987#@	JANTXV1N4987#@	JANS1N4987#@
JAN1N4988#@	JANTX1N4988#@	JANTXV1N4988#@	JANS1N4988#@
JAN1N4989#@	JANTX1N4989#@	JANTXV1N4989#@	JANS1N4989#@
JAN1N4990#@	JANTX1N4990#@	JANTXV1N4990#@	JANS1N4990#@
JAN1N4991#@	JANTX1N4991#@	JANTXV1N4991#@	JANS1N4991#@
JAN1N4992#@	JANTX1N4992#@	JANTXV1N4992#@	JANS1N4992#@
JAN1N4993#@	JANTX1N4993#@	JANTXV1N4993#@	JANS1N4993#@
JAN1N4994#@	JANTX1N4994#@	JANTXV1N4994#@	JANS1N4994#@
JAN1N4995#@	JANTX1N4995#@	JANTXV1N4995#@	JANS1N4995#@
JAN1N4996#@	JANTX1N4996#@	JANTXV1N4996#@	JANS1N4996#@
JAN1N5968#@	JANTX1N5968#@	JANTXV1N5968#@	JANS1N5968#@
JAN1N5969#@	JANTX1N5969#@	JANTXV1N5969#@	JANS1N5969#@
JAN1N6632#@	JANTX1N6632#@	JANTXV1N6632#@	JANS1N6632#@
JAN1N6633#@	JANTX1N6633#@	JANTXV1N6633#@	JANS1N6633#@
JAN1N6634#@	JANTX1N6634#@	JANTXV1N6634#@	JANS1N6634#@
JAN1N6635#@	JANTX1N6635#@	JANTXV1N6635#@	JANS1N6635#@
JAN1N6636#@	JANTX1N6636#@	JANTXV1N6636#@	JANS1N6636#@
JAN1N6637#@	JANTX1N6637#@	JANTXV1N6637#@	JANS1N6637#@

(1) The pound sign (#) represents the voltage tolerance suffix "C", "D" or left blank (see 1.5.3.1) and the at-sign (@) represents the package suffix of either a blank or "US" suffix symbol (see 1.5.3.2).

6.5.2 List of PINs for un-encapsulated devices. The following is a list of possible PINs available for encapsulated devices covered by this specification sheet.

PINs for die of quality level JANHC (1)	PINs for die of quality level JANKC (1)	PINs for die of quality level JANHC (1)	PINs for die of quality level JANKC (1)
JANHC@1N4954#	JANKC@1N4954#	JANHC@1N4980#	JANKC@1N4980#
JANHC@1N4955#	JANKC@1N4955#	JANHC@1N4981#	JANKC@1N4981#
JANHC@1N4956#	JANKC@1N4956#	JANHC@1N4982#	JANKC@1N4982#
JANHC@1N4957#	JANKC@1N4957#	JANHC@1N4983#	JANKC@1N4983#
JANHC@1N4958#	JANKC@1N4958#	JANHC@1N4984#	JANKC@1N4984#
JANHC@1N4959#	JANKC@1N4959#	JANHC@1N4985#	JANKC@1N4985#

See note at end of listing.

6.5.2 List of PINs for un-encapsulated devices – Continued.

PINs for die of quality level JANHC (1)	PINs for die of quality level JANKC (1)	PINs for die of quality level JANHC (1)	PINs for die of quality level JANKC (1)
JANHC@1N4960#	JANKC@1N4960#	JANHC@1N4986#	JANKC@1N4986#
JANHC@1N4961#	JANKC@1N4961#	JANHC@1N4987#	JANKC@1N4987#
JANHC@1N4962#	JANKC@1N4962#	JANHC@1N4988#	JANKC@1N4988#
JANHC@1N4963#	JANKC@1N4963#	JANHC@1N4989#	JANKC@1N4989#
JANHC@1N4964#	JANKC@1N4964#	JANHC@1N4990#	JANKC@1N4990#
JANHC@1N4965#	JANKC@1N4965#	JANHC@1N4991#	JANKC@1N4991#
JANHC@1N4966#	JANKC@1N4966#	JANHC@1N4992#	JANKC@1N4992#
JANHC@1N4967#	JANKC@1N4967#	JANHC@1N4993#	JANKC@1N4993#
JANHC@1N4968#	JANKC@1N4968#	JANHC@1N4994#	JANKC@1N4994#
JANHC@1N4969#	JANKC@1N4969#	JANHC@1N4995#	JANKC@1N4995#
JANHC@1N4970#	JANKC@1N4970#	JANHC@1N4996#	JANKC@1N4996#
JANHC@1N4971#	JANKC@1N4971#	JANHC@1N5968#	JANKC@1N5968#
JANHC@1N4972#	JANKC@1N4972#	JANHC@1N5969#	JANKC@1N5969#
JANHC@1N4973#	JANKC@1N4973#	JANHC@1N6632#	JANKC@1N6632#
JANHC@1N4974#	JANKC@1N4974#	JANHC@1N6633#	JANKC@1N6633#
JANHC@1N4975#	JANKC@1N4975#	JANHC@1N6634#	JANKC@1N6634#
JANHC@1N4976#	JANKC@1N4976#	JANHC@1N6635#	JANKC@1N6635#
JANHC@1N4977#	JANKC@1N4977#	JANHC@1N6636#	JANKC@1N6636#
JANHC@1N4978#	JANKC@1N4978#	JANHC@1N6637#	JANKC@1N6637#
JANHC@1N4979#	JANKC@1N4979#		

(1) The at-sign (@) represents the die version "A", "C" or "D" (see 1.5.5) and the pound sign (#) represents the voltage tolerance suffix "C", "D" or left blank (see 1.5.3.1).

6.6 Substitutability of 2 percent and 1 percent tolerance devices. Devices of tighter tolerance are a direct one way substitute for the looser tolerance devices (example: JANTX1N4954D substitutes for a JANTX1N4954 or JANTX1N4954DUS substitutes for a JANTX1N4954US).

6.7 Applications data.

6.7.1 PCB mounting with FR4 material for the full 5 Watts. For a PCB mounting example with FR4 material where the full 5 Watt rating is used at a T_J of 175°C and ambient temperature of 55°C, the following steps guide the user in what the PCB pad size will need to be with 1 ounce, 2 ounce, and 3 ounce copper. For axial-leaded, the lead length for mounting will be .187 inch (4.76 mm) or less from body to entry point on PCB surface.

a. Calculate maximum thermal resistance allowed from junction to ambient (175°C to 55°C) for the required 5 Watts: $R_{\theta JA}$ = (175°C - 55°C)/5.00 W = 24°C/W.

b. Look up thermal resistance of 24°C/W on Y-axis on figure 9 using a thermal resistance versus pad area plot on one of the three curves for different weights of copper cladding and then intersect curve horizontally to get the answer. These curves assume still air, horizontal position.

c. The answer is: 1 ounce PCB = Not applicable, 2 ounce PCB = 4.0 inch^2 (25.8 cm^2), 3 ounce PCB = 2.5 in^2 (16.1 cm^2) for each pad.

d. Add a conservative guard-band to the pad size (larger) to keep T_J below 175°C.

6.7.2 PCB mounting with FR4 material for only 1.5 Watts. For a PCB mounting example with FR4 material where only 1.5 Watts of power is used at a T_J of 175°C and ambient temperature of 55°C, the following steps guide the user in what the PCB pad size will need to be in area for each pad with 1 ounce, 2 ounce, and 3 ounce copper. For axial-leaded, the lead length for mounting will be .187 inch (4.76 mm) or less from body to entry point on PCB surface.

a. Calculate maximum thermal resistance allowed from junction to ambient (175°C to 55°C) for the required 1.5 Watts: $R_{\theta JA}$ = (175°C - 55°C)/1.5 W = 80°C/W.

b. Find thermal resistance of 80°C/W on Y-axis in figure 9 using a thermal resistance versus pad area plot on one of the three curves for different weights of copper cladding and then intersect curve horizontally to get answer. These curves assume still air, horizontal position.

c. The answer is: 1 ounce PCB = .13 inch^2 (83.9 mm^2), 2 ounce PCB = .082 inch^2 (52.9 mm^2), 3 ounce PCB = .055 inch^2 (35.4 mm^2) for each pad.

d. Add a conservative guard-band to the pad size (larger) to keep T_J below 175°C.

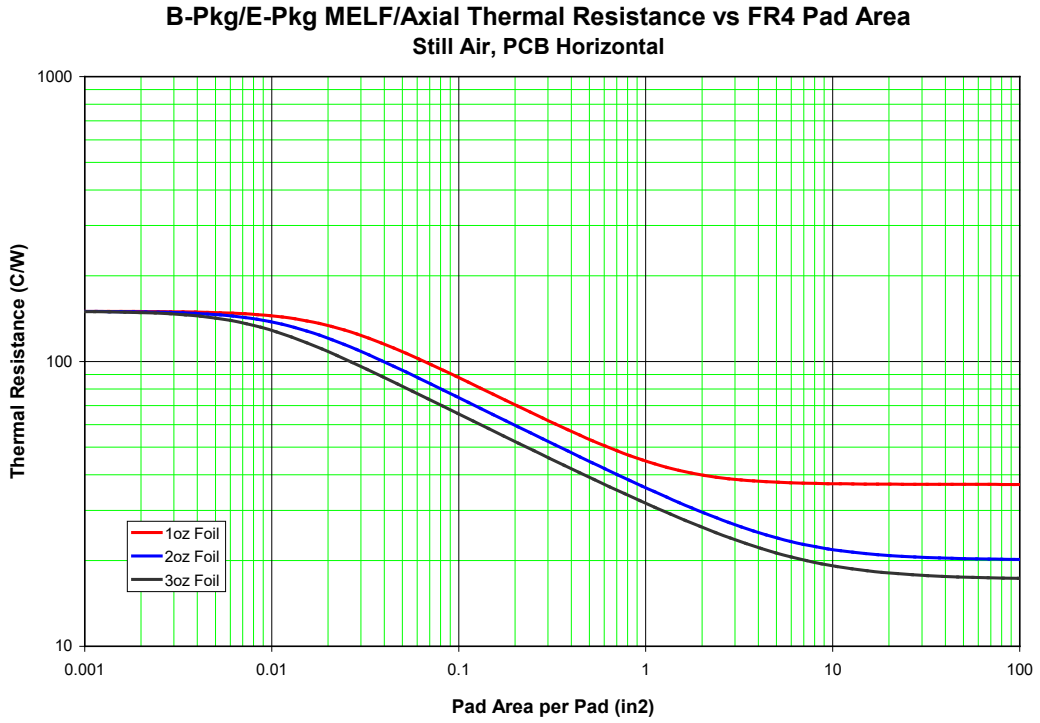


FIGURE 9. Thermal resistance versus FR4 pad area still air, PCB horizontal (for each pad) with 1 ounce copper (top curve), 2 ounce copper (middle curve), and 3 ounce copper (bottom curve).

6.8 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example: JANHCA1N4954) will be identified on the QML.

JANHC and JANKC ordering information		
PIN	Manufacturer	
	43611	13409
* 1N4954 through 1N4996, 1N5968, 1N5969		JANKCD1N4954 through JANKCD1N4996, JANKCD1N5968, JANKCD1N5969
1N6632 through 1N6637	JANKCA1N6632 through JANKCA1N6637	JANKCD1N6632 through JANKCD1N6637

6.9 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.10 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

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