DATA SHEET
www.onsemi.com

MOSFET – P-Channel

100 V

FQD8P10TM-F085

Description

These P–Channel enhancement mode power field effect transistors are produced using **onsemi**'s proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on–state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

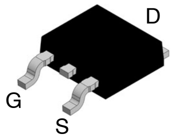
Features

- –6.6 A, –100 V, $R_{DS(on)} = 0.53\ \Omega$ @ $V_{GS} = -10$ V
- Low Gate Charge (Typ. 12 nC)
- Low Crss (Typ. 30 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- Qualified to AEC–Q101
- RoHS Compliant

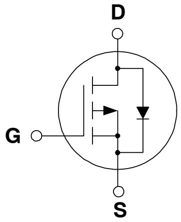
ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain–Source Voltage	–100	V
I_D	Drain Current – Continuous (T_C = 25°C) – Continuous (T_C = 100°C)	–6.6 –4.2	A
I_{DM}	Drain Current – Pulsed (Note 1)	–26.4	A
V_{GSS}	Gate–Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	150	mJ
I_{AR}	Avalanche Current (Note 1)	–6.6	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	–6.0	V/ns
P_D	Power Dissipation (T_A = 25°C)*	2.5	W
	Power Dissipation (T_C = 25°C) – Derate above 25°C	44 0.35	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	–55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

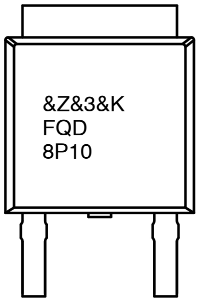
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



DPAK3
CASE 369AS



MARKING DIAGRAM



&Z	=	Assembly Code
&3	=	Date Code (Year and Week)
&K	=	Lot Code
FQD8P10	=	Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FQD8P10TM–F085	DPAK3 (Pb–Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

January, 2024 – Rev. 4

THERMAL CHARACTERISTICS

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	−	2.84	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient*	−	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	−	110	°C/W

NOTE:
*When mounted on the minimum pad size recommended (PCB Mount)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA	−100	−	−	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	−	−0.1	−	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −100 V, V_{GS} = 0 V	−	−	−1	μA
		V_{DS} = −80 V, T_C = 125°C	−	−	−10	μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = −30 V, V_{DS} = 0 V	−	−	−100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = 30 V, V_{DS} = 0 V	−	−	100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−2.0	−	−4.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = −10 V, I_D = −3.3 A	−	0.41	0.53	Ω
g_{FS}	Forward Transconductance	V_{DS} = −40 V, I_D = −3.3 A (Note 4)	−	4.1	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −25 V, V_{GS} = 0 V, f = 1.0 MHz	−	360	470	pF
C_{oss}	Output Capacitance		−	120	155	pF
C_{rss}	Reverse Transfer Capacitance		−	30	40	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −50 V, I_D = −8.0 A, R_G = 25 Ω (Note 4, 5)	−	11	30	ns
t_r	Turn−On Rise Time		−	110	230	ns
$t_{d(off)}$	Turn−Off Delay Time		−	20	50	ns
t_f	Turn−Off Fall Time		−	35	80	ns
Q_g	Total Gate Charge	V_{DS} = −80 V, I_D = −8.0 A, V_{GS} = −10 V (Note 4, 5)	−	12	15	nC
Q_{gs}	Gate−Source Charge		−	3.0	−	nC
Q_{gd}	Gate−Drain Charge		−	6.4	−	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		−	−	−6.6	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		−	−	−26.4	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −6.6 A	−	−	−4.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = −8.0 A, dI_F / dt = 100 A/ μs (Note 4)	−	98	−	ns
Q_{rr}	Reverse Recovery Charge		−	0.35	−	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. Repetitive Rating: Pulse−width limited by maximum junction temperature.
2. L = 5.2 mH, I_{AS} = −6.6 A, V_{DD} = −25 V, R_G = 25 Ω, Starting T_J = 25°C.
3. $I_{SD} \le -8.0$ A, di/dt ≤ 300 A/μs, $V_{DD} \le BV_{DSS}$, Starting T_J = 25°C.
4. Pulse Test : Pulse width ≤ 300 μs, Duty cycle ≤ 2%.
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

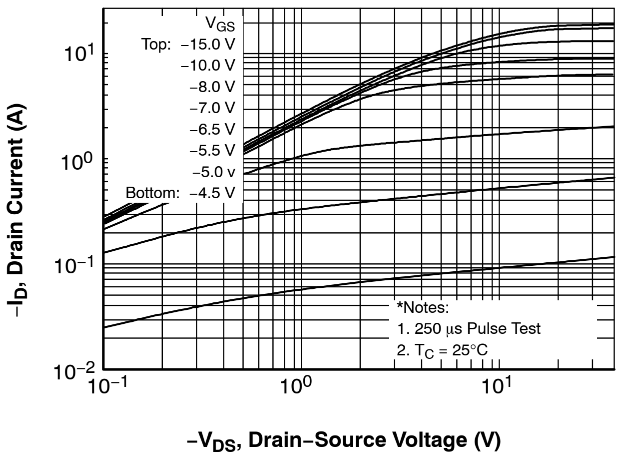


Figure 1. On−Region Characteristics

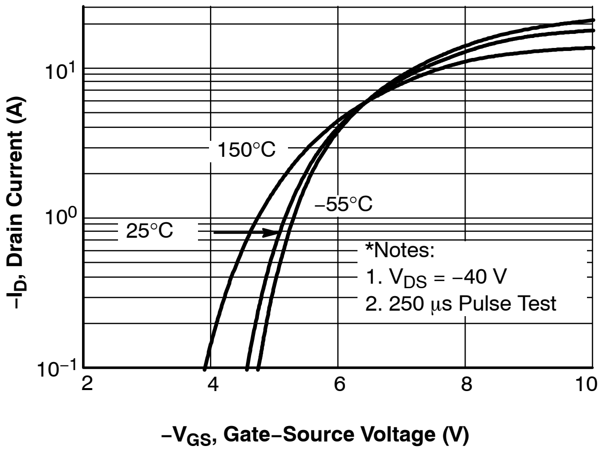


Figure 2. Transfer Characteristics

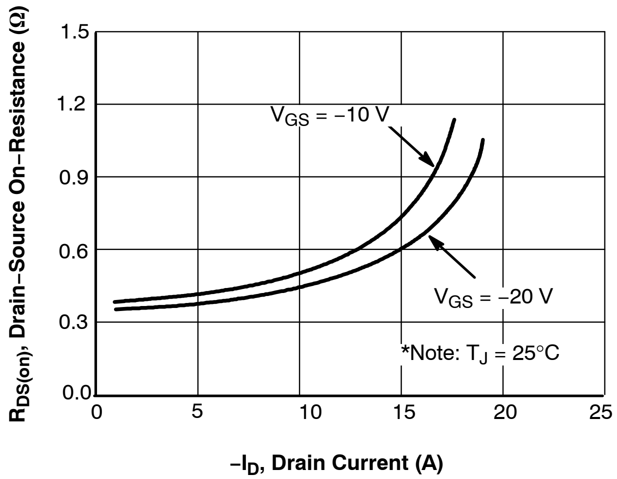


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

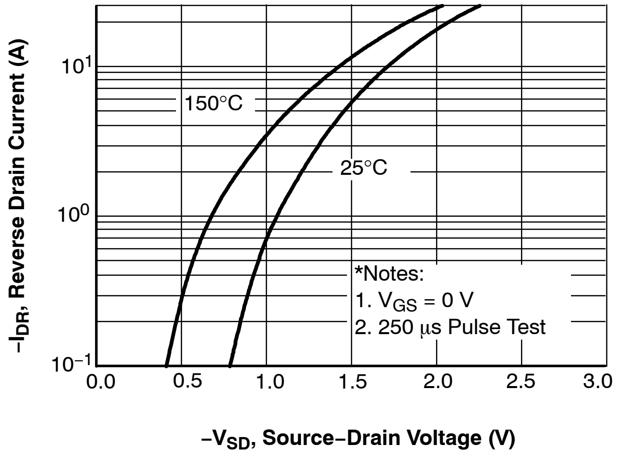


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

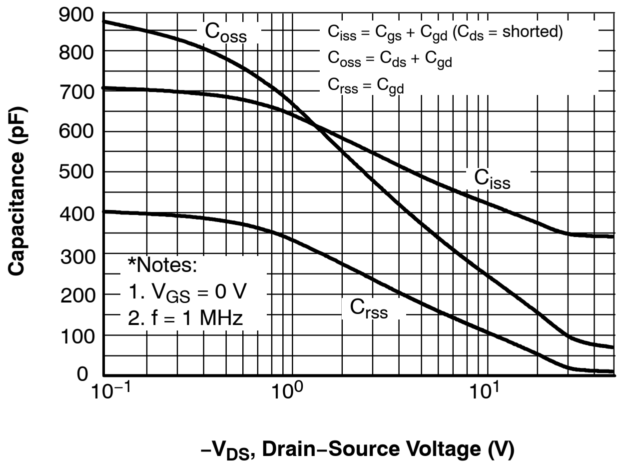


Figure 5. Capacitance Characteristics

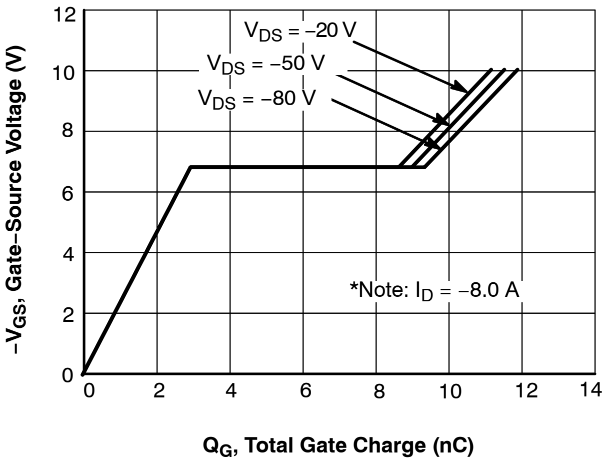


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continue)

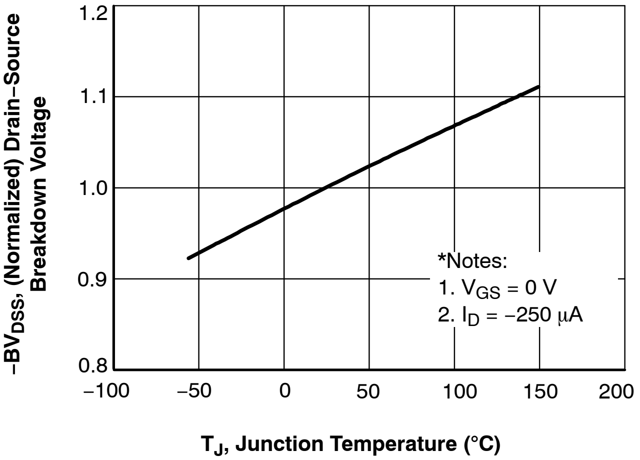


Figure 7. Breakdown Voltage Variation vs. Temperature

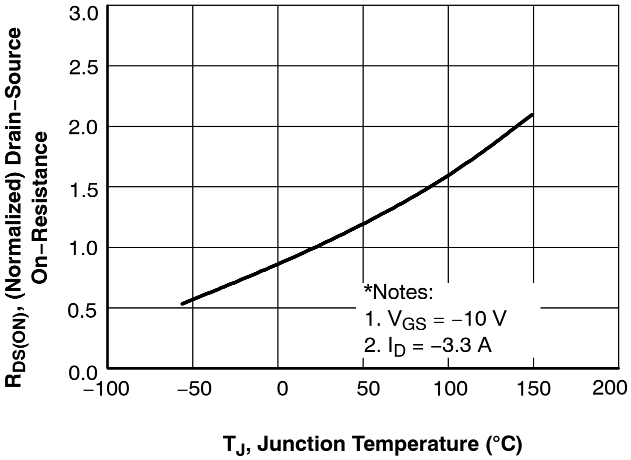


Figure 8. On−Resistance Variation vs. Temperature

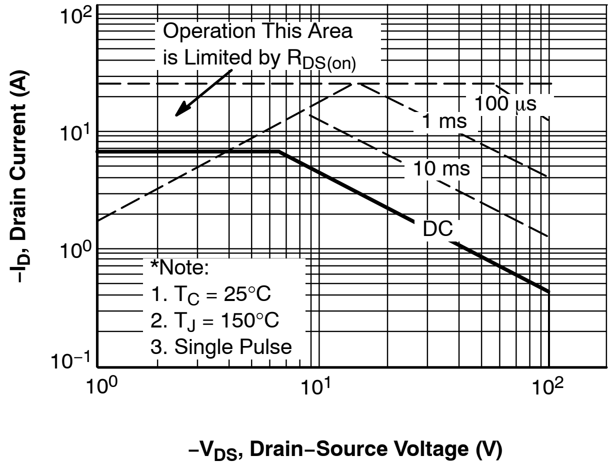


Figure 9. Maximum Safe Operating Area

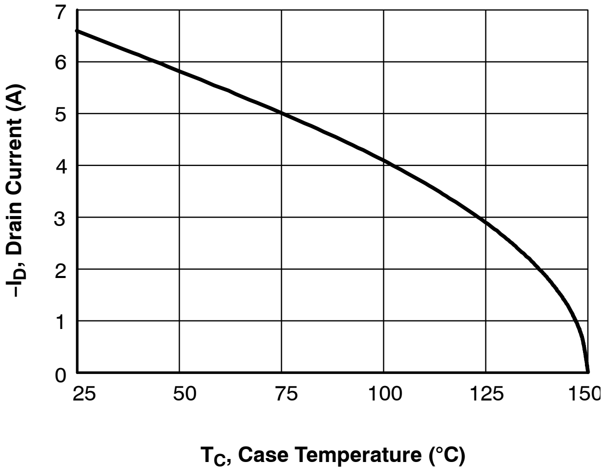


Figure 10. Maximum Drain Current vs. Case Temperature

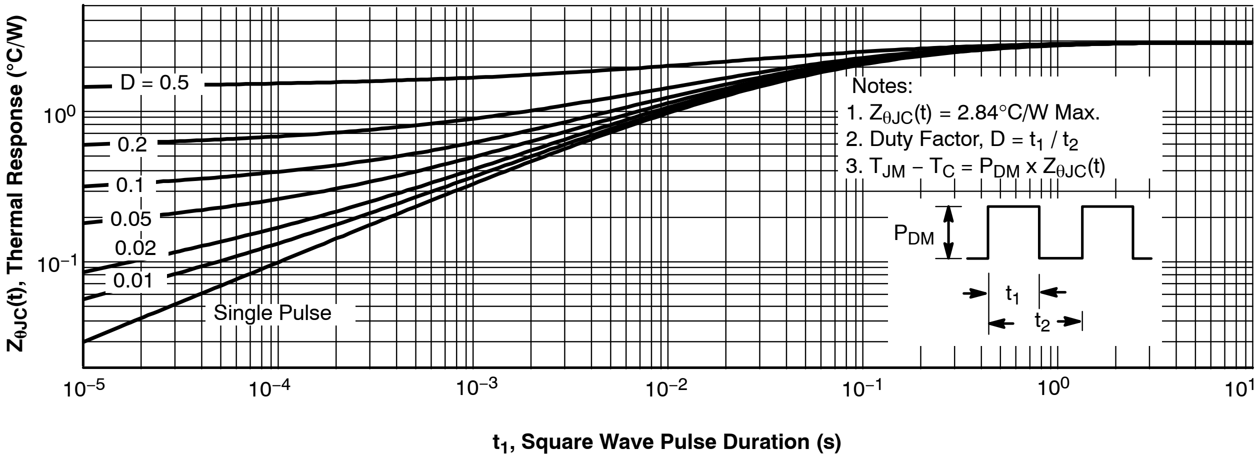


Figure 11. Transient Thermal Response Curve

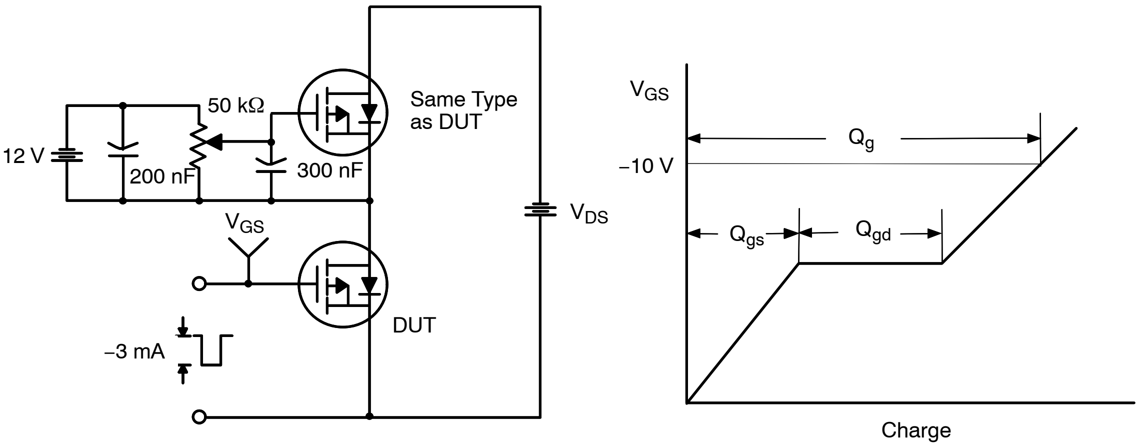


Figure 12. Gate Charge Test Circuit & Waveform

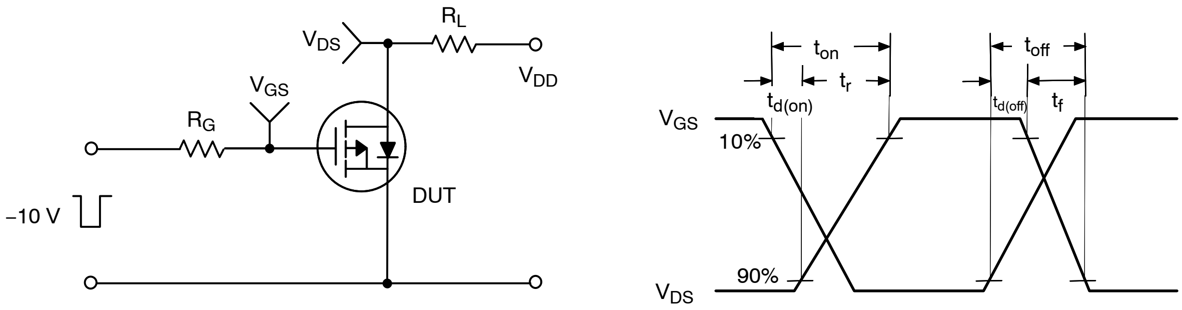
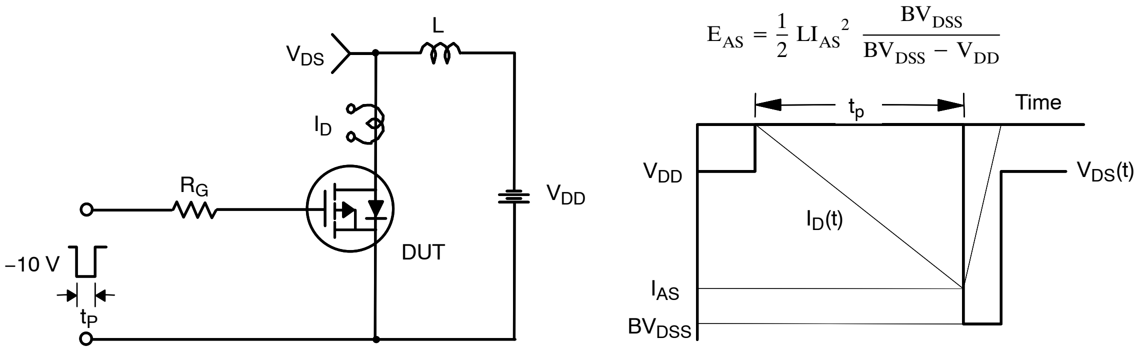


Figure 13. Resistive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} LI_{AS}^{2} \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

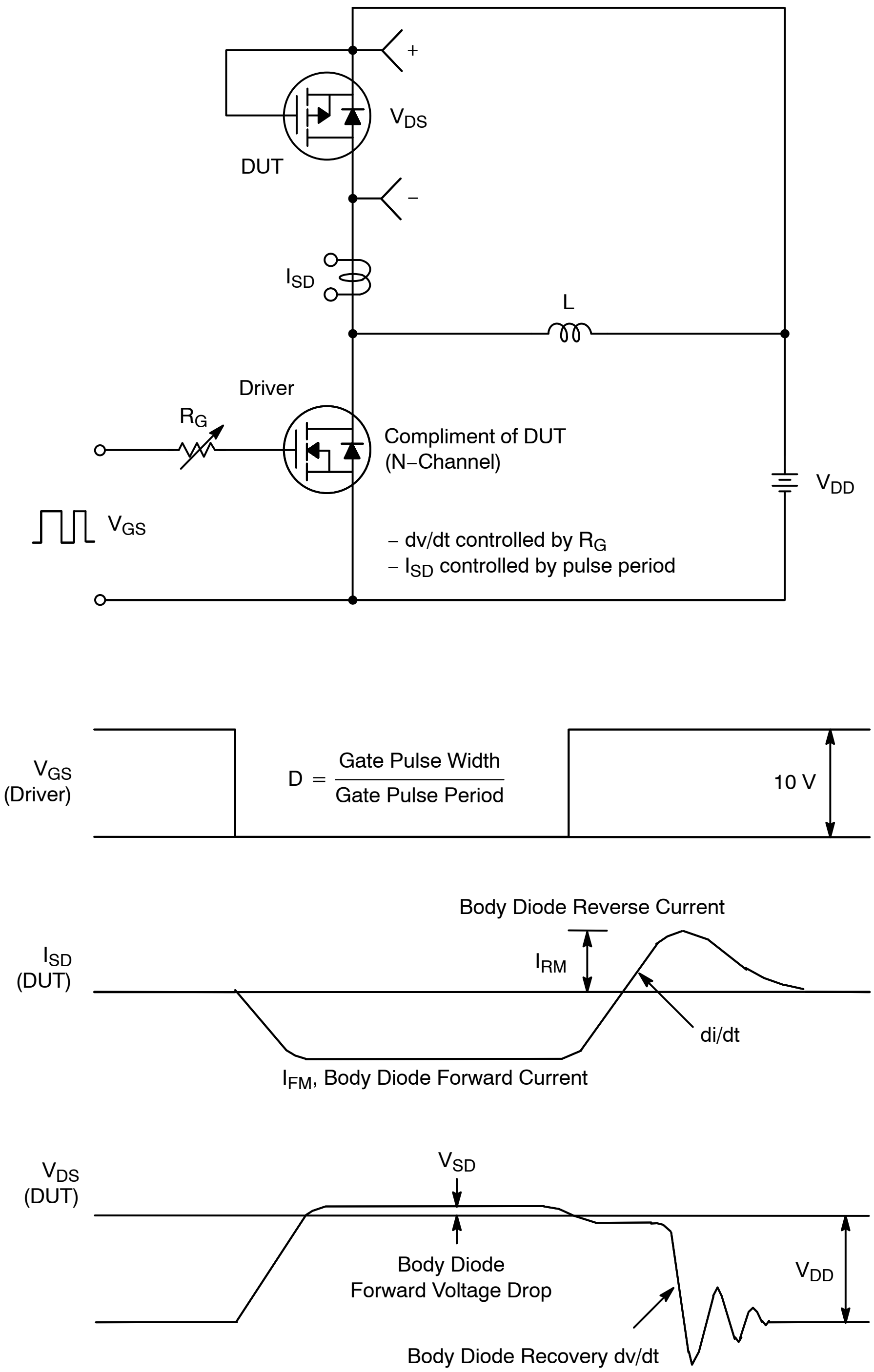
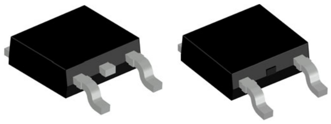
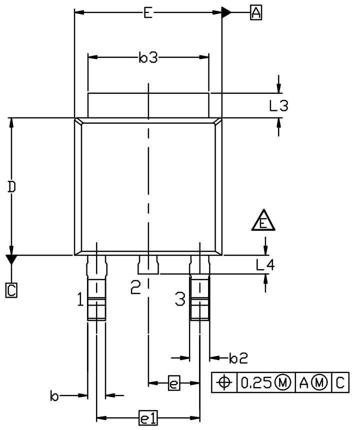


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

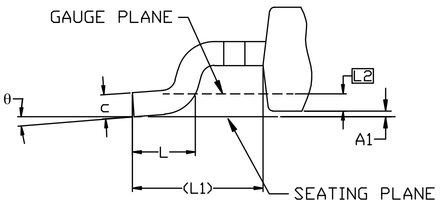
DATE 20 DEC 2023



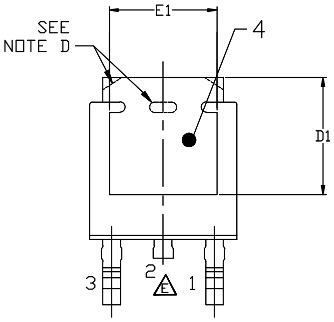
NON-DIODE PRODUCTS VERSION

NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- △E FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
- F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

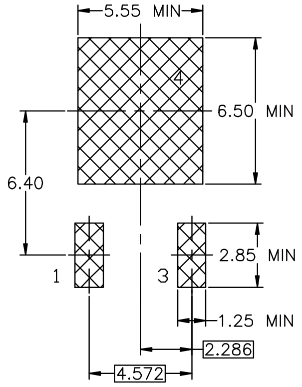
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°



DETAIL A
(ROTATED -90°)
SCALE: 12X

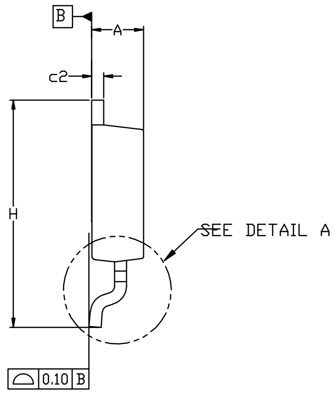


NON-DIODE PRODUCTS VERSION

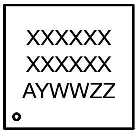


LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DPAK3 6.10x6.54x2.29, 4.57P**	**PAGE 1 OF 1**

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