



# SN74LVC2G74 Single Positive-Edge-Triggered D-Type Flip-Flop With Clear and Preset

## 1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.9 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

## 2 Applications

- Servers
- LED displays
- Network switch
- Telecom infrastructure
- Motor drivers
- I/O Expanders

## 3 Description

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) input sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

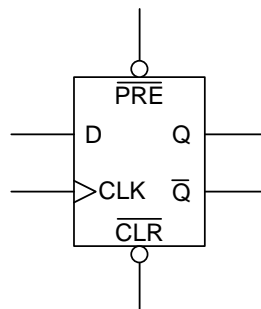
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE
SN74LVC2G74	SM8 (8)	2.95 mm × 2.80 mm
	VSSOP (8)	2.30 mm × 2.00 mm
	DSBGA (8)	1.91 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



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## 4 Revision History

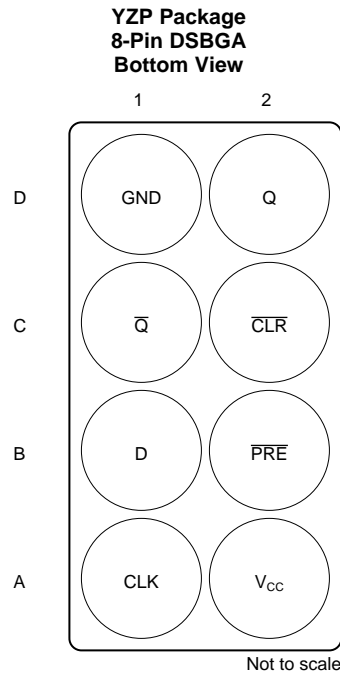
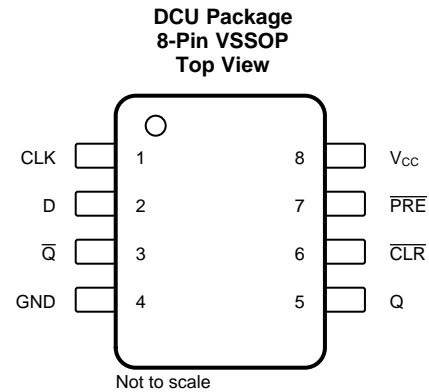
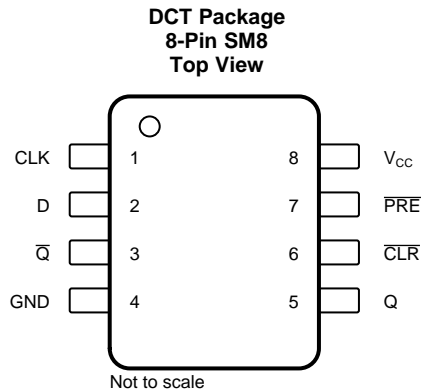
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (January 2015) to Revision P	Page
• Changed SSOP to SM8 in <i>Device Information</i> table .....	1
• Updated pinout images to new format .....	3
• Added pin number for DSBGA package in <i>Pin Functions</i> table .....	3
• Changed 6 PINS to 8 PINS in <i>Thermal Information</i> table .....	5
• Changed 23 to 2.3 for $t_{su}$ data in <i>Timing Requirements, –40°C to +125°C</i> .....	6
• Added <i>Receiving Notification of Documentation Updates</i> section and <i>Community Resources</i> section .....	13

Changes from Revision N (July 2013) to Revision O	Page
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....	1

Changes from Revision M (February 2007) to Revision N	Page
• Changed $I_{off}$ description in <i>Features</i> .....	1
• Added parameter values for –40 to +125°C temperature ratings in <i>Electrical Characteristics</i> table. ....	6
• Changed <i>Timing Requirements, –40°C to +85°C</i> table .....	6
• Added <i>Timing Requirements, –40°C to +125°C</i> table .....	6
• Changed <i>Switching Characteristics, –40°C to +85°C</i> table .....	7
• Added <i>Switching Characteristics, –40°C to +125°C</i> table .....	7

## 5 Pin Configuration and Functions



See mechanical drawings for dimensions.

### Pin Functions

PIN			TYPE	DESCRIPTION
NAME	VSSOP, SM8	DSBGA		
CLK	1	A1	I	Clock input
$\overline{\text{CLR}}$	6	C2	I	Clear input - Pull low to set Q output low
D	2	B1	I	Input
GND	4	D1	—	Ground
Q	5	D2	O	Output
$\overline{\text{Q}}$	3	C1	O	Inverted output
$\overline{\text{PRE}}$	7	B2	I	Preset input - Pull low to set Q output high
$V_{\text{CC}}$	8	A2	—	Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	−0.5	6.5	V
$V_I$	Input voltage <sup>(2)</sup>	−0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	−0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	−0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	−50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	−50	mA
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$T_{stg}$	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the *Recommended Operating Conditions* table.

### 6.2 ESD Ratings

PARAMETER	DEFINITION	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
		V <sub>CC</sub> = 3 V to 3.6 V		0.8	
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 × V <sub>CC</sub>	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		–4	mA
		V <sub>CC</sub> = 2.3 V		–8	
		V <sub>CC</sub> = 3 V		–16	
				–24	
		V <sub>CC</sub> = 4.5 V		–32	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4	mA
		V <sub>CC</sub> = 2.3 V		8	
		V <sub>CC</sub> = 3 V		16	
				24	
		V <sub>CC</sub> = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V <sub>CC</sub> = 3.3 V ± 0.3 V		10	
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
T <sub>A</sub>	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LVC2G74			UNIT
		DCT	DCU	YZP	
		8 PINS			
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	220	227	102	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

## SN74LVC2G74

SCES203P – APRIL 1999 – REVISED JULY 2016

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### 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	–40°C to +85°C			–40°C to +125°C			UNIT
						Recommended			
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 5.5 V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = –4 mA	1.65 V	1.2			1.2			
	I <sub>OH</sub> = –8 mA	2.3 V	1.9			1.85			
	I <sub>OH</sub> = –16 mA	3 V	2.4			2.4			
	I <sub>OH</sub> = –24 mA		2.3			2.3			
	I <sub>OH</sub> = –32 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V	0.1			0.1			V
	I <sub>OL</sub> = 4 mA	1.65 V	0.45			0.45			
	I <sub>OL</sub> = 8 mA	2.3 V	0.3			0.3			
	I <sub>OL</sub> = 16 mA	3 V	0.4			0.4			
	I <sub>OL</sub> = 24 mA		0.55			0.55			
	I <sub>OL</sub> = 32 mA	4.5 V	0.55			0.55			
I <sub>I</sub> Data or control inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V	±5			±5			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	±10			±10			μA
I <sub>CC</sub>	V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V	10			10			μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V	500			500			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	5			5			pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

### 6.6 Timing Requirements, –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	TO	–40°C to +85°C								UNIT
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>			80		175		175		200		MHz
t <sub>w</sub>	CLK		6.2		2.7		2.7		2		ns
	PRE or CLR low		6.2		2.7		2.7		2		
t <sub>su</sub>	Data		2.9		1.7		1.3		1.1		ns
	PRE or CLR inactive		1.9		1.4		1.2		1		
t <sub>h</sub>			0		0.3		1.2		0.5		ns

### 6.7 Timing Requirements, –40°C to +125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM	TO	–40°C to +125°C								UNIT
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>			80		120		120		140		MHz
t <sub>w</sub>	CLK		6.2		3.5		3.5		3.3		ns
	PRE or CLR low		6.2		3.5		3.5		3.3		
t <sub>su</sub>	Data		2.9		2.3		1.9		1.7		ns
	PRE or CLR inactive		1.9		2		1.8		1.6		
t <sub>h</sub>			0		0.3		0.5		0.5		ns

## 6.8 Switching Characteristics, –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM	TO	–40°C to +85°C								UNIT
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			80		175		175		200		MHz
t <sub>pd</sub>	CLK	Q	4.8	13.4	2.2	7.1	2.2	5.9	1.4	4.1	ns
		$\overline{Q}$	6	14.4	3	7.7	2.6	6.2	1.6	4.4	
	$\overline{PRE}$ or $\overline{CLR}$ low	Q or Q	4.4	12.9	2.3	7	1.7	5.9	1.6	4.1	

## 6.9 Switching Characteristics, –40°C to +125°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM	TO	–40°C to +125°C								UNIT
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			80		120		120		140		MHz
t <sub>pd</sub>	CLK	Q	4.8	14.4	2.2	8.1	2.2	6.9	1.4	5.1	ns
		$\overline{Q}$	6	16	3	9.7	2.6	7.2	1.6	5.4	
	$\overline{PRE}$ or $\overline{CLR}$ low	Q or $\overline{Q}$	4.4	14.9	2.3	9.5	1.7	7.9	1.6	6.1	

## 6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	$V_{CC} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance	$f = 10\text{ MHz}$	35	35	37	40	pF

## 6.11 Typical Characteristics

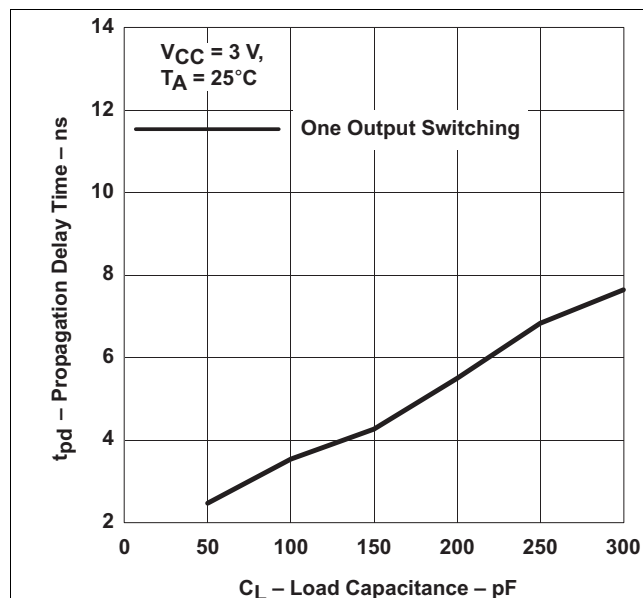


Figure 1. Propagation Delay (Low to High Transition) vs Load Capacitance

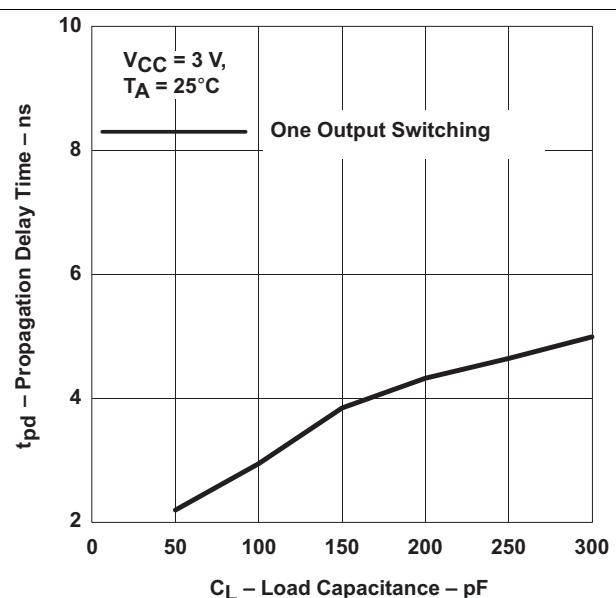


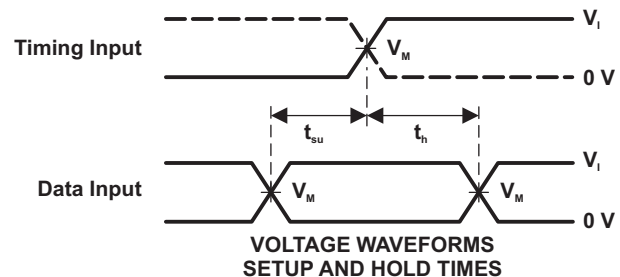
Figure 2. Propagation Delay (High to Low Transition) vs Load Capacitance

## 7 Parameter Measurement Information



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_i/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

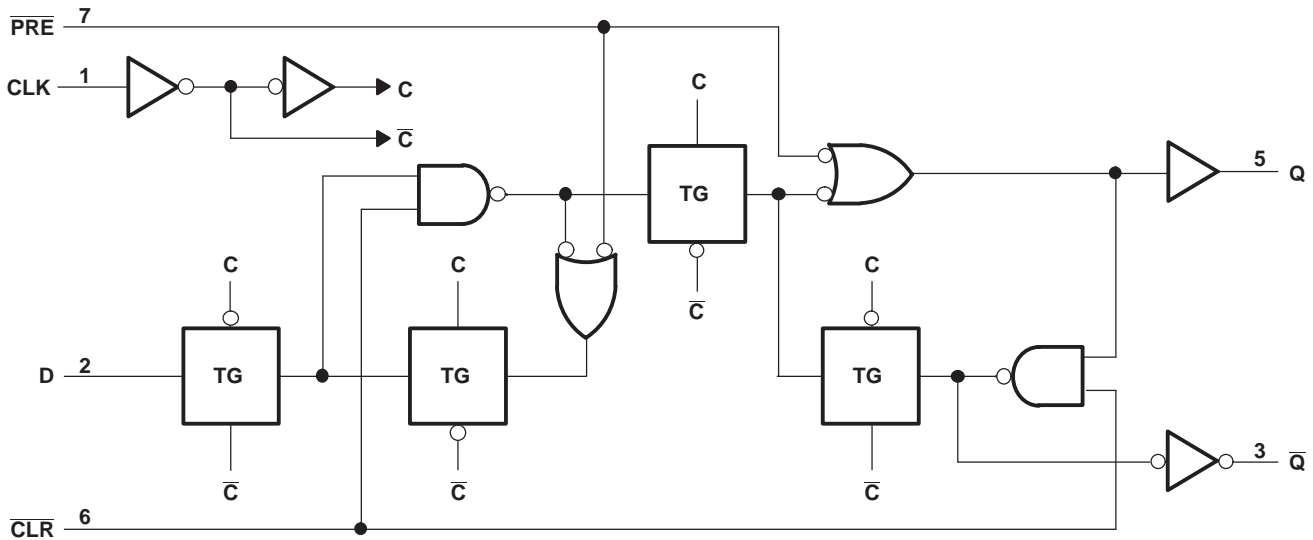


## 8 Detailed Description

## 8.1 Overview

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 8.2 Functional Block Diagram



### 8.3 Feature Description

- Allows down voltage translation
  - 5 V to 3.3 V
  - 5 V or 3.3 V to 1.8V
- Inputs accept voltage levels up to 5.5 V
- I<sub>off</sub> Feature
  - Can prevent backflow current that can damage device when powered down.

## 8.4 Device Functional Modes

Table 1 shows the functional modes of SN74LVC2G74.

### Table 1. Function Table

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>(1)</sup>	H <sup>(1)</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\overline{Q_0}$

(1) This configuration is non-stable; that is, it does not persist when  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

## 9 Application and Implementation

### NOTE

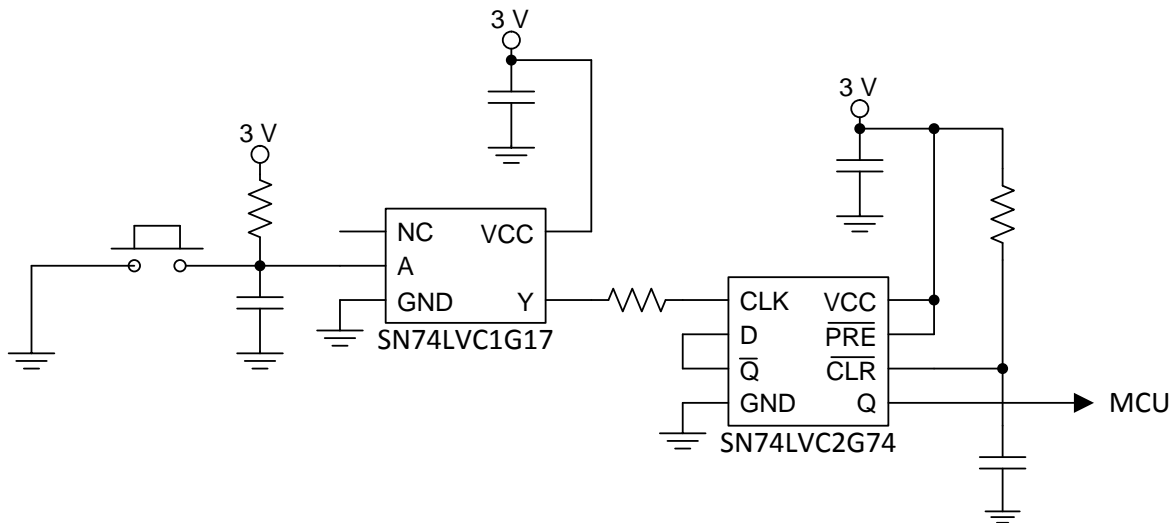
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) input sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The resistor and capacitor at the  $\overline{\text{CLR}}$  pin are optional. If they are not used, the  $\overline{\text{CLR}}$  pin should be connected directly to  $V_{CC}$  to be inactive.

### 9.2 Typical Power Button Circuit



**Figure 4. Device Power Button Circuit**

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

##### 1. Recommended Input Conditions:

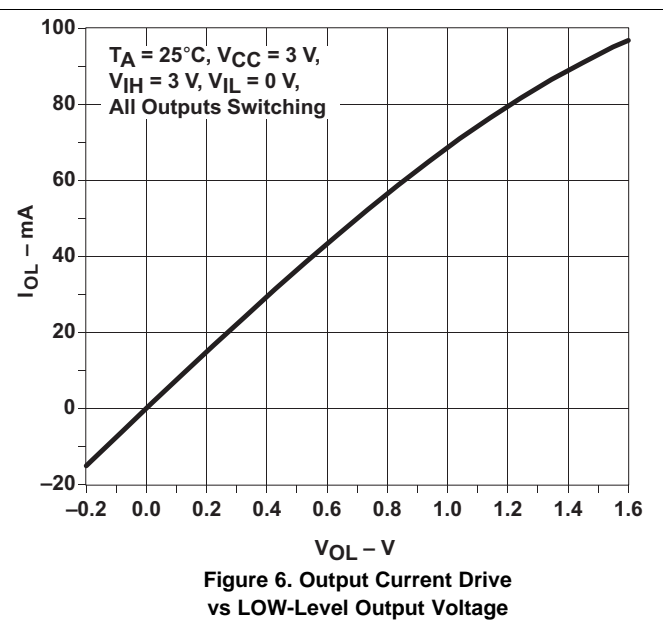
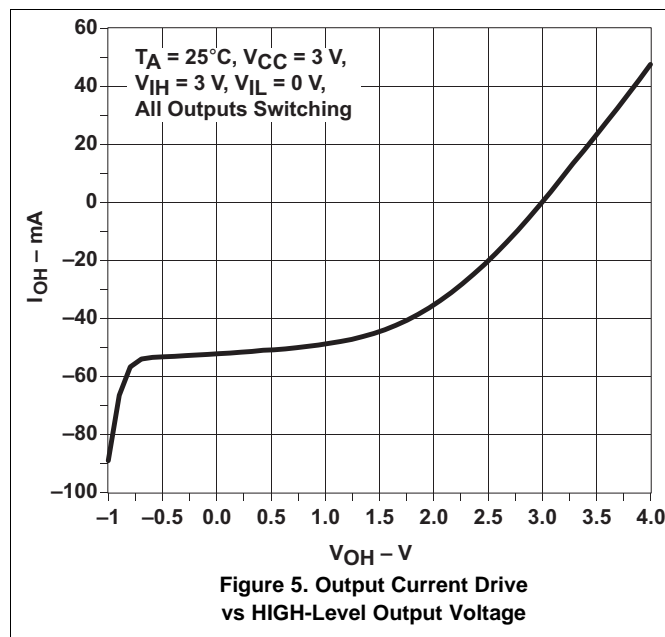
- For rise time and fall time specifications, see ( $\Delta t/\Delta V$ ) in [Recommended Operating Conditions](#) table.
- For specified high and low levels, see ( $V_{IH}$  and  $V_{IL}$ ) in [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$

##### 2. Recommend Output Conditions:

- Load currents should not exceed 50 mA per output and 100 mA total for the part.
- Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

## Typical Power Button Circuit (continued)

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F capacitor is recommended and if there are multiple  $V_{CC}$  terminals then .01- $\mu$ F or .022- $\mu$ F capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

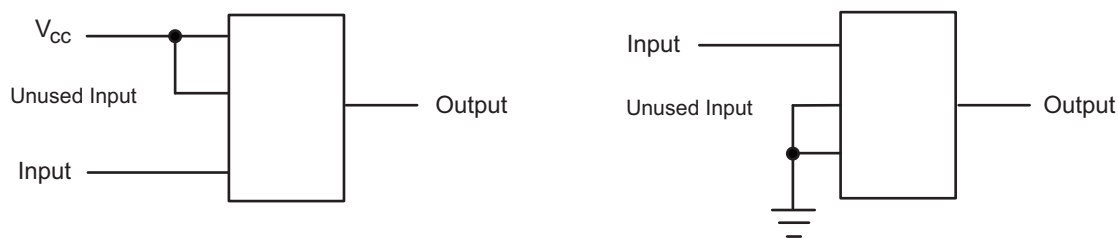
## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 11.2 Layout Example



**Figure 7. Layout Diagram**

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G74DCT3	ACTIVE	SM8	DCT	8	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 125	C74 Z	<a href="#">Samples</a>
SN74LVC2G74DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74 Z	<a href="#">Samples</a>
SN74LVC2G74DCTRE4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74 Z	<a href="#">Samples</a>
SN74LVC2G74DCTRE6	ACTIVE	SM8	DCT	8	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 125	C74 Z	<a href="#">Samples</a>
SN74LVC2G74DCTRG4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74 Z	<a href="#">Samples</a>
SN74LVC2G74DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(74, C74J, C74Q, C74R) CZ	<a href="#">Samples</a>
SN74LVC2G74DCURE4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R	<a href="#">Samples</a>
SN74LVC2G74DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R	<a href="#">Samples</a>
SN74LVC2G74DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C74J, C74Q, C74R)	<a href="#">Samples</a>
SN74LVC2G74DCUTE4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R	<a href="#">Samples</a>
SN74LVC2G74DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R	<a href="#">Samples</a>
SN74LVC2G74YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CPN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### **OTHER QUALIFIED VERSIONS OF SN74LVC2G74 :**

- Automotive: [SN74LVC2G74-Q1](#)
- Enhanced Product: [SN74LVC2G74-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G74DCT3	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G74DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G74DCTRE6	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G74YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1



## TAPE AND REEL BOX DIMENSIONS

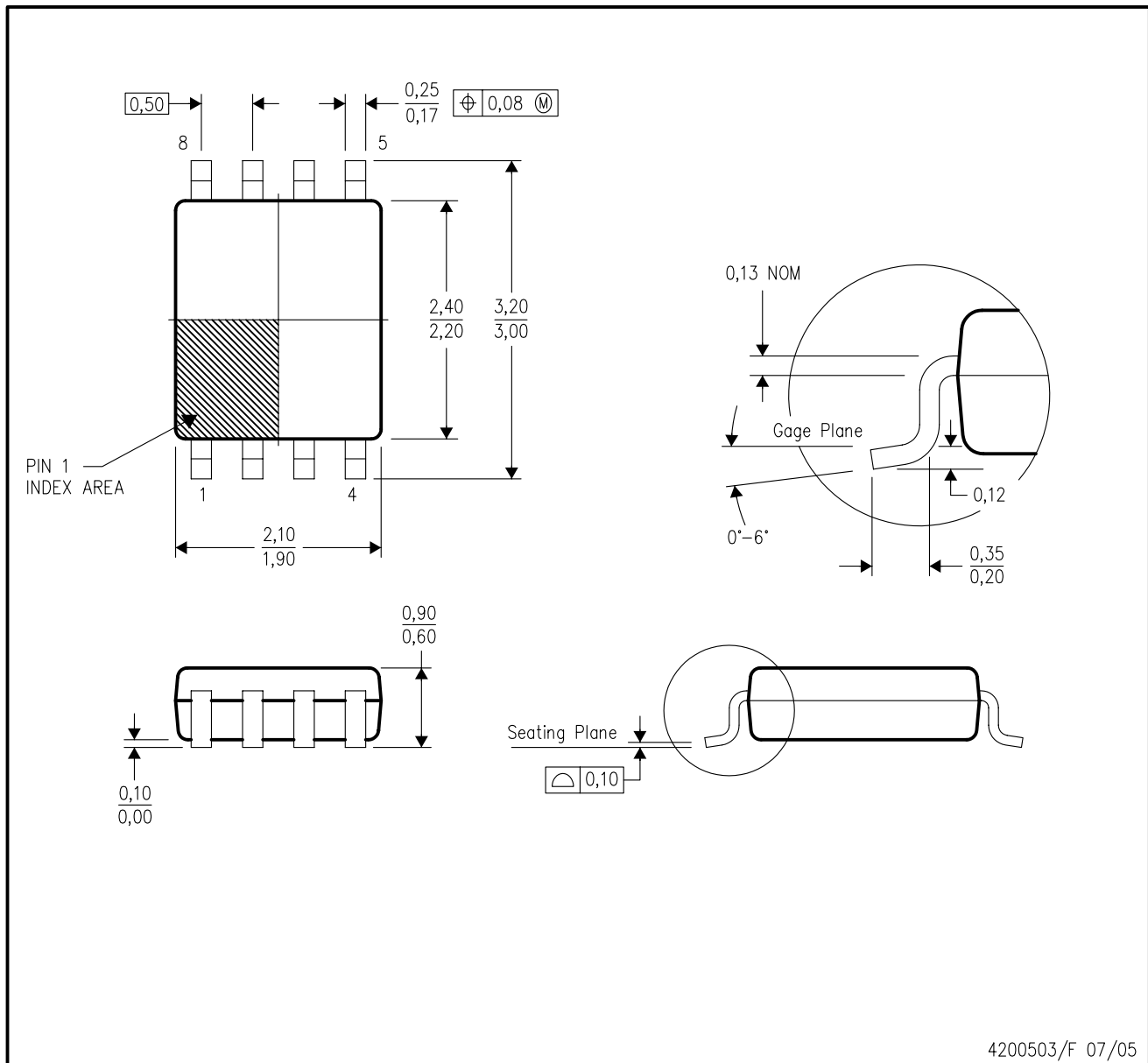


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G74DCT3	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G74DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G74DCTRE6	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G74DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G74DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G74DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC2G74DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G74YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



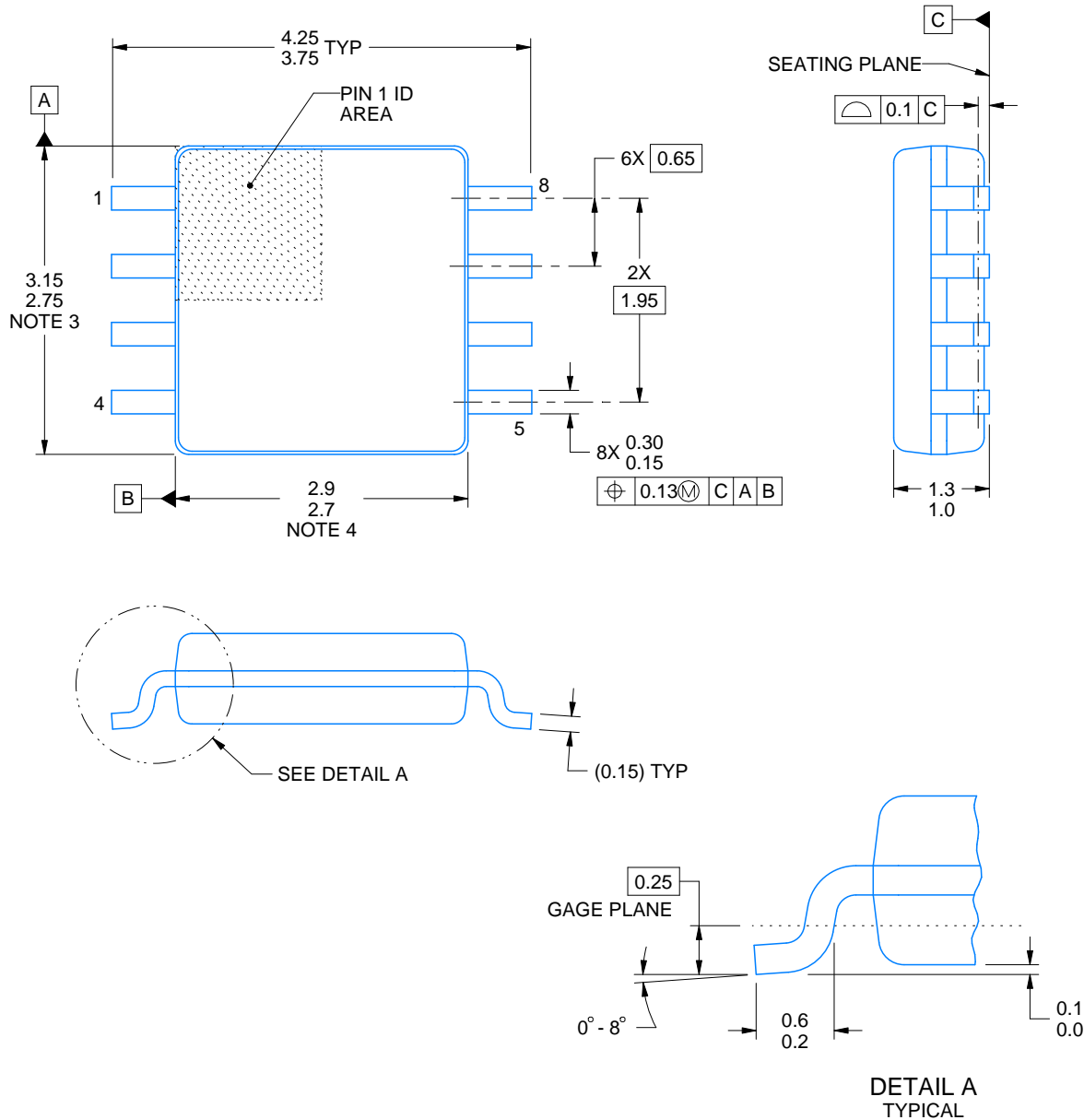
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**DCT0008A**

# PACKAGE OUTLINE

## SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



4220784/B 07/2020

**NOTES:**

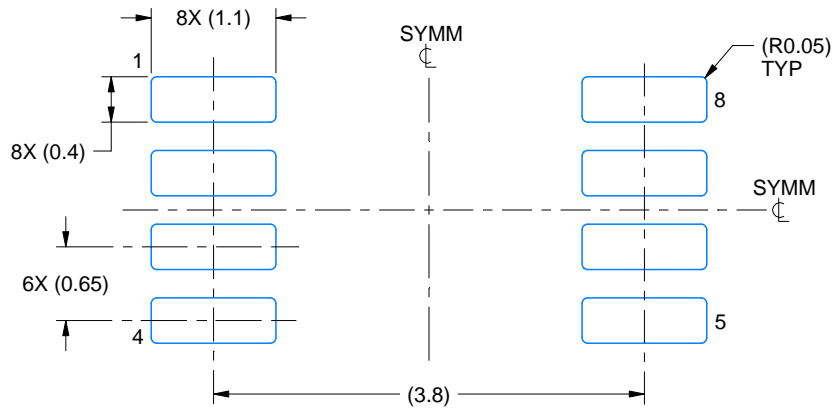
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-187.

# EXAMPLE BOARD LAYOUT

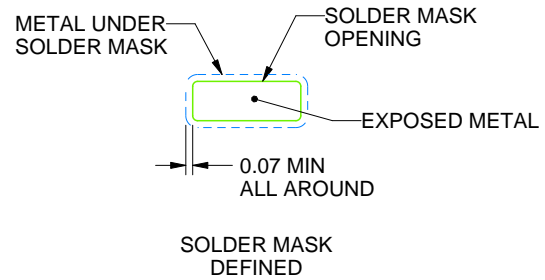
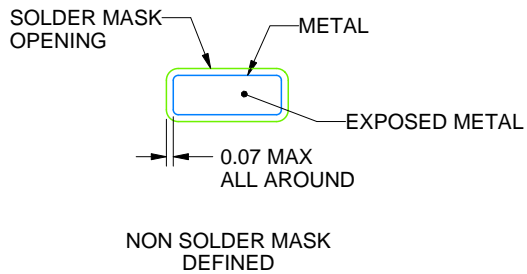
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4220784/B 07/2020

NOTES: (continued)

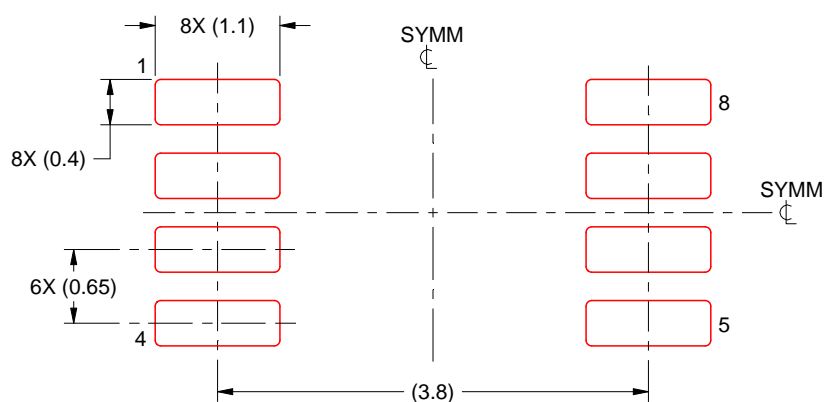
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



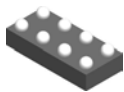
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4220784/B 07/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

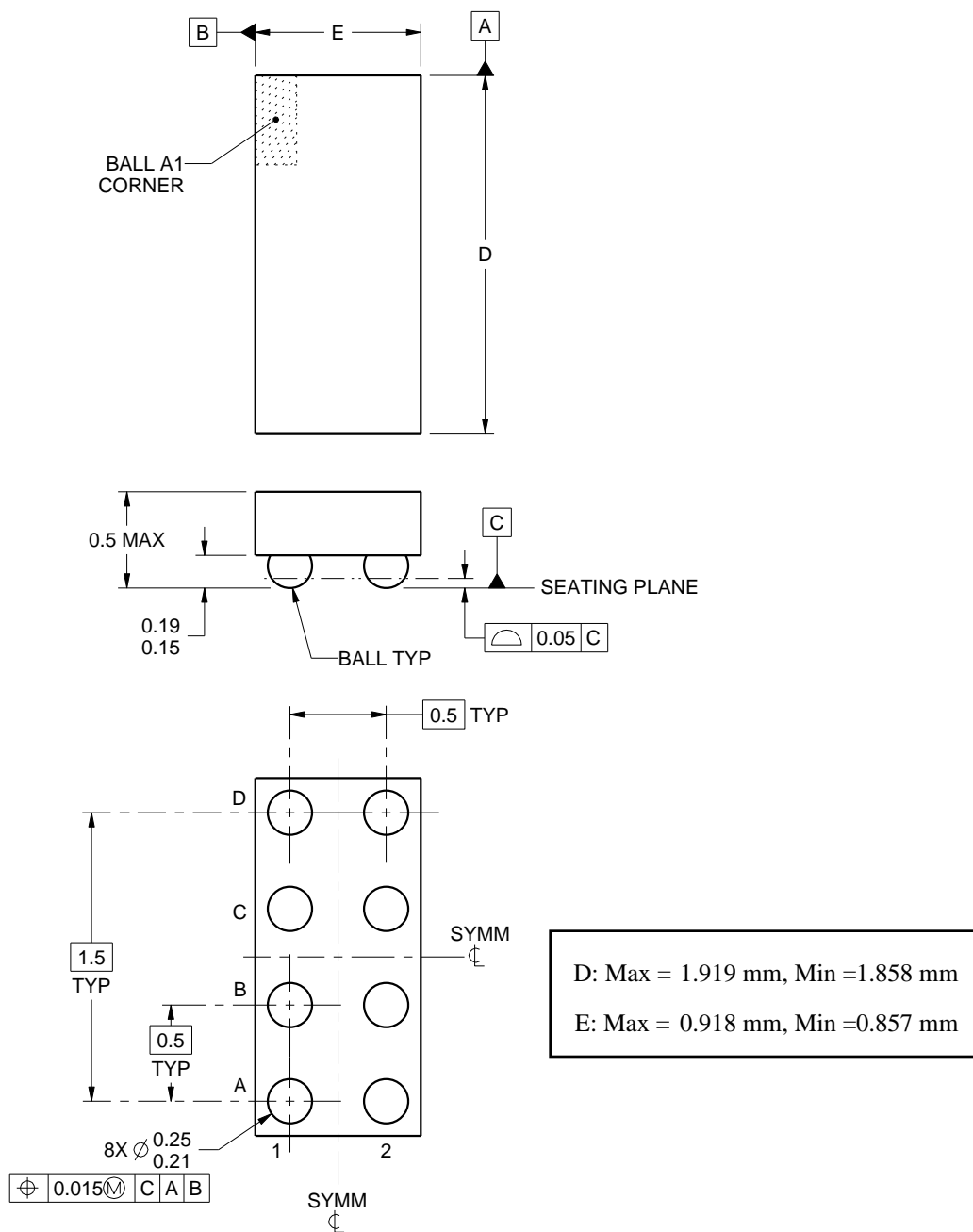
YZP0008



## PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

### NOTES:

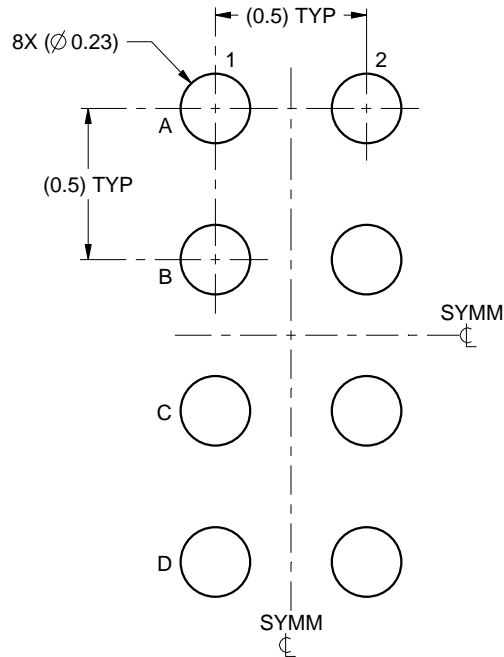
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

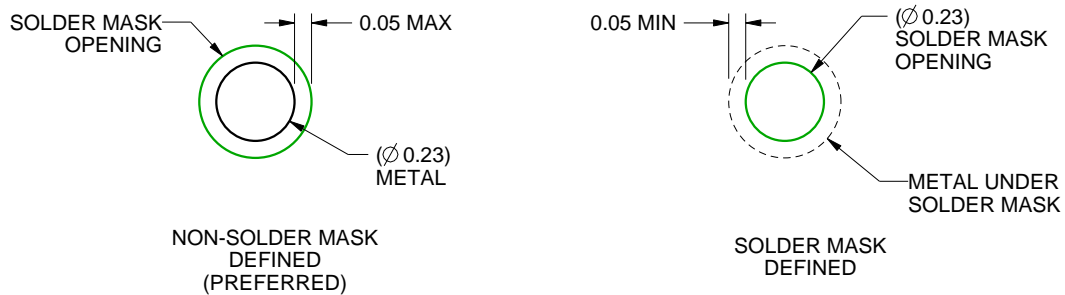
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).



## EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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