

Voltage Regulator - Low Dropout, On/Off Control

300 mA

MC33375, NCV33375 Series

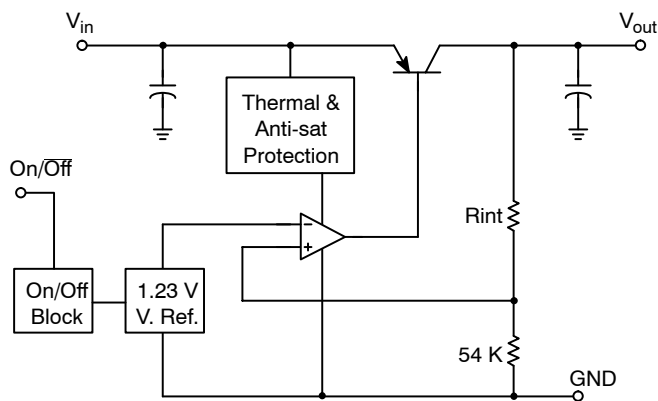
The MC33375 series are micropower low dropout voltage regulators available in a wide variety of output voltages as well as packages, SOT-223 and SOP-8. These devices feature a very low quiescent current and are capable of supplying output currents up to 300 mA. Internal current and thermal limiting protection are provided by the presence of a short circuit at the output and an internal thermal shutdown circuit.

The MC33375 has a control pin that allows a logic level signal to turn-off or turn-on the regulator output.

Due to the low input-to-output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

Features

- Low Quiescent Current (0.3 μ A in OFF mode; 125 μ A in ON mode)
- Low Input-to-Output Voltage Differential of 25 mV at $I_O = 10$ mA, and 260 mV at $I_O = 300$ mA
- Extremely Tight Line and Load Regulation
- Stable with Output Capacitance of only 0.33 μ F for 2.5 V Output Voltage
- Internal Current and Thermal Limiting
- Logic Level ON/OFF Control
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

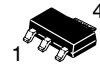


This device contains 41 active transistors

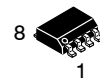
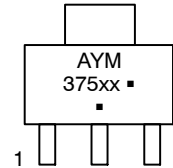
Figure 1. Simplified Block Diagram

LOW DROPOUT MICROPOWER VOLTAGE REGULATOR

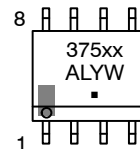
MARKING DIAGRAMS



SOT-223
ST SUFFIX
CASE 318E



SOIC-8
D SUFFIX
CASE 751



A = Assembly Location
Y = Year
M = Date Code
L = Wafer Lot
W = Work Week
xx = Voltage Version
▪ = Pb-Free Package

(Note: Microdot may be in either location)

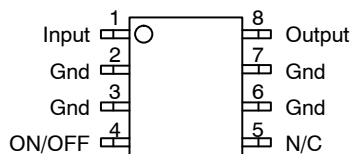
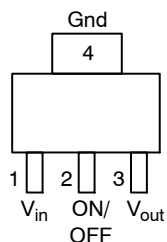
ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 11.

MC33375, NCV33375 Series

PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V _{CC}	13	Vdc
Power Dissipation and Thermal Characteristics T _A = 25 °C			
Maximum Power Dissipation	P _D	Internally Limited	W
Case 751 (SOP-8) D Suffix			
Thermal Resistance, Junction-to-Ambient	R _{θJA}	160	°C/W
Thermal Resistance, Junction-to-Case	R _{θJC}	25	°C/W
Case 318E (SOT-223) ST Suffix			
Thermal Resistance, Junction-to-Air	R _{θJA}	245	°C/W
Thermal Resistance, Junction-to-Case	R _{θJC}	15	°C/W
Output Current	I _O	300	mA
Maximum Junction Temperature	T _J	150	°C
Operating Ambient Temperature Range	T _A	– 40 to +125	°C
Storage Temperature Range	T _{stg}	– 65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MC33375, NCV33375 Series

ELECTRICAL CHARACTERISTICS ($C_L = 1.0 \mu F$, $T_A = 25^\circ C$, for min/max values $T_J = -40^\circ C$ to $+125^\circ C$, Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage $I_O = 0 \text{ mA to } 250 \text{ mA}$ $T_A = 25^\circ C$, $V_{in} = [V_O + 1] \text{ V}$ 1.8 V Suffix 2.5 V Suffix 3.0 V Suffix 3.3 V Suffix 5.0 V Suffix $V_{in} = [V_O + 1] \text{ V}$, $0 < I_O < 100 \text{ mA}$ 2% Tolerance from $T_J = -40$ to $+125^\circ C$ 1.8 V Suffix 2.5 V Suffix 3.0 V Suffix 3.3 V Suffix 5.0 V Suffix	V_O	1.782 2.475 2.970 3.267 4.950 1.764 2.450 2.940 3.234 4.900	1.80 2.50 3.00 3.30 5.00 – – – – –	1.818 2.525 3.030 3.333 5.05 1.836 2.550 3.060 3.366 5.100	Vdc
Line Regulation $V_{in} = [V_O + 1] \text{ V to } 12 \text{ V}$, $I_O = 250 \text{ mA}$, All Suffixes $T_A = 25^\circ C$	Reg_{line}	–	2.0	10	mV
Load Regulation $V_{in} = [V_O + 1] \text{ V}$, $I_O = 0 \text{ mA to } 250 \text{ mA}$, All Suffixes $T_A = 25^\circ C$	Reg_{load}	–	5.0	25	mV
Dropout Voltage (Note 3) $I_O = 10 \text{ mA}$ $I_O = 100 \text{ mA}$ $I_O = 250 \text{ mA}$ $I_O = 300 \text{ mA}$ $T_J = -40^\circ C$ to $+125^\circ C$	$V_{in} - V_O$	– – – –	25 115 220 260	100 200 400 500	mV
Ripple Rejection (120 Hz) $V_{in(peak-peak)} = [V_O + 1.5] \text{ V to } [V_O + 5.5] \text{ V}$	–	65	75	–	dB
Output Noise Voltage $C_L = 1.0 \mu F$ $C_L = 200 \mu F$ $I_O = 50 \text{ mA}$ (10 Hz to 100 kHz)	V_n	– –	160 46	– –	μV_{rms}

CURRENT PARAMETERS

Quiescent Current ON Mode $V_{in} = [V_O + 1] \text{ V}$, $I_O = 0 \text{ mA}$	I_{QON}	–	125	200	μA
Quiescent Current OFF Mode	I_{QOFF}	–	0.3	4.0	μA
Quiescent Current ON Mode SAT $V_{in} = [V_O - 0.5] \text{ V}$, $I_O = 0 \text{ mA}$ (Notes 2, 4) 3.0 V Suffix 3.3 V Suffix 5.0 V Suffix	I_{QSAT}	– – –	1500 1500 1500	2000 2000 2000	μA
Current Limit $V_{in} = [V_O + 1] \text{ V}$, V_O Shorted	I_{LIMIT}	–	450	–	mA

ON/OFF INPUTS

On/Off Input Voltage Logic "1" (Regulator On) $V_{out} = V_O \pm 2\%$ Logic "0" (Regulator Off) $V_{out} < 0.03 \text{ V}$ Logic "0" (Regulator Off) $V_{out} < 0.05 \text{ V}$ (1.8 V Option)	V_{CTRL}	2.4 – –	– – –	– 0.5 0.3	V
---	------------	---------------	-------------	-----------------	---

THERMAL SHUTDOWN

Thermal Shutdown	–	–	150	–	$^\circ C$
------------------	---	---	-----	---	------------

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. Quiescent Current is measured where the PNP pass transistor is in saturation. $V_{in} = [V_O - 0.5] \text{ V}$ guarantees this condition.
3. For 1.8 V version V_{DO} is constrained by the minimum input voltage of 2.5 V.
4. For 1.8 V and 2.5 V versions, I_{QSAT} is constrained by the minimum input voltage of 2.5 V.

DEFINITIONS

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Dropout Voltage – The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Output Noise Voltage – The RMS AC voltage at the output with a constant load and no input ripple, measured over a specified frequency range.

Maximum Power Dissipation – The maximum total dissipation for which the regulator will operate within specifications.

Quiescent Current – Current which is used to operate the regulator chip and is not delivered to the load.

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Maximum Package Power Dissipation – The maximum package power dissipation is the power dissipation level at which the junction temperature reaches its maximum value i.e. 150 °C. The junction temperature is rising while the difference between the input power ($V_{CC} \times I_{CC}$) and the output power ($V_{out} \times I_{out}$) is increasing.

Depending on ambient temperature, it is possible to calculate the maximum power dissipation and so the maximum current as following:

$$P_D = \frac{T_J - T_A}{R_{\theta JA}}$$

The maximum operating junction temperature T_J is specified at 150 °C, if $T_A = 25$ °C, then P_D can be found. By neglecting the quiescent current, the maximum power dissipation can be expressed as:

$$I_{out} = \frac{P_D}{V_{CC} - V_{out}}$$

The thermal resistance of the whole circuit can be evaluated by deliberately activating the thermal shutdown of the circuit (by increasing the output current or raising the input voltage for example).

Then you can calculate the power dissipation by subtracting the output power from the input power. All variables are then well known: power dissipation, thermal shutdown temperature (150 °C for MC33375) and ambient temperature.

$$R_{\theta JA} = \frac{T_J - T_A}{P_D}$$



MC33375, NCV33375 Series

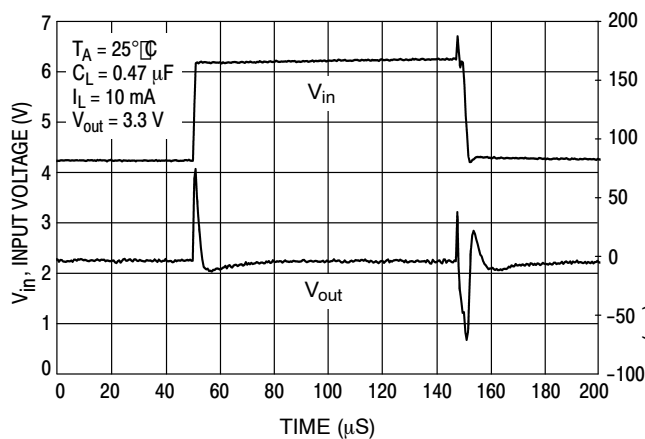


Figure 2. Line Transient Response

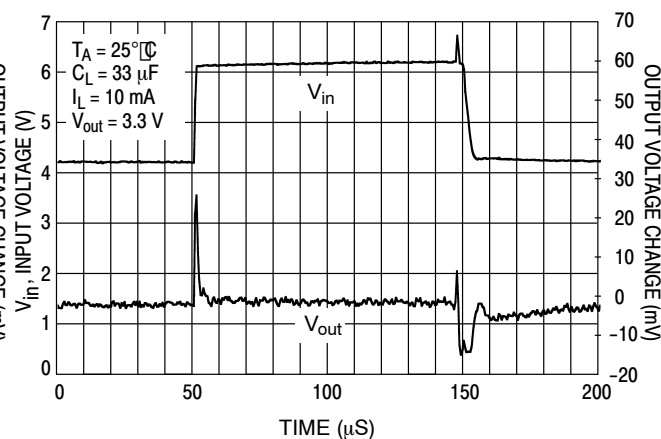


Figure 3. Line Transient Response

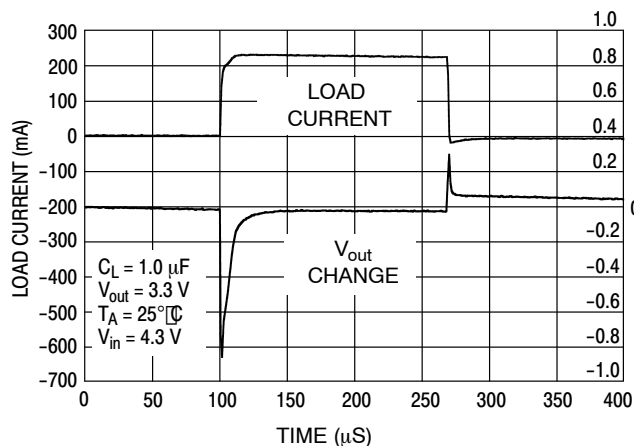


Figure 4. Load Transient Response

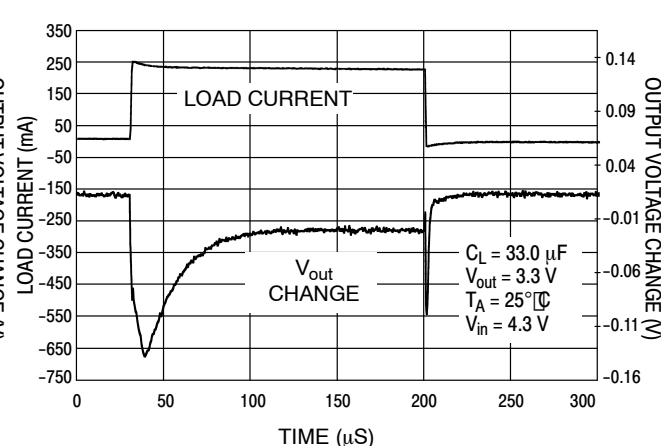


Figure 5. Load Transient Response

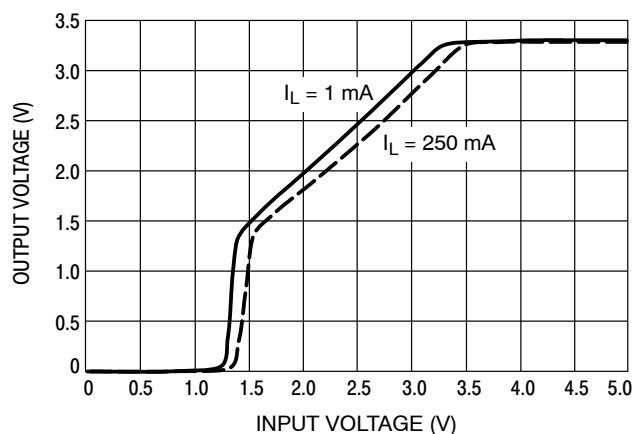


Figure 6. Output Voltage versus Input Voltage

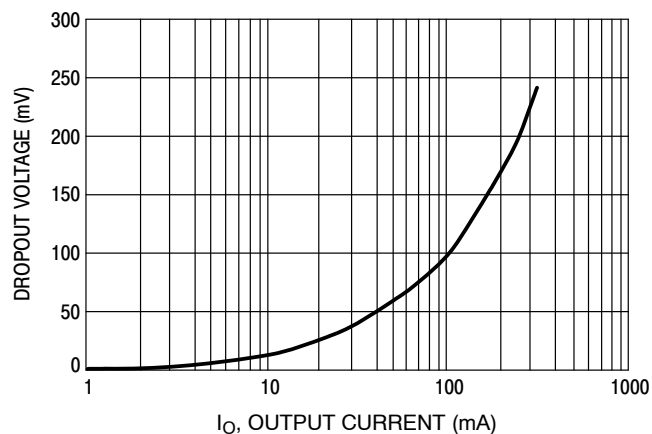


Figure 7. Dropout Voltage versus Output Current

MC33375, NCV33375 Series

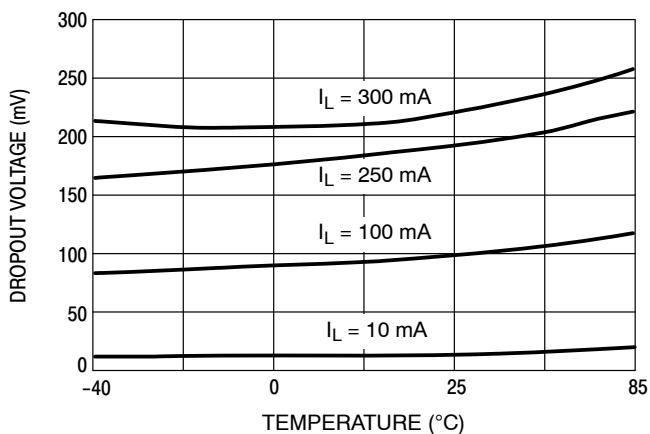


Figure 8. Dropout Voltage versus Temperature

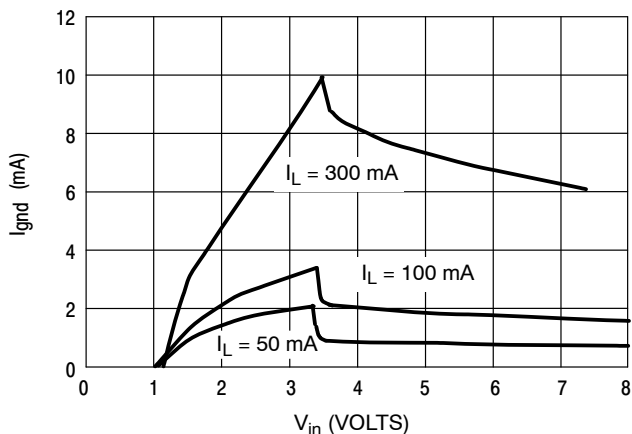


Figure 9. Ground Pin Current versus Input Voltage

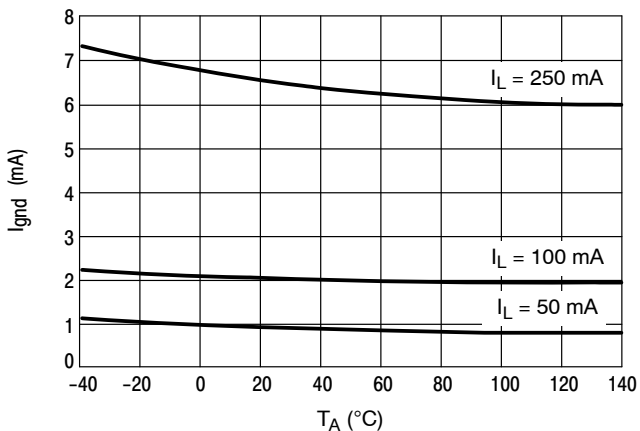


Figure 10. Ground Pin Current versus Ambient Temperature

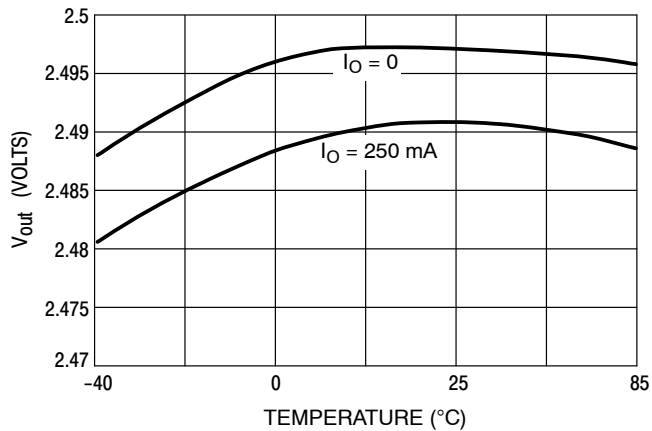


Figure 11. Output Voltage versus Ambient Temperature ($V_{in} = V_{out} + 1V$)

MC33375, NCV33375 Series

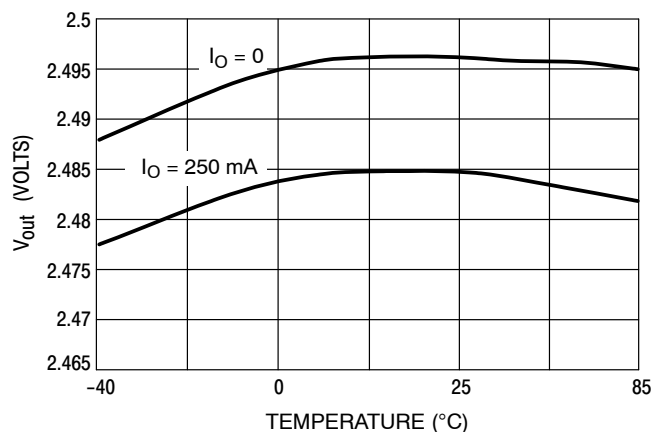


Figure 12. Output Voltage versus Ambient Temperature ($V_{in} = 12\text{ V}$)

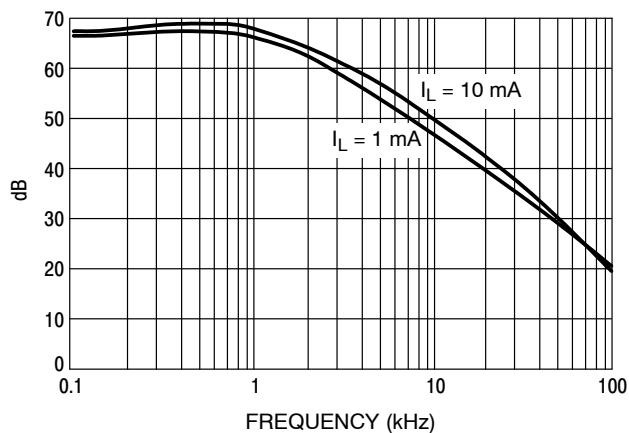


Figure 13. Ripple Rejection

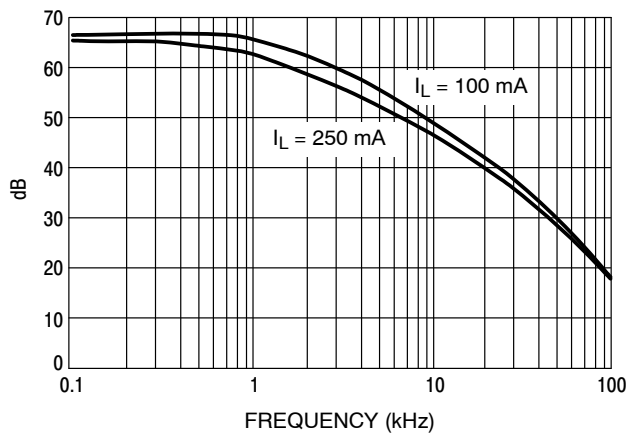


Figure 14. Ripple Rejection

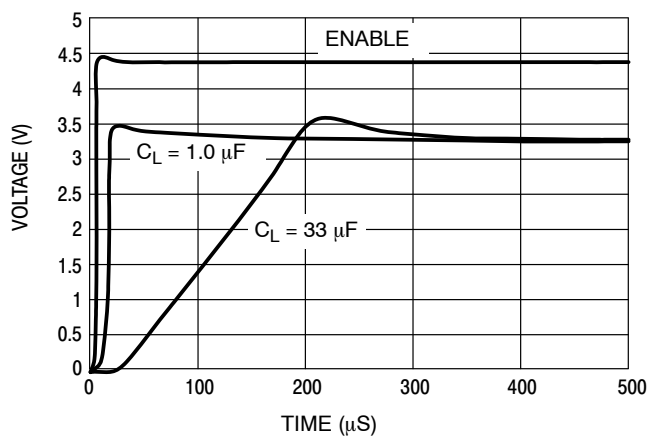


Figure 15. Enable Transient

1.8 V OPTION

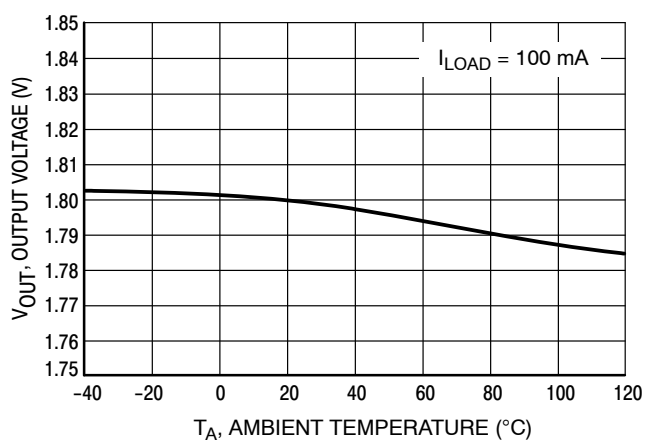


Figure 16. Output Voltage versus Temperature

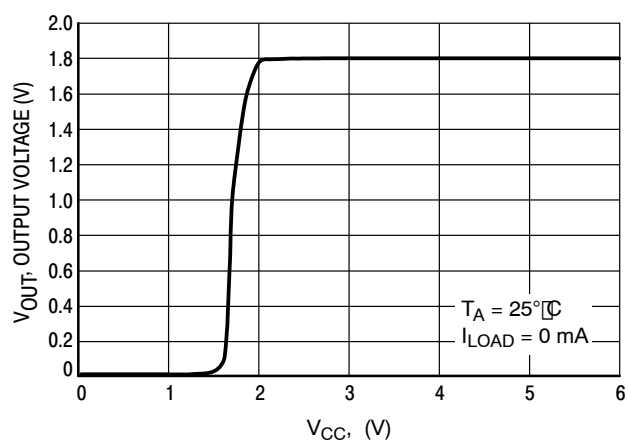


Figure 17. Output Voltage versus Input Voltage

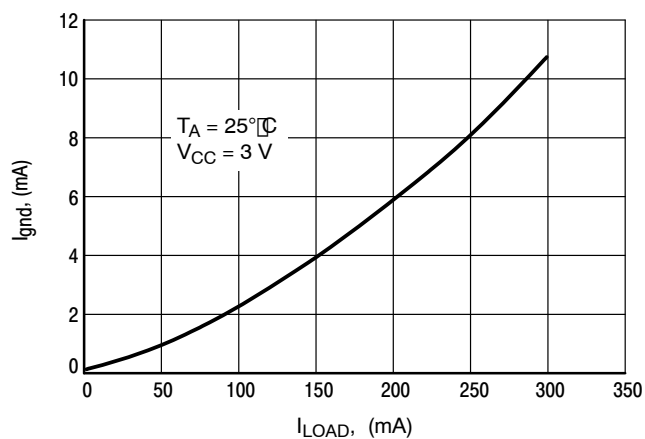


Figure 18. Ground Current versus Load Current

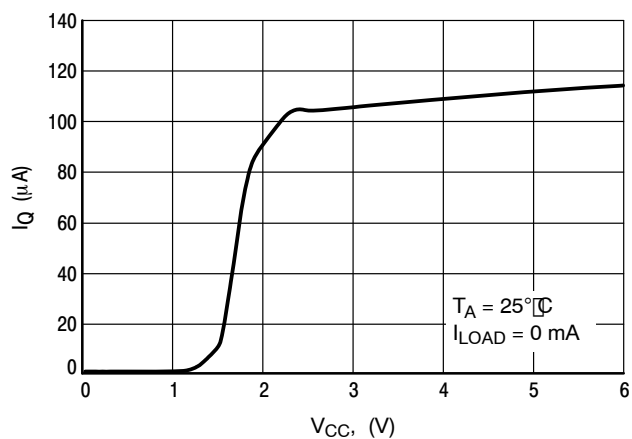


Figure 19. Quiescent Current versus Input Voltage

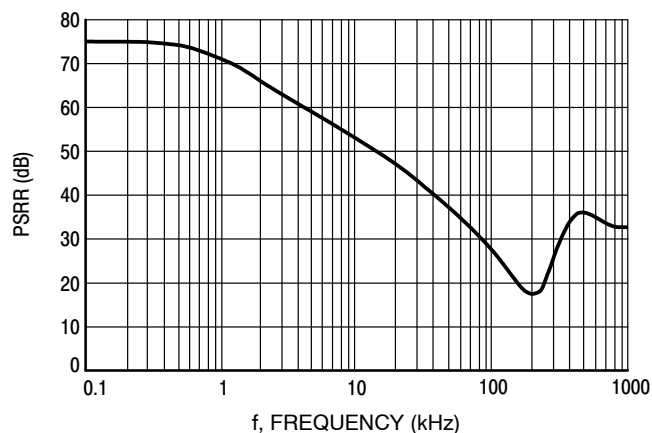


Figure 20. PSRR versus Frequency

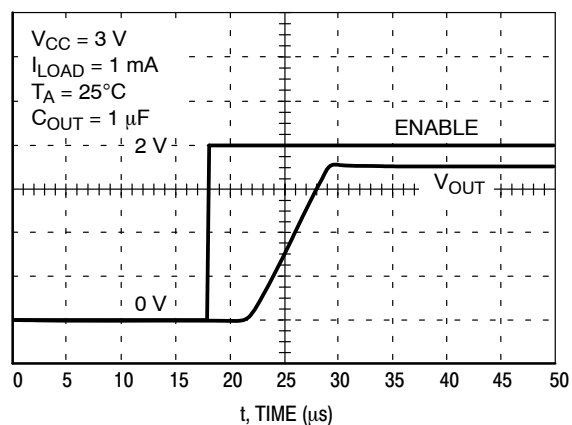


Figure 21. Enable Response

MC33375, NCV33375 Series

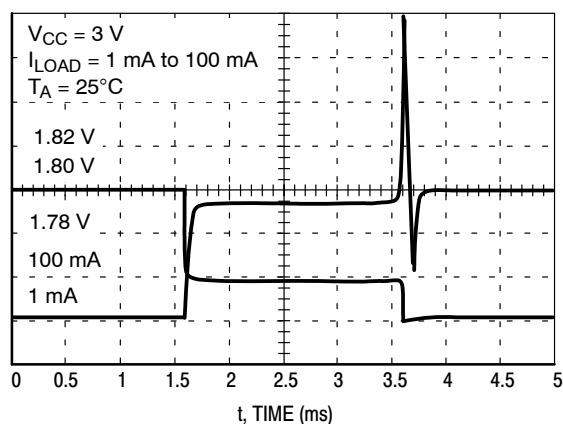


Figure 22. Load Transient Response

APPLICATIONS INFORMATION

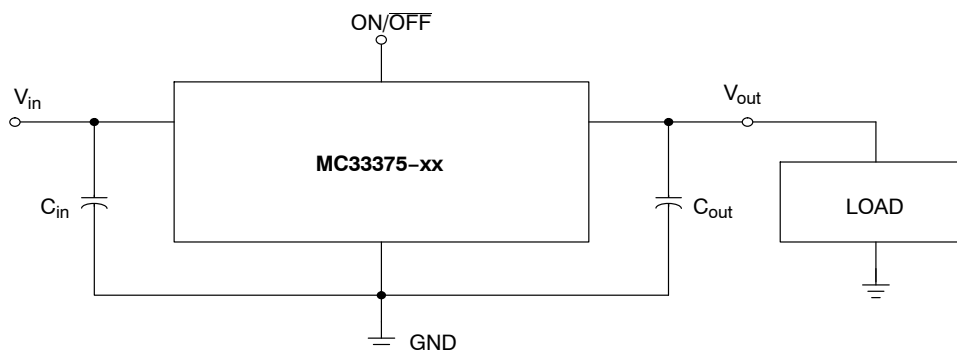


Figure 23. Typical Application Circuit

The MC33375 regulators are designed with internal current limiting and thermal shutdown making them user-friendly. Figure 15 is a typical application circuit. The output capability of the regulator is in excess of 300 mA, with a typical dropout voltage of less than 260 mV. Internal protective features include current and thermal limiting.

EXTERNAL CAPACITORS

These regulators require only a 0.33 μF (or greater) capacitance between the output and ground for stability for 1.8 V, 2.5 V, 3.0 V, and 3.3 V output voltage options. Output voltage options of 5.0 V require only 0.22 μF for stability. The output capacitor must be mounted as close as possible to the MC33375. If the output capacitor must be mounted further than two centimeters away from the MC33375, then a larger value of output capacitor may be required for stability. A value of 0.68 μF or larger is recommended. Most type of aluminum, tantalum, or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below 25 °C. An input bypass capacitor is recommended to improve transient response or if the regulator is connected to the supply input filter with long wire lengths, more than 4 inches. This will reduce the

circuit's sensitivity to the input line impedance at high frequencies. A 0.33 μF or larger tantalum, mylar, ceramic, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with shortest possible lead or track length directly across the regulator's input terminals. Figure 16 shows the ESR that allows the LDO to remain stable for various load currents.

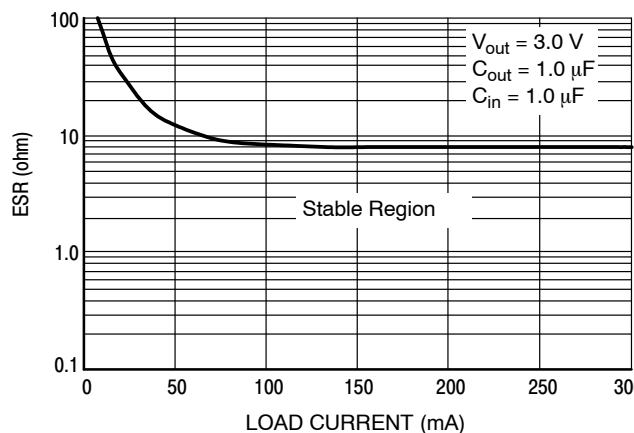


Figure 24. ESR for $V_{\text{out}} = 3.0\text{V}$

MC33375, NCV33375 Series

Applications should be tested over all operating conditions to insure stability.

THERMAL PROTECTION

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 150 °C, the output is disabled. There is no hysteresis built into the thermal protection. As a result the output will appear to be oscillating during thermal limit. The output will turn off until the temperature drops below the 150 °C then the output turns on again. The process will repeat if the junction increases above the threshold. This will continue until the existing conditions allow the junction to operate below the temperature threshold.

Thermal limit is not a substitute for proper heatsinking.

The internal current limit will typically limit current to 450 mA. If during current limit the junction exceeds 150 °C, the thermal protection will protect the device also. **Current limit is not a substitute for proper heatsinking.**

OUTPUT NOISE

In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor will reduce the noise on the MC33375.

ON/OFF PIN

When this pin is pulled low, the MC33375 is off. This pin should not be left floating. The pin should be pulled high for the MC33375 to operate.

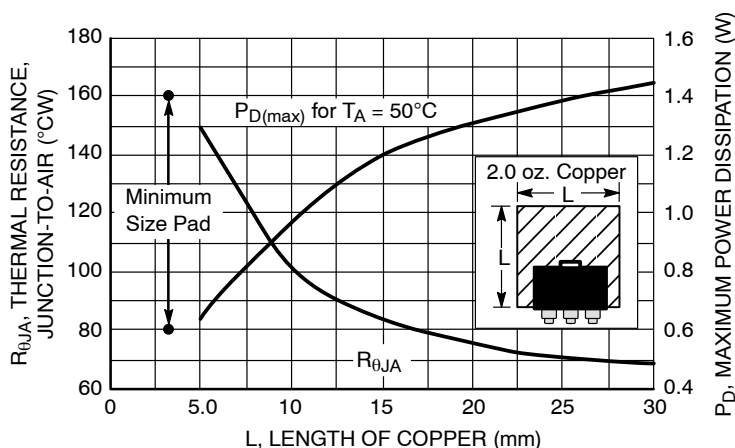


Figure 25. SOT-223 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

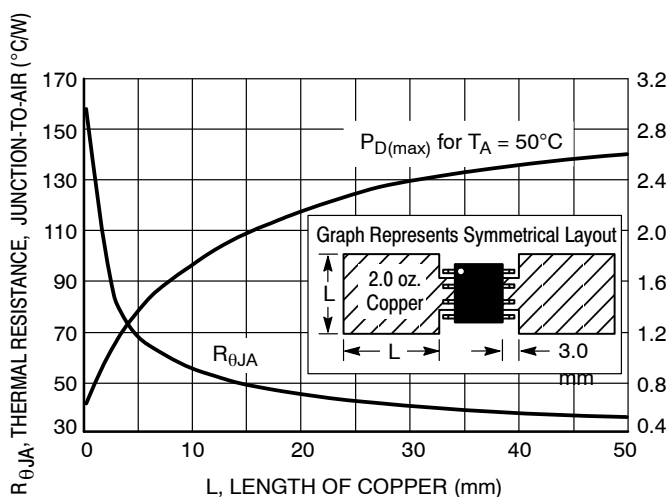


Figure 26. SOP-8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

MC33375, NCV33375 Series

ORDERING INFORMATION

Device	Type	Operating Temperature Range, Tolerance	Package	Shipping [†]
MC33375ST-1.8T3G	1.8 V (Fixed Voltage)	1% Tolerance at T _A = 25 °C 2% Tolerance at T _J from -40 to +125 °C	SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV33375ST1.8T3G*				
MC33375D-2.5G	2.5 V (Fixed Voltage)		SOIC-8 (Pb-Free)	98 Units / Rail
MC33375ST-3.3T3G	3.3 V (Fixed Voltage)		SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV33375ST3.3T3G*				
NCV33375D-5.0R2G*	5.0 V (Fixed Voltage)		SOIC-8 (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 5)

MC33375D-2.5R2G	2.5 V (Fixed Voltage)	1% Tolerance at T _A = 25 °C 2% Tolerance at T _J from -40 to +125 °C	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCV33375D-2.5R2G*	2.5 V (Fixed Voltage)		SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC33375ST-2.5T3G	2.5 V (Fixed Voltage)		SOT-223 (Pb-Free)	4000 / Tape & Reel
MC33375D-3.0G	3.0 V (Fixed Voltage)		SOIC-8 (Pb-Free)	98 Units / Rail
MC33375D-3.0R2G	3.0 V (Fixed Voltage)		SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC33375ST-3.0T3G	3.0 V (Fixed Voltage)		SOT-223 (Pb-Free)	4000 / Tape & Reel
MC33375D-3.3G	3.3 V (Fixed Voltage)		SOIC-8 (Pb-Free)	98 Units / Rail
MC33375D-3.3R2G	3.3 V (Fixed Voltage)		SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCV33375D-3.3R2G*	3.3 V (Fixed Voltage)		SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC33375D-5.0G	5.0 V (Fixed Voltage)		SOIC-8 (Pb-Free)	98 Units / Rail
MC33375D-5.0R2G	5.0 V (Fixed Voltage)		SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC33375ST-5.0T3G	5.0 V (Fixed Voltage)		SOT-223 (Pb-Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

* NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

5. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

DEVICE MARKING

Device	Version	Marking (1st line)
MC33375, NCV33375	1.8 V	37518
MC33375, NCV33375	2.5 V	37525
MC33375	3.0 V	37530
MC33375, NCV33375	3.3 V	37533
MC33375, NCV33375	5.0 V	37550



MC33375, NCV33375 Series

REVISION HISTORY

Revision	Description of Changes	Date
19	Rebranded the Data Sheet to onsemi format. MC33375D-2.5R2G, NCV33375D-2.5R2G, MC33375ST-2.5T3G, MC33375D-3.0G, MC33375D-3.0R2G, MC33375ST-3.0T3G, MC33375D-3.3G, MC33375D-3.3R2G, NCV33375D-3.3R2G, MC33375D-5.0G, MC33375D-5.0R2G, MC33375ST-5.0T3G OPNs Marked as Discontinued.	07/31/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

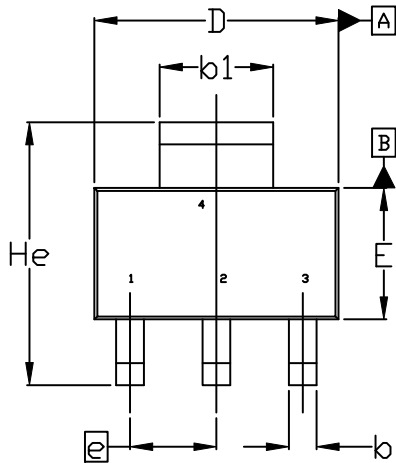




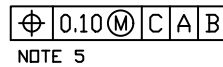
SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

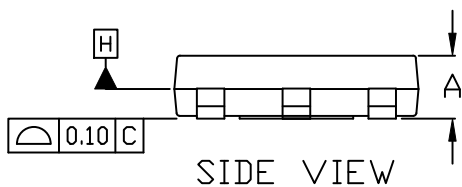
DATE 02 OCT 2018



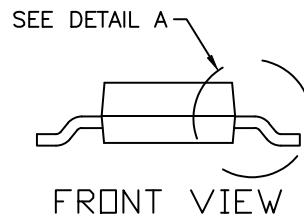
TOP VIEW



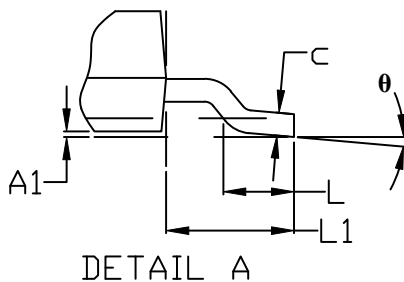
NOTE 5



SIDE VIEW



FRONT VIEW

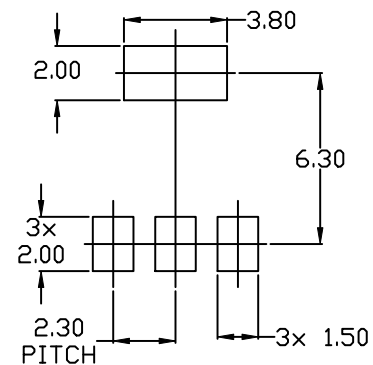


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING
FOOTPRINT

DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-223 (TO-261)	PAGE 1 OF 2

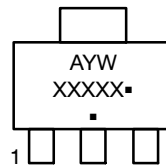
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

**GENERIC
MARKING DIAGRAM***

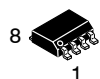


A = Assembly Location
 Y = Year
 W = Work Week
 XXXXX = Specific Device Code
 ■ = Pb-Free Package

(Note: Microdot may be in either location)
 *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-223 (TO-261)	PAGE 2 OF 2

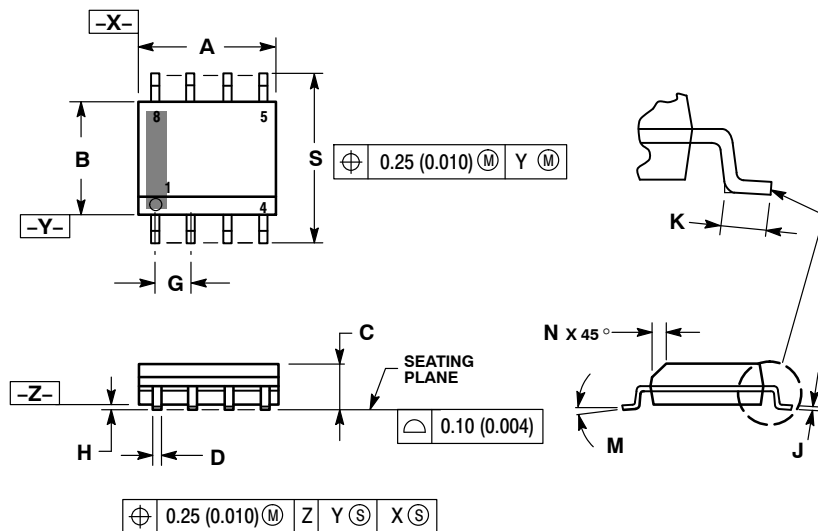
onsemi and **Onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

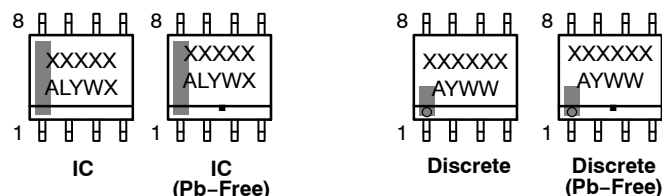
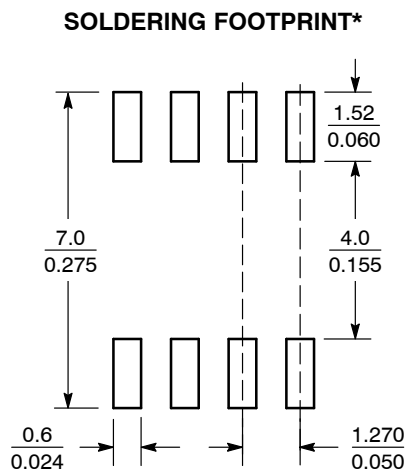


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

